INTEGRATED CIRCUITS

Semiconductors for Wired Telecom Systems

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Data Handbook IC03a

Let's make things better.

Philips Semiconductors

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QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be ‘chemical’, ‘special’ or sometimes ‘industrial’ waste. Disposal as domestic waste is usually not permitted.

PREFACE

Thank you for your interest in wired telecom products from Philips Semiconductors. As a leading supplier to the telephony market, we offer a wide range of discrete and integrated semiconductor telecom components.

A DETAILED REFERENCE SOURCE

This wired telecom handbook includes information on Philips Semiconductors current integrated circuits and discrete products for wired applications. The products offer a comprehensive solution for wired telephony terminals, from line-interfaces, tone and pulse diallers and discrete devices though to hands-free circuits and LCD drivers.

To make selection easier, information is grouped into sections, each accompanied by a product selector guide, which describes the most significant product features. Each section contains detailed product descriptions in the form of data sheets.

Relevant application notes are published in the Application Handbook for Wired Telecom Systems (IC03b). Together IC03 part a) and b) provides a comprehensive reference source for wired telephony, including not only details about Philips Semiconductors products, but also how best to apply them. Summaries of the application notes available for wired telecom systems are on page 41, which also indicates how to order the application handbook (IC03b)

COMPREHENSIVE SOLUTIONS

Philips Semiconductors is a recognised leader in enabling technologies, system-level Know-How, silicon, software and product development resources to help customers take full advantage of one of the fastest growing markets in the world. Specifically the company is a leading innovator of products for:

- Speech and Transmission circuits.
- Listening-in and hands-free circuits.
- Diallers and DTMF generators.
- Derivative telephony-specific micro-controllers; the largest range of configurations and performance options, including low-voltage devices operating down to 1.8V.
- Low-voltage one-time-programmable (OTP) devices, including the PCD3755/56, the lowest-voltage OTP on the market!
- Bipolar transistors, regulators and protection diodes.
- LCD display drivers (available additionally as naked die or as chip-on-glass module assemblies).

TECHNOLOGY LEADER

Implementation of cost-effective Telecom terminals demands a broad knowledge, not only at the systems level, but also at the interconnection and component level. Philips Semiconductors state-of-the art fabrication and packaging expertise provides the technology needed for today's demanding applications, together with the reliability and quality levels customers have come to rely upon from one of the world's top-ten semiconductor companies.

UNRIVALLED RESOURCES

Philips Semiconductors has one of the widest portfolios of technology in Semiconductors to meet the needs of the wired telephony market. World-class designs, advanced fabrication processes and up-to-date manufacturing plans and logistics has established Philips Semiconductors as a world supplier. Quality Assurance is based on internationally-accepted quality standards such as ISO9000 as well as customer-specific standards such as Ford's TQE - awarded to Philips Semiconductors in 1995, and AT&T's 'Partner in Excellence' award in 1995, which will honour only five suppliers (including only two semiconductor suppliers) this year.

CUSTOMER CO-OPERATION

Co-operation with customers is vital for securing market acceptance of customers' products and our own. In addition, we believe that technical partnerships are extremely important for stimulating further development of advanced Telecom technology, and have successful partnerships with major Telecom systems suppliers and terminal makers.

WORLD-WIDE RESEARCH AND DESIGN-IN SUPPORT

Over 18 per cent of our turnover is invested back into research and development, covering process technology, design, system innovation, type/product development and assembly technology. The result is over 300 new devices per year, along with new technology and process developments, software and services.

We have our own divisional PCALs (Product Concept and Application Laboratories), which explore new uses and applications; act as design and development laboratories to uncover potential problems from customers and help them develop their products faster through shared development; and replicate customer engineering efforts in-house.

Product development teams located at our manufacturing and development sites are technology-oriented. Many of our new products are the direct result of work done by the development teams, working alone, or in conjunction with groups in the Research or Applications Laboratories.

Philips Corporate Research Labs

- Eindhoven, The Netherlands
- Redhill, UK
- Limeil-BrÈvannes, France
- Aachen/Hamburg, Germany
- Briarcliff Manor, USA

Philips System Labs

- Eindhoven, The Netherlands
  - TV, Telephony, Micro-controllers
- Southampton, UK
  - Teletext, digital audio, software for TV and CD-ROM
- Hamburg, Germany
  - Automotive, identification, DSP in radio and TV, Multimedia
- Sunnyvale, USA
  - Multimedia, datacom, automotive
- Taipei, Taiwan
  - In construction

Product Development Teams

- Caen, France
  - Speech and Transmission circuits, hands-free Ics
- Zürich, Switzerland
  - Telecom Microcontrollers, LCD drivers, peripheral Ics
- Hamburg, Germany
- Nijmegen, The Netherlands
- Stadskanaal, The Netherlands
  - Discrete semiconductors and regulators

Semiconductors for Wired Telecom Systems

CONTENTS

	Page
PREFACE	3
SELECTION GUIDE	5
GENERAL	27
APPLICATION NOTES SUMMARIES	41
DEVICE DATA (in alphanumeric sequence)	57
PACKAGE INFORMATION	873
DATA HANDBOOK SYSTEM	898

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I^2C COMPONENTS

Purchase of Philips I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

SELECTION GUIDE

Page

Functional index 6

Alphanumeric index 9

Replacement list 12

Selection lists 15

SPEECH/TRANSMISSION CIRCUITS

		PAGE
PCA1070	Multistandard programmable analog CMOS transmission IC	110
TEA1060; TEA1061	Versatile telephone transmission circuits with dialler interfac	483
TEA1062; TEA1062A	Low-voltage transmission circuit with dialler interface	500
TEA1064A	Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting	521
TEA1064B	Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting	549
TEA1065	Versatile telephone transmission circuit with dialler interface	576
TEA1066T	Versatile telephone transmission circuit with dialler interface	595
TEA1067	Low voltage versatile telephone transmission circuit with dialler interface	613
TEA1068	Versatile telephone transmission circuit with dialler interface	632
TEA1112; TEA1112A	Low voltage versatile transmission circuits with dialler interface	802
TEA1113	Low voltage versatile telephone transmission circuit with dialler interface	821
TEA1118; TEA1118A	Versatile cordless transmission	835

LISTENING-IN CIRCUITS

TDA7050	Low voltage mono/stereo power amplifier	466
TDA7050T	Low voltage mono/stereo power amplifier	471
TDA7052A/AT	1 W BTL mono audio amplifier	475
TEA1083; TEA1083A	Call progress monitor for line powered telephone sets	682
TEA1085; TEA1085A	Listening-in circuit for line powered telephone sets	699
TEA1096; 1096A	Speech and listening-in IC	781

HANDS-FREE CIRCUITS

TEA1093	Hands-free IC	722
TEA1094; TEA1094A	Hands-free IC	744
TEA1095	Noise switched speakerphone IC	763

SINGLE-CHIP TELEPHONE IC

TEA1069N	Versatile speech/dialler/ringer with music-on-hold	649

DIALLERS AND DTMF GENERATORS

PCD3310 family	Pulse and DTMF dialler with redial	141
PCD3311C; PCD3312C	DTMF/modem/musical-tone generators	154
PCD3330	Multistandard repertory dialler/ringer with EEPROM	176
PCD3332-X family	Multistandard pulse/tone repertory dialler/ringer	179

COMPLEMENTARY PRODUCTS

		PAGE
NE/SE567	Tone decoder/phase-locked loop	90
NE5900	Call progress decoder	103
PCD3360	Programmable multi-tone telephone ringer	321
PCD4440T	analog voice scrambler/descrambler	411
TEA1081	Supply circuit with power-down for telephone set peripherals	680
UBA1702; UBA1702A	Line interrupter driver and ringer	850

MICROCONTROLLERS

PCD33XXA family	8-bit telecom microcontroller	334
PCD3344A; PCD3349A	8-bit microcontroller with DTMF generator	201
PCD3350A	8-bit microcontroller with DTMF generator and 256 bytes EEPROM and real-time clock	215
PCD3351A/52A/53A; PCA3351C/52C/53C	8-bit microcontroller with DTMF generator and 128 bytes EEPROM	246
PCD3354A/54C	8-bit microcontroller with DTMF generator and 256 bytes EEPROM	271
PCD3356A/57A/59A	8-bit microcontroller with DTMF generator and 128 bytes EEPROM	296
PCD3755X	8-bit microcontroller with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM	362
PCD3756X	8-bit microcontroller with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM	386
PCF84C12A/22A/42A	8-bit microcontroller	425

BIPOLAR TRANSISTORS, D-MOS-FETs SWICHTES, REGULATOR AND PROTECTION DIODES

2N5400; 2N5401	Silicon PNP high-voltage transistor	869
2N5550; 2N5551	Silicon NPN high-voltage transistor	870
2N7000	N-channel enhancement mode vertical D-MOS transistor	871
2N7002	N-channel vertical D-MOS transistor	872
BC327; BC327A; BC328	Silicon planar epitaxial transistor	58
BC337; BC337A; BC338	Silicon planar epitaxial transistor	59
BC546; BC547; BC548	Silicon planar epitaxial transistor	60
BC556; BC557; BC558	Silicon planar epitaxial transistor	61
BC846; BC847; BC848	Silicon planar epitaxial transistor	62
BC856/7/8	Silicon planar epitaxial transistor	63
BR211 series	Breakover diodes	64
BS107	N-channel enhancement mode vertical D-MOS transistor	65
BS107A	N-channel enhancement mode vertical D-MOS transistor	66
BS108	N-channel enhancement mode vertical D-MOS transistor	67
BS170	N-channel vertical D-MOS transistor	68
BSN10; BSN10A	N-channel enhancement mode vertical D-MOS transistor	69
BSN20	N-channel enhancement mode vertical D-MOS transistor	70

		PAGE
BSN254; BSN254A	N-channel enhancement mode vertical D-MOS transistor	71
BSN274; BSN274A	N-channel enhancement mode vertical D-MOS transistor	72
BSN304; BSN304A	N-channel enhancement mode vertical D-MOS transistor	73
BSP126	N-channel enhancement mode vertical D-MOS transistor	74
BSP130	N-channel enhancement mode vertical D-MOS transistor	75
BSP145	N-channel enhancement mode vertical D-MOS transistor	76
BSP225	P-channel enhancement mode vertical D-MOS transistor	72
BSP254; BSP254A	P-channel enhancement mode vertical D-MOS transistor	78
BSP304; BSP304A	P-channel enhancement mode vertical D-MOS transistor	79
BSP92	P-channel enhancement mode vertical D-MOS transistor	80
BSS89	N-channel enhancement mode vertical D-MOS transistor	81
BSS92	P-channel enhancement mode vertical D-MOS transistor	82
BST124	N-channel depletion mode vertical D-MOS transistor	83
BST74A	N-channel vertical D-MOS transistor	84
BZW03 series	Regulator diodes	85
BZW14	Transient suppressor diode	86
MPSA42; MPSA43	High-voltage silicon planar transistor	87
MPSA44; MPSA45	NPH high-voltage transistor	88
MPSA92; MPSA93	High-voltage silicon planar transistor	89
PMBF107	P-channel enhancement mode vertical D-MOS transistor	451
PMBF170	N-channel enhancement mode vertical D-MOS transistor	452
PMBTA42; PMBTA43	Silicon epitaxial transistor	453
PMBTA92; PMBTA93	Silicon epitaxial transistor	456
PZTA42; PZTA43	Silicon epitaxial transistor	458
PZTA44; PZTA45	NPN high-voltage transistor	461
PZTA92; PZTA93	Silicon epitaxial transistor	464
VN2406L	N-channel enhancement mode vertical D-MOS transistor	868

LCD DRIVERS AND MOCIROCONTROLLER PERIPHERALS

PCA8581; PCA8581C	128 x 8-bit EEPROM with I2C-bus interface	138
PCF2104 family	LCD controller/drivers	417
PCF2116 family (PCF2114X; PCF2116X)	LCD controller/drivers	420
PCF8566	Universal LCD driver for low multiplex rates	435
PCF8574	Remote 8-bit I/O expander for I2C-bus	438
PCF8576C	Universal LCD driver for low multiplex rates	441
PCF8578	LCD row/column driver for dot matrix graphic displays	446
PCF8593	Low power clock calendar	449

Alphanumeric index

		PAGE
BC327; BC327A; BC328	Silicon planar epitaxial transistor	58
BC337; BC337A; BC338	Silicon planar epitaxial transistor	59
BC546; BC547; BC548	Silicon planar epitaxial transistor	60
BC556; BC557; BC558	Silicon planar epitaxial transistor	61
BC846; BC847; BC848	Silicon planar epitaxial transistor	62
BC856/7/8	Silicon planar epitaxial transistors	63
BR211 series	Breakover diodes	64
BS107	N-channel enhancement mode vertical D-MOS transistor	65
BS107A	N-channel enhancement mode vertical D-MOS transistor	66
BS108	N-channel enhancement mode vertical D-MOS transistor	67
BS170	N-channel vertical D-MOS transistor	68
BSN10; BSN10A	N-channel enhancement mode vertical D-MOS transistor	69
BSN20	N-channel enhancement mode vertical D-MOS transistor	70
BSN254; BSN254A	N-channel enhancement mode vertical D-MOS transistor	71
BSN274; BSN274A	N-channel enhancement mode vertical D-MOS transistor	72
BSN304; BSN304A	N-channel enhancement mode vertical D-MOS transistor	73
BSP126	N-channel enhancement mode vertical D-MOS transistor	74
BSP130	N-channel enhancement mode vertical D-MOS transistor	75
BSP145	N-channel enhancement mode vertical D-MOS transistor	76
BSP225	P-channel enhancement mode vertical D-MOS transistor	77
BSP254; BSP254A	P-channel enhancement mode vertical D-MOS transistor	78
BSP304; BSP304A	P-channel enhancement mode vertical D-MOS transistor	79
BSP92	P-channel enhancement mode vertical D-MOS transistor	80
BSS89	N-channel enhancement mode vertical D-MOS transistor	81
BSS92	P-channel enhancement mode vertical D-MOS transistor	82
BST124	N-channel depletion mode vertical D-MOS transistor	83
BST74A	N-channel vertical D-MOS transistor	84
BZW03 series	Regulator diodes	85
BZW14	Transient suppressor diode	86
MPSA42; MPSA43	High-voltage silicon planar transistor	87
MPSA44; MPSA45	NPN high-voltage transistor	88
MPSA92; MPSA93	High-voltage silicon planar transistor	89
NE/SE567	Tone decoder/phase-locked loop	90
NE5900	Call progress decoder	103
PCA1070	Multistandard programmable analog CMOS transmission IC	110
PCA8581; PCA8581C	128 x 8-bit EEPROM with I2C-bus interface	138
PCD3310 family	Pulse and DTMF dialler with redial	141
PCD3311C; PCD3312C	DTMF/modem/musical-tone generators	159
PCD3330	Multistandard repertory dialler/ringer with EEPROM	176
PCD3332-X family	Multistandard pulse/tone repertory dialler/ringer	179

		PAGE
PCD3344A; PCD3349A	8-bit microcontroller with DTMF generator	201
PCD3350A	8-bit microcontroller with DTMF generator and 256 bytes EEPROM and real-time clock	215
PCA3351C/52C/53C; PCD3351A/52A/53A	8-bit microcontroller with DTMF generator and 128 bytes EEPROM	246
PCD3354A/54C	8-bit microcontroller with DTMF generator and 256 bytes EEPROM	271
PCD3356A/57A/59A	8-bit microcontroller with DTMF generator and 128 bytes EEPROM	296
PCD3360	Programmable multi-tone telephone ringer	321
PCD33XXA Family	8-bit telecom microcontroller	334
PCD3755X	8-bit microcontroller with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM	362
PCD3756X	8-bit microcontroller with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM	386
PCD4440T	Analog voice scrambler/descrambler	411
PCF2104 family	LCD controller/drivers	417
PCF2116 family	LCD controller/drivers	420
PCF84C12A/22A/42A	8-bit microcontroller	425
PCF8566	Universal LCD driver for low multiplex rates	435
PCF8574	Remote 8-bit I/O expander for I2C-bus	438
PCF8576C	Universal LCD driver for low multiplex rates	441
PCF8578	LCD row/column driver for dot matrix graphic displays	446
PCF8593	Low power clock calendar	449
PMBF107	P-channel enhancement mode vertical D-MOS transistor	451
PMBF170	N-channel enhancement mode vertical D-MOS transistor	452
PMBTA42; PMBTA43	Silicon epitaxial transistor	453
PMBTA92; PMBTA93	Silicon epitaxial transistor	456
PZTA42; PZTA43	Silicon epitaxial transistor	458
PZTA44; PZTA45	NPN high-voltage transistor	461
PZTA92; PZTA93	Silicon epitaxial transistor	464
TDA7050	Low voltage mono/stereo power amplifier	466
TDA7050T	Low voltage mono/stereo power amplifier	471
TDA7052 A/AT	1 W BTL mono audio amplifier	475
TEA1060; TEA1061	Versatile telephone transmission circuits with dialler interface	483
TEA1062; TEA1062A	Low-voltage transmission circuit with dialler interface	500
TEA1064A	Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting	521
TEA1064B	Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting	549
TEA1065	Versatile telephone transmission circuit with dialler interface	576
TEA1066T	Versatile telephone transmission circuit with dialler interface	595
TEA1067	Low voltage versatile telephone transmission circuit with dialler interface	613
TEA1068	Versatile telephone transmission circuit with dialler interface	632

		PAGE
TEA1069N	Versatile speech/dialler/ringer with music-on-hold	649
TEA1081	Supply circuit with power-down for telephone set peripherals	680
TEA1083; TEA1083A	Call progress monitor for line powered telephone sets	687
TEA1085; TEA1085A	Listening-in circuit for line powered telephone sets	699
TEA1093	Hands-free IC	722
TEA1094; TEA1094A	Hands-free IC	744
TEA1095	Noise switched speakerphone IC	763
TEA1096; 1096A	Speech and listening-in IC	781
TEA1112; TEA1112A	Low voltage versatile transmission circuits with dialler interface	807
TEA1113	Low voltage versatile telephone transmission circuit with dialler interface	821
TEA1118; TEA1118A	Versatile cordless transmission	835
UBA1702; UBA1702A	Line interrupter driver and ringer	850
VN2406L	N-channel enhancement mode vertical D-MOS transistor	868
2N5400; 2N5401	Silicon PNP high-voltage transistor	869
2N5550; 2N5551	Silicon NPN high-voltage transistor	870
2N7000	N-channel enhancement mode vertical D-MOS transistor	871
2N7002	N-channel vertical D-MOS transistor	872

REPLACEMENT/WITHDRAWAL TYPES

The following type numbers were in the previous issue of this data handbook, but not in the current version:

TYPE NUMBER	REPLACED BY	REASON FOR DELETION
CT914; CT918		Transferred to IC17
MC3361		Discontinued
NE570/571/SA571		Transferred to IC17
NE/SA572		Transferred to IC17
NE/SA575		Transferred to IC17
NE/SA576		Transferred to IC17
NE/SA577		Transferred to IC17
NE/SA578		Transferred to IC17
NE/SA600		Transferred to IC17
NE/SA602A		Transferred to IC17
NE/SA604A		Transferred to IC17
NE/SA605		Transferred to IC17
NE/SA612A		Transferred to IC17
NE/SA614A		Transferred to IC17
NE/SA615		Transferred to IC17
NE/SA624		Transferred to IC17
NE/SA625		Transferred to IC17
NE/SA627		Transferred to IC17
NE/SA630		Transferred to IC17
NE/SA5200		Transferred to IC17
NE/SA/SE5205A		In IC11
NE/SA5209		Transferred to IC17
NE/SA5219		Transferred to IC17
NE/SA5234		In IC11
NE/SA5750		Transferred to IC17
NE/SA5751		Transferred to IC17
OM4031T		Transferred to IC17
OM5300		discontinued
OM5301		discontinued
OM5302		discontinued
PCA5000AT		Transferred to IC17
PCD332XC family		discontinued
PCD3315A		discontinued
PCD3343A; PCD3348A		discontinued
PCD3346		discontinued
PCD3347		discontinued
PCD5002		Transferred to IC17
PCD5003		Transferred to IC17
PCD5032		Transferred to IC17

TYPE NUMBER	REPLACED BY	REASON FOR DELETION
PCD5040/PCD5041		Transferred to IC17
PCF5001		Transferred to IC17
PCF5075		Transferred to IC17
PCF5081		Transferred to IC17
PCF5083		Transferred to IC17
PCF8591		In IC12
SA601		Transferred to IC17
SA606		Transferred to IC17
SA607		Transferred to IC17
SA608		Transferred to IC17
SA616		Transferred to IC17
SA617		Transferred to IC17
SA620		Transferred to IC17
SA626		Transferred to IC17
SA636		Transferred to IC17
SA637		Transferred to IC17
SA639		Transferred to IC17
SA701		Transferred to IC17
SA702		Transferred to IC17
SA703		Transferred to IC17
SA900		Transferred to IC17
SA1620		Transferred to IC17
SA1638		Transferred to IC17
SA5752		Transferred to IC17
SA5753		Transferred to IC17
SA7025		Transferred to IC17
SA8025		Transferred to IC17
SAA1500T		Transferred to IC17
SAA1501T		Transferred to IC17
TDA1010A		In IC01
TDA1011		In IC01
TDA1015T		In IC01
TDA1576T		In IC01
TDA8041H		In IC02
TDA8568		discontinued
TDA8569		discontinued
TDA8579		discontinued
TDA8780M		Transferred to IC17
TDA8781T		discontinued
TDD1742T		Transferred to IC17
TEA1041T		Transferred to IC17

TYPE NUMBER	REPLACED BY	REASON FOR DELETION
TEA1088T		Transferred to IC17
TEA1100; TEA1100T		Transferred to IC17
TEA1101; TEA1101T		Transferred to IC17
TEA1102		Transferred to IC17
TEA1104		Transferred to IC17
UAA2050T		Transferred to IC17
UAA2072M		Transferred to IC17
UAA2073AM		Transferred to IC17
UAA2073M		Transferred to IC17
UAA2076G		Transferred to IC17
UAA2077AM		Transferred to IC17
UAA2077BM		Transferred to IC17
UAA2080		Transferred to IC17
UAA2082		Transferred to IC17
UMA1000LT		Transferred to IC17
UMA1002		Transferred to IC17
UMA1005T		Transferred to IC17
UMA1014		Transferred to IC17
UMA1015M		Transferred to IC17
UMA1016XT		Transferred to IC17
UMA1017M		Transferred to IC17
UMA1018M		Transferred to IC17
UMA1019AM		Transferred to IC17
UMA1019M		Transferred to IC17
UMA1020AM		Transferred to IC17
UMA1020M		Transferred to IC17
UMA1021M		Transferred to IC17
UMA1022		Transferred to IC17
UMF1000T		discontinued

LISTENING-IN ICs

PRODUCT TYPE	DESCRIPTION	SUPPLY VOLTAGE (V)	LINE-POWERED	CURRENT CONSUMPTION (mA) TYP.	PD	LOUDSPEAKER GAIN (dB)	R_{xout}[1]	PACKAGE	PAGE
TDA7050	loudspeaker amplifier	1.6-6.0	No	3.2	No	26	BTL	DIP8, SO8	466
TDA7052	loudspeaker amplifier	3-18	No	4	No	39	BTL	DIP8	475
TEA1083	call-progress monitoring IC	3.0	Yes	2.5	No	35	SEL	DIP8	687
TEA1083A	TEA1083 with PD	3.0	Yes	2.5	Yes	35	SEL	DIP16, SO16	687
TEA1085	TEA1083A with dynamic limiter, Larsen level limiter and volume control	3.6 adjustable	Yes	4.2	Yes	41	BTL	DIP24, SO24	699
TEA1085A	TEA1085 with logic MUTE function instead of toggle function	3.6 adjustable	Yes	4.2	Yes	41	BTL	DIP24, SO24	699
TEA1096	speech and listening-in IC	3.6 adjustable supplied by speech part	Yes	2.4	Yes	35.5	SEL	DIP28, SO28	781
TEA1096A	speech and listening-in IC with volume control	3.6 fixed supplied by speech part	Yes	2.4	Yes	35.5	SEL	DIP28, SO28	649

Note

1. Bridge Tied Load; Single Ended Load.

HANDSFREE ICs

PRODUCT TYPE	DESCRIPTIO	SUPPLY VOLTAGE (V)	LINE-POWERED	CURRENT CONSUMPTION (mA) TYP.	PD	$G_{v(Tx)}$ (dB)	$G_{v(Rx)}$ (dB)	R_{xout}(1)	SWITCHING RANGE (dB)	PACKAGE	PAGE
TEA1093	handsfree IC combined with power supply	3.6 adjustable	Yes	5.5	Yes	5-25	3-39	BTL	0-52	DIP28, SO28	722
TEA1094	for use with external supply	3.3-12	No	3.1	No	0-31	0-33	SEL	0-52	DIP28, SO28	744
TEA1094A	TEA1094 with power-down	3.3-12	No	3.1	Yes	0-31	0-33	SEL	0-52	DIP24, SO24, SSOP24	744
TEA1095	TEA1094A without loudspeaker drive capability	2.9-12	No	2.7	Yes	0-40	−14 to 26	X	0-52	DIP24, SO24	763

Note

1. Bridge Tied Load; Single Ended Load.

SPEECH / TRANSMISSIONS ICS

PRODUCT TYPE[(1)]	DESCRIPTION	V_{LN} (V) TYP@15 mA	PARALLEL OPERATION	I_{CC} (mA) TYP.	PD	$G_{V(mic)}$ (dB)	MICRO-PHONE MUTE	$G_{v(Rx)}$ (dB)	R_{xout}[(2)]	$\Delta G_{V(AGC)}$ (dB) TYP.	PACKAGE	PAGE
TEA106	low-impedance microphone (magnetic, dynamic)	4.45	No	0.96	Yes	44-60	No	17-39	BTL	–5.9	DIP18	483
TEA1061	high-impedance microphone (electret)	4.45	No	0.96	Yes	30-46	No	17-39	BTL	–5.9	DIP18	483
TEA1066T	TEA1060 & TEA1061 combination in SO20	4.45	No	0.96	Yes	44-60 30-46	No	17-39	BTL	–5.9	SO20	595
TEA1068	all microphone types	4.45	No	0.96	Yes	44-60	No	17-39	BTL	–5.9	DIP18, SO20	632
TEA1067	optimized for parallel phones operation	3.9	Yes	1	Yes	44-52	No	20-45	BTL	–5.9	DIP18; SO20	613
TEA1062	simplified TEA1067 (no PD, SE-receiver)	4.0	Yes	0.9	No	44-52	No	20-31	SEL	–5.8	DIP16, SO16	500
TEA1062A	TEA1062 with inverted MUTE polarity	4.0	Yes	0.9	No	44-52	No	20-31	SEL	–5.8	DIP16, SO16	500
TEA1064A	improved TEA1067 with Dynamic limiter, strong supply point	3.6	Yes	1.3	Yes	44-52	Yes	20-45	BTL	–6.1	DIP20, SO20	521
TEA1065	for DC current regulation	4.45	No	1.14	Yes	30-46	No	20-45	BTL	–5.9	DIP24, SO24	526
TEA1064B	TEA1064A with single-ground reference	3.5	Yes	1.3	Yes	44-52	Yes	20-45	BTL	–6.1	DIP20, SO20	549
PCA1070	fully programmable line interface	4.83@12 mA	Yes	2.3	Yes	30-51	Yes	–25 to 11	BTL	via software	DIP24, SO24	110
TEA1112	EMC optimized, on-chip default settings, LED on-hook/off-hook indication	3.65	Yes	1.15	No	39-52	Yes	19-31	SEL	–5.8	DIP16, SO16	807

PRODUCT TYPE[1]	DESCRIPTION	V_{LN} (V) TYP@15 mA	PARALLEL OPERATION	I_{CC} (mA) TYP.	PD	$G_{V(mic)}$ (dB)	MICRO-PHONE MUTE	$G_{v(Rx)}$ (dB)	R_{xout}[2]	$\Delta G_{V(AGC)}$ (dB) TYP.	PACKAGE	PAGE
TEA1112A	TEA1112 with inverted MUTE polarity	3.65	Yes	1.15	No	39-52	Yes	19-31	SEL	–5.8	DIP16, SO16	807
TEA1113	TEA1112A with Tx Dynamic limiter	4.0	Yes	1.3	No	39-52	Yes	19-31	SEL	–5.8	DIP16, SO16	821
TEA1118	interface for cordless, answering machine and modem	3.65	Yes	1.15	No	0-11	No	19-31	SEL	–5.8	SSOP16, SO14	835
TEA1118A	TEA1118 with DTMF input	3.65	Yes	1.15	No	11	Yes	19-31	SEL	–5.8	SSOP16, SO14	835

Notes

1. Devices are listed as they were initially introduced.
2. BridgeTied Load, Single Ended Load.

MICROCONTROLLER SELECTOR GUIDE FOR IC03

PRODUCT TYPE	ROM	RAM (BYTES)	EEPROM	I/O	OPERATING VOLTAGE (V)	FEATURES	PACKAGE	MAX. SPEED
PCD3344A	2K	224	no	20	1.8 - 6(1)	DTMF	DIL/SO28	16 MHz
PCD3349A	4K	224	no	20	1.8 - 6(1)	DTMF, Melody Output	DIL/SO28	16 MHz
PCD3350A	8K	256	256	34	1.8 - 6(1)	DTMF, Melody Output, Realtime Clock	QFP44	16 MHz
PCD3351A	2K	64	128	20	1.8 - 6(1)	DTMF, Melody Output	DIL/SO28, QFP32	16 MHz
PCA3351C	2K	64	128	20	1.8 - 6(1)	As PCD3351A, 0-50 °C, VPOR = 2.0 V, ±300 mV	DIL/SO28, QFP32	16 MHz
PCD3352A	4K	128	128	20	1.8 - 6(1)	DTMF, Melody Output	DIL/SO28, QFP32	16 MHz
PCA3352C	4K	128	128	20	1.8 - 6(1)	As PCD3352A, 0-50 °C, VPOR = 2.0 V, ±300 mV	DIL/SO28, QFP32	16 MHz
PCD3353A	6K	128	128	20	1.8 - 6(1)	DTMF, Melody Output	DIL/SO28, QFP32	16 MHz
PCA3353C	6K	128	128	20	1.8 - 6(1)	As PCD3353A, 0-50 °C, VPOR = 2.0 V, ±300 mV	DIL/SO-28, QFP32	16 MHz
PCD3354A	8K	256	256	36	1.8 - 6(1)	DTMF, Melody Output	QFP44	16 MHz
PCA3354C	8K	256	256	36	1.8 - 6(1)	As PCD3354A, 0-50 °C, VPOR = 2.0 V, ±300 mV	QFP44	16 MHz
PCD3355A	8K	128	128	20	1.8 - 6(1)	DTMF, Melody Output	DIL/SO28, QFP32	16 MHz
PCD3356A	8K	128	128	20	1.8 - 6(1)	DTMF, Melody Output	DIL/SO28, QFP32	16 MHz
PCD3357A	6K	128	128	20	1.8 - 6(1)	DTMF, Melody Output	DIL/SO28, QFP32	16 MHz
PCD3359A	2K	64	128	20	1.8 - 6(1)	As PCD3351A + keyboard interrupt. Tone disabled during ringing	DIL/SO28, QFP32	16 MHz
PCD3755X	8K OTP	128	128	20	1.8 - 6(1)	OTP for 3351A/52A/53A/55A	DIL/SO28, QFP32	16 MHz
PCD3756X	8K OTP	128	128	20	1.8 - 6(1)	OTP for 3356A/57A/59A	DIL/SO28, QFP32	16 MHz

PRODUCT TYPE	ROM	RAM (BYTES)	EEPROM	I/O	OPERATING VOLTAGE (V)	FEATURES	PACKAGE	MAX. SPEED
PCF84C12A	1K	64	no	13	2.5 - 5.5	use external generator	DIL/SO20	16 MHz
PCF84C22A	2K	64	no	13	2.5 - 5.5	use external generator	DIL/SO20	16 MHz
PCF84C42A	4K	64	no	13	2.5 - 5.5	use external generator	DIL/SO20	16 MHz

Note

1. DTMF tone output and/or EEPROM erase/write from 2.5 V.

LCD SEGMENT DRIVERS

Device	Drive capability, Number of segments at a Multiplex rate (Duty)						Logic voltage range	LCD voltage V_{op} max.	Typ. system current (μA)	On-chip bias voltage generator	Interface	Special futures	Packages		Gold Bumps	Available
	1 : 1	1 : 2	1 : 3	1 : 4	1 : 8	1 : 16										
PCF8566	24	48	72	96			2.5 to 6.0	6	15	yes	I²C-bus	cascadable with PCF8566/76	DIP40	VSO40		now
PCF8576 (C)	40	80	120	160			2.0 to 9.0 (6)	9 (6)	25	yes	I²C-bus	cascadable with PCF8566/76	VSO56	LQFP64	on FFC	now
PCF8578					256	384	2.5 to 6.0	9	250(1)	no	I²C-bus	easy blinking, scratch pad RAM	VSO56	LQFP64	on FFC	now

Note

1. Including external bias generator.

GRAPHIC LCD DRIVERS

Device	Rows	Columns	Matrix size	Logic voltage range	LCD voltage V_{op} max.	Typ. system current (μA)	On-chip bias voltage generator	On-chip bias voltage multiplier	Interface	Special futures	Packages		Gold Bumps	Available
PCF8578	8, 16, 24, 32	32, 24, 16, 8	any	2.5 to 6.0	9	250(1)	no	no	I²C-bus	for mux 1 : 8, 16, 24, 32	VSO56	LQFP64	on FFC	now
PCF8579		40	any	2.5 to 6.0	9	9	-	no	I²C-bus	for mux 1 : 8, 16, 24, 32	VSO56	LQFP64	on FFC	now

Note

1. Including external bias generator.

DOT-MATRIX CHARACTER LCD DRIVERS

Device	Rows	Columns	Matrix size	Logic voltage range	LCD voltage V_{op} max.	Typ. system current (μA)	On-chip bias voltage generator	On-chip bias voltage multiplier	Interface	Special futures	Packages		Gold Bumps	Available
PCF2114; PCF2116	16/32	60	1/2 line by 24; 2/4 line by 12	2.5 to 6.0	9	150(1) 500(2)	yes	yes	I^2C-bus and parallel 4/8-bit	on-chip voltage multiplier	LQFP128	Xtal on FFC	bumps on FFC	now
PCF2104	16/32	60	1/2 line by 24; 2/4 line by 12	2.5 to 6.0	9	150(1)	yes	yes	I^2C-bus and parallel 4/8-bit			Xtal on FFC	bumps on FFC	now

Notes

1. External V_{LCD}, on-chip bias generator.
2. On-chip V_{LCD}, on-chip bias generator.

TYPE NUMBER	V_{CEO} (V)	I_C (mA)	P_{tot} (mW)	h_{FE}		$f_{T(MIN)}$ typ. (MHz)	PAGE
				min.	max.		
Leaded transistors							
NPN							
BC337	45	500	800	100	600	100	59
BC337A	60	500	800	100	600	100	59
BC338	25	500	800	100	600	100	59
BC546	65	100	500	110	450	100	60
BC547	45	100	500	110	800	100	60
BC548	30	100	500	110	800	100	60
MPSA42	300	500	625	40	–	50	87
MPSA43	200	500	625	40	–	50	87
2N5550	140	600	500	60	250	100	870
2N5551	160	600	500	80	250	100	870
PNP							
BC327	45	500	800	100	600	80	58
BC327A	60	500	800	100	400	80	58
BC328	25	500	800	100	600	80	58
BC556	65	100	500	125	800	100	61
BC557	45	100	500	125	800	100	61
BC558	30	100	500	125	800	100	61
MPSA92	300	500	625	25	–	50	89
MPSA93	200	500	625	25	–	50	89
2N5400	120	600	500	40	180	100	869
2N5401	150	600	500	60	240	100	869
Surface mounted transistors							
NPN							
BC846	65	100	250	110	450	100	62
BC847	45	100	250	110	800	100	62
BC848	30	100	250	110	800	100	62
PZTA42	300	500	1500	40	–	50	458
PZTA43	200	500	1500	40	–	50	458
PMBTA42	300	500	250	40	–	50	453
PMBTA43	200	500	250	40	–	50	453
PZTA44	400	300	1500	50	200	20	461
PZTA45	350	300	1500	50	200	20	461

PNP							
BC856	65	100	250	125	800	100	63
BC857	45	100	250	125	800	100	63
BC858	30	100	250	125	800	100	63
PZTA92	300	500	1500	40	–	50	464
PZTA93	200	500	1500	40	–	50	464
PMBTA92	300	500	250	40	–	50	456
PMBTA93	200	500	250	40	–	50	456

N-CHANNEL VERTICAL D-MOS-FETS FOR SWITCHING

Total power dissipation (P_{tot}) measured at T_{amb} = 25 °C, unless otherwise specified.

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS107	TO-92 var.	200	150	830	0.8 to 2.4	20	28	20	2.6	10/20	65
BS107A	TO-92 var.	200	250	600	1 to 3	4.5	6.4	250	10	5/15	66
BS108	TO-92 var.	200	250	1000	0.4 to 1.8	5	8	100	2.8	10/30	67
BS170	TO-92 var.	60	500	830	0.8 to 3	2.5	5	200	10	10/10	68
BSN10	TO-92 var.	50	175	830	0.4 to 1.8	12	20	100	5	5/10	69
BSN10A	TO-92 var.	50	175	830	0.4 to 1.8	12	20	100	5	5/10	69
BSN20	SOT23	50	100	250	0.4 to 1.8	14	20	100	5	5/10	70
BSN254	TO-92 var.	250	300	1000	0.8 to 2	4.5	10	20	2.4	10/30	71
BSN254A	TO-92 var.	250	300	1000	0.8 to 2	4.5	10	20	2.4	10/30	71
BSN274	TO-92 var.	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	72
BSN274A	TO-92 var.	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	72
BSN304	TO-92 var.	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	73
BSN304A	TO-92 var.	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	73
BSP126	SOT223	250	350	1500	0.8 to 2	5	10	20	2.4	10/30	74
BSP130	SOT223	300	300	1500	0.8 to 2	6.7	8	250	10	10/30	75
BSP145	SOT223	450	250	1500	2 to 4	10	14	100	10	10/100	76
BSS89	TO-92 var.	200	300	1000	0.8 to 2.8	4.5	6	400	10	5/15	81
BST74A	TO-92 var.	200	250	1000	0.8 to 2.8	6	12	250	10	10/25	84
BST124	TO-126	250	450	6000	0.6 to 1.4	–	12	250	5	10/30	83
PMBF107	SOT23	200	100	250	0.8 to 2.4	20	28	20	2.6	10/20	451
PMBF170	SOT23	60	250	300	0.8 to 3	2.5	5	200	10	10/15	452
VN2406L	TO-92 var.	240	210	1000	0.8 to 2	–	6	500	10	10/30	868
2N7000	TO-92 var.	60	280	830	0.8 to 3	3.5	5.3	75	4.5	10/10	871
2N7002	SOT23	60	180	300	0.8 to 3	3.5	5.3	75	4.5	10/15	872

P-CHANNEL VERTICAL D-MOS-FETS FOR SWITCHING

P_{tot} measured at T_{amb} = 25 °C.

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	R_{DSon} (Ω)		at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
						typ.	max.				
BSP92	SOT223	240	180	1500	0.8 to 2	10	20	180	10	10/30	81
BSP225	SOT223	250	225	1500	0.8 to 2.8	10	15	200	10	10/30	77
BSP254	TO-92 var.	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	78
BSP254A	TO-92 var.	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	78
BSP304	TO-92 var.	300	170	1000	1.7 to 2.55	–	17	170	10	10/30	79
BSS92	TO-92 var.	200	150	1000	0.8 to 2.8	10	20	100	10	5/20	82

GENERAL

Page

Quality 28

Pro electron type numbering 29

Type numbering of 8051 and 90C microcontroller derivatives 33

Type numbering of 8048 microcontroller derivatives 34

Type numbering of HCMOS integrated circuits 35

Type numbering of linear and memory devices 36

Rating systems 37

Handling MOS devices 39

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A	Germanium or other material with a band gap of 0.6 to 1 eV
B	Silicon or other material with a band gap of 1 to 1.3 eV
C	Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more
R	Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A	Diode; signal, low power
B	Diode; variable capacitance
C	Transistor; low power, audio frequency
D	Transistor; power, audio frequency
E	Diode; tunnel
F	Transistor; low power, high frequency
G	multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under “Serial number/special third letter”
H	Diode; magnetic sensitive
L	Transistor; power, high frequency
N	Photocoupler
P	Radiation detector; e.g. high sensitivity photo-transistor; with special third letter
Q	Radiation generator; e.g. LED, laser; with special third letter
R	Control or switching device; e.g. thyristor, low power; with special third letter
S	Transistor; low power, switching
T	Control and switching device; e.g. thyristor, power; with special third letter
U	Transistor; power, switching
W	Surface acoustic wave device
X	Diode; multiplier, e.g. varactor, step recovery
Y	Diode; rectifying, booster
Z	Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A	For triacs, after second letter ‘R’ or ‘T’
F	For emitters and receivers in fibre-optic communication, after second letter ‘G’, ‘P’ or ‘Q’. When the second letter is ‘G’, the first letter should be defined in accordance with the material of the main optical device.
L	For lasers in non-fibre-optic applications, after second letter ‘G’ or ‘Q’. When the second letter is ‘G’, the first letter should be defined in accordance with the material of the main optical device.
O	For opto-triacs, after second letter ‘R’
T	For 3-state bicolour LEDs, after second letter ‘Q’
W	For transient voltage suppressor diodes, after second letter ‘Z’.

EXAMPLES OF BASIC TYPE NUMBERS

AA112	Germanium, low power signal diode (consumer type)
ACY32	Germanium, low power AF transistor (industrial type)
BD232	Silicon, power AF transistor (consumer type)
CQY17	GaAs, light-emitting diode (industrial type)
RPY84	CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter ‘R’ indicates reverse polarity and the letter ‘W’ indicates a surface mounted device (SMD).

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(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A	1%
B	2%
C	5%
D	10%
E	20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S	Solitary digital circuits
T	Analog circuits
U	Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA	Microcomputer or central processing unit
MB	Slice processor (functional slice of microprocessor)

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(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD	Related memories
ME	Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH	Hybrid circuits
NL	Logic circuits
NM	Memories
NS	Analog signal processing using switched capacitors
NT	Analog signal processing using charge-transfer devices
NX	Imaging devices
NY	Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A	temperature range not specified below
B	0 to + 70 °C
C	−55 to +125 °C
D	−25 to + 70 °C
E	−25 to + 85 °C
F	−40 to + 85 °C
G	−55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C	Cylindrical
D	Ceramic dual in-line (CERDIL, CERDIP)
F	Flat pack (two leads)
G	Flat pack (four leads)
H	Quad flat pack (QFP)
L	Chip on tape (foil)
P	Plastic dual in-line (DIL)
Q	Quad in-line (QUIL)
T	Mini pack (SOL, SO, VSO)
U	Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C	Cylindrical
D	Dual in-line (DIL)
E	Power DIL (with external heatsink)
F	Flat pack (leads on two sides)
G	Flat pack (leads on four sides)
H	Quad flat pack (QFP)
K	Diamond (TO-3 family)
M	Multiple in-line (except dual, triple and quad)
Q	Quad in-line (QUIL)
R	Power QUIL (with external heatsink)
S	Single in-line (SIL)
T	Triple in-line
W	Leaded chip carrier (LCC)
X	Leadless chip carrier (LLCC)
Y	Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C	Metal-ceramic
G	Glass-ceramic
M	Metal
P	Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

TYPE NUMBERING OF 8051 AND 90C MICROCONTROLLER DERIVATIVES

P N X C L DDD F T P /RRR

P	Philips
N	8 for 8051 9 for 90C
X	0 for ROM-less 3 for ROM 5 for bondout 7 for EPROM 9 for FEE
C	CMOS
L E	low power, low voltage low electromagnetic emission
DDD	derivative indication

ROM code identification

Package code

A	plastic leaded chip carrier (PLCC)
B	quad flat pack (QFP)
F	ceramic dual in-line (CERDIP) with window
L	leadless ceramic chip carrier (LCCC) with window
N	ceramic pin grid array (CPGA)
P	plastic dual in-line (DIL)
Q	quad ceramic flat pack (QCERPA)
T	small outline (SO), small outline large (SOL) or very small outline (VSO)
Z	metal-ceramic dual in-line piggyback (CPB)

Temperature range

A	other than specified below
B	0 to +70 °C
C	–55 to +125 °C
D	–25 to +70 °C
E	–25 to +85 °C
F	–40 to +85 °C
G	–55 to +85 °C
H	–40 to +125 °C

Frequency range

A	other than specified below
B	3.5 to 12 MHz
C	1.2 to 12 MHz
D	0.5 to 12 MHz
E	3.5 to 16 MHz
F	1.2 to 16 MHz
G	1.2 to 20 MHz
H	DC to 20 MHz

TYPE NUMBERING OF 8048 MICROCONTROLLER DERIVATIVES

PC F 84C270 P
MA B 8441 P

Package code

B	metal-ceramic dual in-line piggyback (CPB)
D	ceramic dual in-line (CERDIP)
H	quad flat pack (QFP)
P	plastic dual in-line (DIL)
T	small outline (SO), small outline, large (SOL) or very small outline (VSO)
WP	plastic leaded chip carrier (PLCC)

Generic type number

Temperature range

A	other than specified below
B	0 to +70 °C
D	–25 to +70 °C
F	–40 to +85 °C
H	–40 to +125 °C
V	–40 to +110 °C

Technology

PC	CMOS
MA	NMOS

TYPE NUMBERING OF HCMOS INTEGRATED CIRCUITS

Example: 74 HC XXXXX XX

Complete type number; standard temperature range

Package Code:
N = Plastic dual in-line
D = SO package
DB = SSOP type 11
NB = Plastic dual in-line with burn-in

Device number (up to 5 digits)

HC = CMOS input switching levels, supply voltage range 2 V to 6 V, fully buffered

HCT = TTL input switching levels, supply voltage range 4.5 V to 5.5 V, fully buffered

74 = Standard temperature range: −40 °C to + 125 °C

ORDERING

When ordering, please state:
- the quantity required;
- the package code (N = plastic DIL, D = plastic SO mini-pack, DB = SSOP type 11);
- screening class (B) if burn-in option is required (only applicable for NB package).

TYPE NUMBERING OF LINEAR AND MEMORY DEVICES

NE 567 N
SA 604A D

Package code

A	plastic leaded chip carrier (PLCC)
D	small outline (SO) or small outline large (SOL)
DK	shrink small outline (SSOP)
F	ceramic dual in-line (CERDIP)
N	plastic dual in-line (DIL)
N3	plastic dual in-line (DIL) 300 mil-wide

Generic type number

Linear ICs family and temperature range prefix

MC	0 to +70 °C
N	0 to +70 °C
NE	0 to +70 °C
S	–55 to +125 °C
SE	–55 to +125 °C
SA	–40 to +85 °C

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

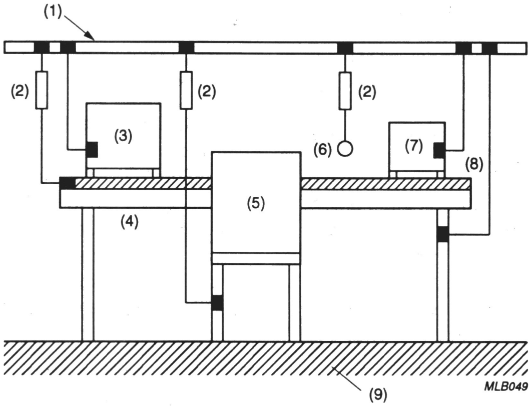
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



Earthing rail.
Resistor (500 kΩ ± 10%, 0.5 W).
Ionizer.
Work bench.
Chair.
Wrist strap.
Electrical equipment.
Conductive surface/antistatic sheet.

Fig.1 Protected work station.

APPLICATION NOTES SUMMARIES

APPLICATION NOTE SUMMARIES

The Application Handbook for Wired Telecom Systems (IC03b, ordering code 9397 750 00811) is largely a compilation of already-published laboratory reports from several Philips Application Laboratories. It contains extensive practical information for those designing-in Philips Semiconductors ICs into a variety of telecom sets - from the simple to the most advanced featurephone. It supplements the latest information given in product data sheets and in the Philips Semiconductors data handbook 'Semiconductors for Wired Telecom Systems' (IC03a).

The book can be obtained by filling in and returning the fax back form..

Below are summaries of application notes available for wired telecom systems. Application notes marked with an * are published in the Application Handbook for Wired Telecom Systems (IC03b). For all other application notes, please contact Philips Semiconductors.

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* AN94016

Basics of PCA1070: a programmable analogue CMOS transmission IC (PACT)

Details: 102 pages, March 1994

The PCA1070 opens the possibility to manufacture a programmable transmission part for use in the telephone line interface of electronic devices such as electronic telephone sets and feature phones, cordless phones, answering machines, modems and fax equipment.

The PCA1070 is a CMOS integrated circuit performing speech and line interface functions. It needs a minimum number of external components. The transmission parameters are programmable via the I^2C-bus. This makes the IC adaptable to nearly all country requirements in the world, and to a various range of speech transducers, without changing the (few) external components of the basic application. With the PCA1070 the number of printed circuit board versions and the number of components is minimised. This reduces the costs of logistics and manufacturing operation extensively. For some countries a 12 kHz or 16 kHz tax pulse filter has to complete the design.

This report gives a detailed description of the PCA1070 and its basic application in electronic telephone sets. Also EMC aspects, protection and tax pulse filtering are discussed. Furthermore an application example of PCA1070 together with a pre-programmed µC PCD3353A/008 is given and some measurement results of this application are shown.

AN94017

Tax pulse filters at 12 and 16 kHz for the PCA1070

Details: 13 pages, March 1994

Tax pulse filters for 12 and 16 kHz metering systems were designed for the PCA1070. With these filters, the BRL of all West-European countries can be met by adaptation of the programmable set impedance, if needed. The range of the programmable sidetone impedance was adequate for the test method used. For the filter design an exchange is possible between receive gain of the PCA1070, the filter Q-factor and spread of filter components. For Switzerland with 12 kHz/10 Vrms tax pulse the maximum receive gain is +6 dB for a filter with a Q of 15,3% inductors and 5% capacitors. For Germany with 16 kHz/9.8 Vrms the maximum receive gain is +10 dB for a Q-factor of 20,3% inductors and 5% capacitors.

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AN94021

French current-regulation circuit for the PCA1070

Details: 17 pages, March 1994

This report contains a detailed description of the circuit blocks of the TEA1112 and the TEA1112A. Two application examples of the TEA1112 are given. The report handles the consecutive steps to design or to adjust the basic application with these ICs The EMC behaviour of an evaluation board with the TEA1112 or the TEA1112A is included.

The General notation in this report for both ICs, TEA1112 and TEA1112A, is: TEA1112/A.

*** CTT/AN95083**

TEA1095 voice-switched speaker-phone IC

Details: 42 pages, September 1995

The TEA1095 is a high-performance, low-power consumption voice switched speakerphone IC designed for integration of a handsfree function in terminal environments.

A detailed description of the IC, advises on the adjustments and a worked-out application example are contained in this report.

EIE/AN91001

Workbench EMC evaluation method

Details: 18 pages, December 1991

With the proposed EMC workbench evaluation method small application boards, printed wiring boards containing one or more ICs can be verified on basic EMC parameters such as Radio Frequency (RF-) emission and immunity over the frequency range from 150 kHz to 230 MHz, or even 1 Ghz.

This EMC evaluation method can be used in a qualification procedure to select between new electronic circuit (systems) implementations from various supplies or as a design tool when developing new products based on modular circuit blocks.

EIE94006

A comparison of test signals for testing the RF immunity with burst-mode disturbances

Details: 18 pages, November 1994

It is expected that RF immunity standards for all electronic equipment will soon be extended with requirements on GSM and DECT frequencies. As the existing test methods use sine wave amplitude modulated RF signals, it is interesting to know the relation to the newly proposed block pulse modulation.

For the judgement of self-pollution, e.g. in a DECT base station, it is also required to look at the psophometrically weighted noise that is added as noise to the line. This report presents a relation between the results as obtained with various test signals.

ESG8801

An evaluation method to characterize the EMC performance of PCBs containing ICs

Details: 44 pages, July 1988

The evaluation of the ElectroMagnetic Compatibility (EMC) performance of Printed Circuit Boards (PCBs) is the most essential part to obtain proper EMC performance of the entire product from the very start of development. These methods can even be applied to evaluate the performance of Integrated Circuits (ICs) either as single device or implemented in a typical application.

It is tried to establish an evaluation method without ambiguity, which is comprehensive and economic in three senses:

- The initial costs of the verification tools

- The ease to perform the measurements
- The benefits: reduction of development throughput-time and re-design.

From the theory and practical experience, based on this EMC-performance evaluation procedure, it can be concluded that only a small number of tests are necessary to determine whether or not a PCB fulfils certain requirements.

ESG89001

Electromagnetic compatibility and printed circuit board (PCB) constraints

Details: 30 pages, April 1989

Today's Printed Circuit Board designs often fail to comply with Electro Magnetic Emission and immunity requirements applicable for complete products. Herewith, guidelines are given which will enable the designer to take those precautions necessary to tailor PCBs, that they will fulfil those requirements.

*** ETT/AN8903**

Galvanic separation of the I^{2}C-bus

Details: 11 pages, March 1989

In some telephone applications, there is a need for galvanic separation of the I^{2}C-bus, for example if I^{2}C devices coupled to the bus are not fed from the same internal power supply. In this note, a technical solution is given where the I^{2}C-bus specification can be met. As galvanic separation device, an optocoupler is used.

*** ETT/AN89008**

Application of the speech-transmission circuit TEA1062

Details: 24 pages, October 1989

The TEA106x family consists of a range of bipolar integrated circuits performing all speech and line interface functions required in fully electronic telephone sets. The TEA1060 family designers guide (lit.1) provides information on most of the members of the TEA106x. The TEA1062 is not described in this guide. Detailed information about this circuit can be found in the data sheet (lit.2).

The TEA1062 is a low-voltage speech-transmission IC able to operate down to a dc line voltage of 1.6 V to facilitate the use of more telephone sets in parallel. The TEA1062 has a modified performance and less features compared to the TEA1067.

In this report differences between the TEA1062 and the TEA1067 as described in lit.1 are elucidated. When applying the TEA1062 this report should be used in combination with the designers guide.

The figures given in this report all refer to the TEA1062. The TEA1062 is described in this report with respect to the basic application circuit shown in fig.1 (lit.3)

*** ETT/AN90005**

The TEA1064A with complex set impedance and complex line termination

Details: 8 pages, February 1990

More and more PTTs require a complex set impedance for telephone sets. It can be expected that the sending frequency curves will be measured with a complex line termination instead of 600 Ω. The German PTT is the first one that actually changed over from 600 Ω to a complex termination. Furthermore they require a better accuracy of the complex set impedance (balance return loss up to 18 dB). To prevent high frequency roll-off in sending direction with the TEA1064A in such a case, the application hint mentioned in this report should be considered.

*** ETT/AN90017**

Software controlled ringer for German market

Details: 32 pages, July 1990

In sets with the listening-in feature, it is possible to generate a ringing signal via the loudspeaker instead of using a separate mechanical bell or PXE. By using the Philips components TEA1064A (speech-transmission), TEA1085 (listening-in), PCD3312 (DTMF-generator), PCD3346 (micro-controller plus EEPROM) and a power converter it is possible to do this software controlled such that both the German TEL02 ringer requirements and the speech-transmission requirements are fulfilled.

*** ETT/AN91010**

User's manual PR4535x DEMO board with TEA1083A-TEA1064 call progress monitoring application.

Details: 25 pages, June 1991

The printed circuit board PR4535x demonstrates the TEA1083A call progress monitoring circuit in combination with the TEA1064A transmission IC. The TEA1083A may be replaced by the TEA1083.

This report describes the printed circuit board and gives some application information. However, it is not intended to be an application report. Refer to the literature given in chapter 7 for application details.

*** ETT/AN91012**

User's Manual - PR4516X; demo board with the TEA1085A-TEA1064A listening-in application

Details: 29 pages, July 1991

The printed circuit board PR4516x demonstrates the TEA1085A listening-in IC in combination with the TEA1064A as transmission IC. This report describes the printed circuit board and gives some application information. However it is not intended to be an application report. Refer to the literature given in chapter 7 for application details.

First version: ETT/AN90006, May 1990. Updates: ETT/AN91012, July 1991: TEA1085 replaced by the TEA1085A. Demonstration board PR4516x is delivered with the TEA1085A. The TEA1085A may be replaced by the TEA1085.

ETT/AN91013

Micro-controller PCF84C12/xxx - for PCD4440 scrambler/descrambler applications

Details: 18 pages, May 1991

An analogue voice scrambler device, the PCD4440 needs to be driven by a controller circuit via the serial inputs SDA (Serial Data), and SCL (Serial Clock), to switch the device to the correct split frequencies in the time domain. Also other features like crystal oscillator frequency generation, initialisation, transparent mode and mute mode switching can be done via the serial bus, the I^2C-bus.

In a system where no controller function is needed for other tasks, this micro-controller can provide these functions. It includes different feature setting via keyboard inputs, while the controller can be switched to the AUTOMATIC or BCD modes so that it can operate without a keyboard as well.

ETT/AN91014

Demonstration board PR45284 for PCD4440 scrambler and NE577 compander

Details: 16 pages, May 1991

The PCD4440 scrambler/descrambler IC has been developed for use in cordless telephones for the purpose of scrambling and descrambling the analogue speech signals which are transmitted by a radio link between handsets and base units. This report describes a printed circuit board designed to exercise the PCD4440, which in combination with the NE577 compander IC provides an excellent vehicle for the purposes of demonstration and measurement. A micro-controller is used to control the PCD4440 via an I^{2}C-Bus.

*** ETT/AN91016**

TEA1085A/TEA1085 - a listening-in facility for electronic telephone sets

Details: 64 pages, September 1991

The TEA1085A and the TEA1085 are designed for use in line powered telephone sets. Besides the listening-in function, they incorporate an effective dynamic limiter and a Larsen Level Limiter to reduce annoying howling effects.

They have to be combined with a transmission IC of the TEA1060 family. Nearly all line current can be utilised for powering the loudspeaker without affecting the transmission characteristics. This report describes the TEA1085A/TEA1085 and an application with the TEA1064A.

*** ETT/AN92010**

User's manual OM4723 demo board: PCD3330-1/TEA1067/TEA1083A feature-phone application

Details: 37 pages, July 1992

This feature-phone board OM4723 is designed to demonstrate the PCD3330-1: a mixed-mode multi-standard repertory dialler/ringer with EEPROM. The on-hook dialling feature is realised with the TEA1083A call progress monitoring IC.

The main components on the board are:

- Multi-standard repertory dialler/ringer IC-PCD3330-1
- Versatile Speech/Transmission IC-TEA1067
- Call progress monitoring IC-TEA1083A
- Line current interrupter DMOST-BSP254A.

ETT/AN92011

Software specification to control the PCA1070 PACT-IC (PCD3353A/008)

Details: 38 pages, January 1993

This report gives the objective target specification of demonstration and test software to control the PCA1070 which is a Programmable Analogue CMOS Transmission (PACT) circuit, with the PCD3353A micro-computer.

The PCD3353A/008 is a member of the PCD3353A micro-computer family, special developed for telephone applications. This PCD3353A micro-controller family has on-board DTMF generator, EEPROM and a special ringer output and is fully able to control the PCA1070 via its software I^{2}C-bus.

The PCA1070/PCD3353A circuits combination performs the following functions:

- Pulse and DTMF dialling
- Redial and repertory dial stored in EEPROM
- PCA1070 control
- PCA1070 variables stored in EEPROM
- PCA1070 variable programmable via I^{2}C-bus and Key-board
- Dialling options programmable via keyboard stored in EEPROM

- Ringer functions incorporated 3-tone, 4-speeds and 4 volumes
- Display.

The program will firstly be used for evaluation of the first samples of this PCA1070 in application with the PCD3353A micro-computer.

To use it for demonstration purposes at customers and to complete the dynamic evaluation a mask programmed version (PCD3353A/008) is made.

ETT/AN93010

User's Manual of the OM4737 evaluation kit for the PCA1070

Details: 8 pages, July 1993

This report describes the OM4737 evaluation kit. The kit is intended to be used for laboratory evaluation of the PCA1070 Multi-standard Programmable Analogue CMOS Transmission IC (PACT).

The kit consists of:

- PCA1070 evaluation board
- I^{2}C-bus interface board for use with an IBM-compatible PC
- Evaluation software with the I^{2}C-bus control program (on 3.5" diskette).

* ETT/AN93015 (SUPERSEDES REPORT NOVEMBER 1993 WITH SAME NUMBER)

Application of the TEA1093 hands-free circuit

Details: 67 pages, 29 November 1993 (revised 30 November 1995)

The TEA1093 is a hands-free telephone IC, that can be used in combination with a transmission IC of the TEA106x, TEA111x family or the PCA1070, in line powered telephone sets and in mains supplied sets, to extend the function of the transmission IC with a handsfree function. It provides a half duplex connection. The decision logic eliminates back ground noise from speech signals. If both sides are quiet the TEA1093 goes into idle mode to avoid the 'line dead' phenomenon.

This report contains a number of application examples that can be taken as starting point for new designs and application hints that can be used during design phase.

* ETT/AN93017

User's manual for the OM4736 demo kit: a multi-standard telephone set with PCA1070 and PCD3353A/008

Details: 34 pages, December 1993

The feature-phone kit OM4736 is designed to demonstrate the programmable transmission IC PCA1070 with the help of the PCD3353A/008 pre-programmed micro-computer.

The PCA1070 is a Multi-standard Programmable Analogue CMOS Transmission (PACT) integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It needs a minimum number of external components. The transmission parameters are programmable via the I^{2}C-bus, which makes the IC suitable for nearly all countries in the world without changing the (few) external components.

The PCD3353A/008 has three functions:

- Control of the normal feature phone functions such as pulse/tone dialling, redial/repertory dialling and software controlled ringer function
- Setting of the transmission parameters of the PCA1070, which are stored in the on-chip EEPROM, via the I^{2}C-bus

- Setting of the dialler and the ringer parameters which are also stored in the EEPROM
- Changing of all the programmable parameters via keyboard to show the flexibility of the total application.

All dialled or programmed numbers, programmed or stored parameters for dialling ringer and PCA1070 control, are shown on an LCD-Display. This report gives a brief description of the application and gives a guide-line for operation of the DEMO kit.

*** ETT/AN94001**

User manual for OM4750: Demonstration board TEA1093 and TEA1094

Details: 16 pages, April 1996

This report describes the TEA1093/TEA1094 demonstration board. The board demonstrates the performance of the TEA1093 and TEA1094 handsfree circuit in conjunction with a TEA1062 or TEA1067 speech transmission circuit. It provides handset, handsfree and listening-in operation. The difference between the TEA1093 and TEA1094 is that the TEA1093 is line powered while the TEA1094 is externally powered. An external power supply is useful, for instance, in answering machines. It has the advantage that a high loudspeaker output power can be realised.

*** ETT/AN94004**

Application of the TEA1094 hands-free circuit

Details: 49 pages, March 1994

A detailed description of the TEA1094 is given. In conjunction with a member of the TEA106x family transmission circuits, it offers a hands-free function. It incorporates a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on the transmit and the receive channel. A cookbook gives the general application steps and also several application examples are given including listening-in, cordless-base and answering machine.

*** ETT/UM95004.0**

OM4775 user manual - basic phone demonstration board OM4775. UBA1702/A, TEA1062/1064B and PCD3755A

Details: 25 pages, November 1995

The OM4775 is a demonstration board of a basic phone realised with the UBA1702/A line interrupter driver and ringer circuit, the TEA1062/1064B transmission circuit and the PCD3755A micro-controller.

The basic phone is in fact a general application with different demonstration possibilities with respect to interrupter/ringer and transmission ICs. It is not made to fulfil specific country requirements, however adaptation is possible to a certain extent and is made easy by mounting concerning components on sockets or solder pins. These components are underlined in the text of chapter 2 and 4.

The OM4775 contains a handset with microphone and earpiece and a base with the hardware including a piezo-buzzer for ringing and a keyboard. The OM4775 is delivered with the UBA1702, BSP254A, TEA1064B and PCD3755A. The UBA1702 and BSP254A can be replaced by the UBA1702A and MPSA92, the TEA1064B by the TEA1062.

ETT/UM95011.0

OM4776 Evaluation board for TEA1112(A) and TEA1113

Details: 17 pages, October 1995

This document describes the evaluation kit OM4776. This kit is intended to be used for laboratory evaluation of the TEA111x.

The TEA1112 and the TEA1112A are speech transmission ICs for application in electronic telephone sets. They are added to the range of transmission circuits of the TEA106x-family. Besides the required basic interface functions between microphone capsule, earpiece, telephone line and dialler circuit (DTMF and pulse dialling) they offer the user a Hook-Status indicator function (LED output) and a transmit mute function (MMUTE). The EMC behaviour is improved with respect to the TEA106x Ics.

The TEA112A differs from the TEA1112 by the inverted MUTE and the MMUTE input (Ref 1). The TEA1113 differs from the TEA1112 by the inverted MUTE and by the use of a dynamic limiter in combination with MMUTE (Ref. 2).

ETT/UM95013.0

OM4766 evaluation kit for TEA1069N speech/dialler/ringer

Details: 25 pages, February 1996

This document describes the evaluation kit OM4766. This kit is intended to be used for laboratory evaluation of Speech/Dialler/Ringer IC TEA1069N.

The purpose of the evaluation kit is to evaluate and demonstrate the basic features of the TEA1069N one-chip telephone IC. The board behaves as a normal telephone. Using the handset and the keyboard telephone calls can be made, and incoming calls can be accepted. In order to accommodate easy evaluation of the additional features of the TEA1069N it is possible to access the different pins of this chip.

ETT/UM96003.0 (ETT/AN89006 REVISION)

OM4729 basic application board for the TEA1062 and TEA1062A

Details: 25 pages, February 1996

This document describes the evaluation kit OM4729 (formerly known as CAB3422) This kit is intended to be used for laboratory evaluation of the TEA1062(A).

The TEA1062 and TEA1062A are speech transmission ICs for application in electronic telephone sets. They are part of the range of transmission circuits of the TEA106x-family.

The TEA1062A differs from the TEA1062 by the inverted MUTE input (Ref. 1).

*** ETT/UM96006.0**

OM4784 user manual - System board of TEA1069N, TEA1093 and UBA1702/A

Details: 33 pages, March 1996

This document describes the system board OM4784. This board is intended to be used for laboratory evaluation of the Speech/Dialler/Ringer IC TEA1069N in combination with the TEA1093 and the UBA1702/A.

The purpose of the system board is to evaluate and demonstrate the features of the TEA1069N one-chip telephone IC in combination with the TEA1093 (handsfree) and the UBA1702A (line-interface). The board is a feature phone with Music On Hold, keytone, parallel set detection and handsfree.

ETT8503

The coupling network between the PCD3311/12 DTMF generator and the TEA1060/61 transmission circuit

Details: 17 pages, March 1985

The DTMF generator PCD3311/12 needs a transmission circuit as an interface to the telephone line. The report describes the design considerations for a fixed passive coupling network between the generator and a TEA1060/61. The worst case variation of the DTMF voltage on the line will, according to the specifications of both devices, exceed the

CEPT recommendation. However, by using statistical methods it can be proved that 99% of the PCD3311/12-TEA1060/61 combinations will meet the recommendation.

*** ETT8612**

Application of the PCD3310 bilingual dialler in electronic telephone sets

Details: 27 pages, October 1986

The PCD3310 is a CMOS integrated dialling circuit with dual-standard dialling for either pulse dialling (PD) or dual tone multi frequency (DTMF) dialling with last-number redial.

This report gives a description of the circuit, the dialling procedures and the subscriber set architectures of the PCD3310. Also the Electro Magnetic immunity compared with other dialling circuits is given.

*** ETT8707**

Application of the TEA1081 - a supply IC for peripheral circuits in electronic telephone sets

Details: 45 pages, 15-9-87

TheTEA1081 is intended for application in electronic telephone sets which are powered from the telephone line. This circuit performs the interface function between telephone line and supply line for peripheral circuits. In combination with a transmission circuit of the TEA1060 family it improves the power supply capabilities of the set depending on the available line current.

The TEA1081 is a successor of the TEA1080, major differences with the TEA1080 are the improved performance and an extension of the circuit with a power down function.

Described are the comparison of the TEA1081 with the TEA1080, applications of the TEA1081 with the TEA1060 including its effect on the transmission characteristics, and application of the TEA1081 in a pulse dial telephone set.

*** ETT8710**

Specification of quartz and ceramic resonators for PCD33xx and PCF84cxx CMOS ICs

Details: 34 pages, September 1987

The oscillator of the PCD33xx and PCF84cxx CMOS integrated circuits was originally designed to operate with a quartz resonator. Ceramic (or PXE) resonators form an economically attractive alternative but can not always replace the quartz. A procedure is described which explains how to decide whether or not a ceramic resonator is suited for the oscillator. The report gives also general and more specific information on oscillators, on start-up time and on parasitic effects in quartz or ceramic resonators.

ETT8711

Bridge: A software tool for optimising the TEA1060 anti-sidetone bridge

Details: 11 pages, September 1987

Bridge is a software tool that helps you to find the optimal anti-sidetone balance network for your TEA1060 application. It is designed for use with the IBM PC or compatibles.

Starting with your initial guess BRIDGE can calculate a better balance network resulting in a lower average sidetone level. It can also present you the performance of balance networks graphically (if your computer is equipped with a colour/graphics adapter).

BRIDGE allows you full editing of all relevant parameters and components. Besides sets of parameters/components can be stored on disk for later retrieval.

There are two versions available on the diskette:

- BRIDGE which will run on every IBM PC or compatible
- BRIDGE87 which runs 4 times faster, but only on PCs equipped with a 8087 mathematical co-processor.

*** ETT8802**

Application proposal for the German market of the TEA1064 speech/transmission IC

Details: 34 pages, March 1988

This report describes an application of the TEA1064 for the German market. The TEA1064 is a bipolar integrated circuit performing all speech and line interface functions in electronic telephone sets. The TEA1064 is based on the well known TEA1068 with some performance improvements with respect to MUTE, AGC, receiving amplifier noise output, parallel operation and DTMF. Besides all features of the TEA1068 the TEA1064 incorporates a dynamic limiter in sending direction and a more flexible and powerful peripheral supply point.

The application is made in accordance with the German PTT requirements as described in "FTZ Pflichtenheft, FTZ 121 TR 8-8" of January 1988 taking into account latest updates until 9-3-88.

*** ETT89008**

Listening-in with the TEA1081, TDA7050 and TEA1064

Details: 27 pages, May 1989

This report describes a listening-in application with the TEA1081 supply IC, the TDA7050 loudspeaker amplifier and the TEA1064 transmission circuit for use in electronic telephone sets.

*** ETT89009**

Application of the versatile speech/transmission circuit TEA1064 in full electronic telephone sets

Details: 84 pages, August 1989

The TEA1064 is a speech/transmission integrated circuit for use in analogue electronic telephone sets. It is added to the range of well-known transmission circuits of the TEA1060-family. The circuit incorporates a relatively powerful supply for peripheral circuits (such as microcomputers and diallers) with two options: a) stabilised supply or b) regulated line voltage. Furthermore a dynamic limiter in the sending channel has been included that on the one hand limits the maximum level (and prevents distortion) of the transmitted line signal and on the other hand improves sidetone performance by reducing the maximum sidetone level and the distortion. This report gives a complete description of the circuit and provides the necessary information to the set-design-engineer in order to enable him to take full advantage of the many application possibilities.

*** ETT89016 (SUPERSEDES ETT8613)**

Measures to meet EMC requirements for TEA1060-family speech/transmission circuits

Details: 19 pages, 1-10-89

Recently the Electro Magnetic Compatibility (EMC) of the TEA1060-family, speech/transmission circuits, have been investigated again. If a few components are placed at the right spots the TEA1060 circuits reach a good performance. This report describes the measures which can be taken without influencing the basic functioning of the IC.

*** ETT94001**

Application of the TEA1096 transmission and listening-in circuit

Details: 60 pages, January 1994

The TEA1096 as well as the TEA1096A are bipolar telephony IC's for use in line powered telephone sets. They offer a transmission function and a group listening-in (or monitoring) facility of the received line signal via a loudspeaker. The TEA1096 and TEA1096A incorporate a line interface with active output stage, a stabilised supply, send and receive amplifiers, a double anti side tone circuit, line loss compensation, a loudspeaker amplifier and dynamic limiters for transmit and loudspeaker signal.

This report gives a detailed description of the TEA1096 and the TEA1096A and an application example. The description is given by means of block diagrams and discussion of the details of the sub-blocks. For product details is referred to the Device Specification ref.1.

ETT94008 (SUPERSEDES ETT/AN92011)

Functional specification of the demo PCD3353A/008 to control the PCA1070 (PACT)

Details: 39 pages, May 1995

This report gives a description of demonstration and test software to control the PCA1070 which is a Programmable Analogue CMOS Transmission (PACT) circuit, with the PCD3353A microcomputer.

The PCD3353A/008, a member of the PCD335xA family of micro-computer special developed for telecom applications. This PCD3353A micro-controller has an on-board DTMF generator, 6K ROM, 128 bytes RAM, 128 bytes EEPROM, 20 I/O and a special ringer output. And is fully able to control the PCA1070 via it's software I^{2}C-bus.

The PCA1070/PCD3353A circuits combination performs the following functions:

- Pulse and DTMF dialling
- Redial and repertory dial stored in EEPROM
- PCA1070 control
- PCA1070 variable stored in EEPROM
- PCA1070 variable programmable via I^{2}C-bus and Keyboard
- Dialling options programmable via keyboard stored in EEPROM
- Ringer functions incorporated in 3-tone, 4-speeds and 4 volumes
- Display.

* ETT95007.0.0

OM4757 demonstration board with the PCD3332-3, TEA1064B/1062 and TEA1093/1094

Details: 37 pages, April 1995

This OM4757 is a demonstration model of a feature phone realised with the PCD3332-3 dialler/ringer, the TEA1064B or TEA1062 transmission IC, the TEA1093 or TEA1094 handsfree circuit and a ringer stage.

The feature phone contains a general application with different demonstration possibilities with respect to transmission and handsfree ICs. It is not made to fulfil specific country requirements.

The OM4757 contains a handset with microphone and earpiece and a base with the hardware including buzzer, microphone and loudspeaker. The OM4757 is delivered with the TEA1064B, TEA1093 and PCD3332-3. The TEA1064B can be replaced by the TEA1062 and the TEA1093 by the TEA1094.

The TEA1093 is line powered. Although the TEA1094 is intended for supply by an external source, the demonstration model is provided with the TEA1094-supply from the line as well.

*** 9398 341 10011**

TEA1060 family designer's guide - versatile speech/transmission ICs for electronic telephone sets

Details: 72 pages, July 1987

This designer's guide gives an overview, subscriber set architectures, a detailed functional description, hints for PCB layout and anti-sidetone bridge calculations for the TEA1060 family. Powered by the telephone line, these ICs can be used with virtually any kind of microphone and the set's impedance can be complex or real. Besides their application in basic and feature phones, they can be used in automatic answering machines, facsimile equipment and cordless phones. The choice of TEA1060 family IC depends upon the microphone used and local PTT requirements.

*** 9398 061 30011**

An introduction to the basics of electronic telephone sets

Details: 53 pages, January 1994

The Telecom Applications Group of Philips Components Division has organised field application engineer (FAE) training sessions on several occasions. These training sessions cover both theoretical and practical work. This course note summarises much of the basic theory presented at the training sessions. It's aim is to give engineers working in the area of components sales, application, and design, a thorough introduction to the fundamentals of analogue telephony circuitry. This consists of the analogue telephone set and other subscriber equipment connected to the analogue local subscriber lines (also referred to as central office lines, PABX lines, a/b wires or ring/tip wires. In later course notes subjects covered will include: switching, cordless telephony, mobile telephony, ISDN, transmission, radio paging, data communication.

The introduction in section 1 gives a brief description of the fundamentals of classical telephone sets (with rotary dial and carbon microphone). Section 2 covers the DC requirements of a telephone set in relation to the line current and operating voltage. Section 3 describes the speech circuitry in more detail. Theory as well as practical electronic replacement for the coil hybrid are described. New features not available with carbon microphone sets are also included. In section 4 the dialling circuitry is described. Electronic pulse diallers, the modern DTMF dialling system, and PTT requirements are also covered in section 4. The ringer is described in section 5, and section 6 summarises all the user-friendly enhanced features of an advanced electronic telephone set.

THE I^{2}C-BUS CONCEPT

Details: 27 pages

This document gives an overview of the design of I^{2}C-bus. The complete specification is given in publication "The I^{2}C-bus and how to use it (including specifications), ordering code 9398 393 40011, April 1995.

***IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-19, NO. 3, JUNE 1984**

Dual tone and modem frequency generator with on-chip filters and voltage reference

Details: 10 pages, June 1984, (Reprint from IEEE journal of solid-state circuits)

A single-chip CMOS circuit is described that contains a dual tone multi-frequency (DTMF) and modern frequency generator. For optimum performance and economy, switched capacitor techniques are used for the on-chip bandgap reference voltage, D-A converters, and filter. CEPT recommendations on output level stability and distortion are met without recourse to external filtering and without a stabilised supply or external reference voltage. A self aligned contact (SAC) CMOS process with 4 μm design rules and with 50 nm thick gate oxide is used to manufacture the circuit.

TTE87132

Documentation for printed circuit board CAB3467

Details: 6 pages, June 1987

This printed circuit board incorporates a full-wave rectifier especially suited for use as polarity guard in electronic pulse-dialling/flash telephone sets. Optionally also an electronic interrupter is presented on the board.

The bridge is realised with DMOS-field effect transistors, combining a very low forward voltage drop (total voltage drop is typ. 0.18 V at 10 mA) with a very high maximum voltage rating (200 V).

The (optional) interrupter is equipped with a DMOS P-channel FET which combines the advantages of conventional N-channel FETs (virtually no driving current required) with those of PNP-transistor interrupters (very simple interface between pulse dialler and interrupter).

The complete board is realised in SMD technology.

TTE87168

Documentation for TEA1064 printed circuit board CAB3458

Details: 21 pages, November 1987

This report describes the printed circuit board CAB3458. This printed circuit board is meant to demonstrate the speech transmission IC TEA1064. This report gives some brief application information, but is not meant as an application report. Please refer to the literature given in chapter 4 for application details.

DEVICE DATA

(in alphanumeric sequence)

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

P-N-P transistors in plastic TO-92 package, primarily intended for use in driver and output stages of audio amplifiers.

The BC327, BC327A, BC328 are complementary to the BC337, BC337A and BC338 respectively.

QUICK REFERENCE DATA

			BC327	BC327A	BC328	
Collector-emitter voltage ($V_{BE} = 0$)	$-V_{CES}$	max.	50	60	30	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	45	60	25	V
Collector current (peak value)	$-I_{CM}$	max.	1000			mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	800			mW
Junction temperature	T_j	max.	150			°C
Transition frequency at f = 100 MHz $-I_C = 10$ mA; $-V_{CE} = 5$ V	f_T	>	80			MHz
D.C. current gain $-I_C = 100$ mA; $-V_{CE} = 1$ V	h_{FE}		100 to 600			

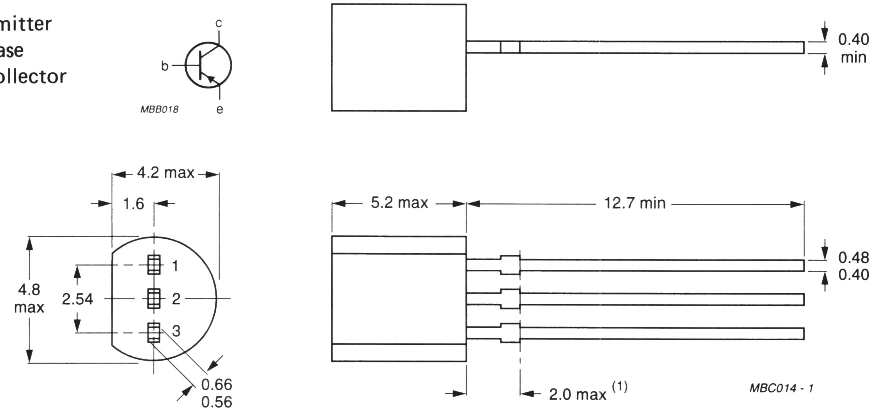
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning

1 = emitter
2 = base
3 = collector



Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

N-P-N transistors in plastic TO-92 package, primarily intended for use in driver and output stages of audio amplifiers.

The BC337, BC337A, BC338 are complementary to the BC327, BC327A and BC328 respectively.

QUICK REFERENCE DATA

			BC337	BC337A	BC338	
Collector-emitter voltage (V_{BE} = 0)	V_{CES}	max.	50	60	30	V
Collector-emitter voltage (open base)	V_{CEO}	max.	45	60	25	V
Collector current (peak value)	I_{CM}	max.		1000		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		800		mW
Junction temperature	T_j	max.		150		°C
Transition frequency at f = 100 MHz I_C = 10 mA; V_{CE} = 5 V	f_T	>		100		MHz
D.C. current gain I_C = 100 mA; V_{CE} = 1 V	h_{FE}			100 to 600		

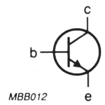
MECHANICAL DATA

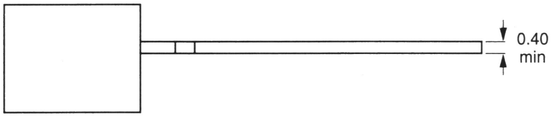
Dimensions in mm

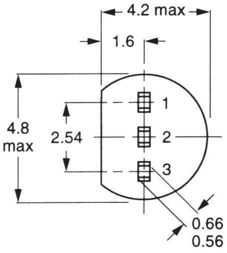
Fig. 1 TO-92.

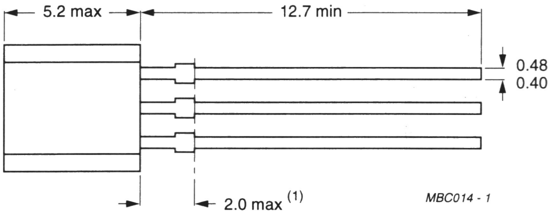
Pinning

1 = emitter
2 = base
3 = collector









Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

General purpose n-p-n transistors in a plastic TO-92 package.

QUICK REFERENCE DATA

			BC546	BC547	BC548	
Collector-emitter voltage ($V_{BE} = 0$)	V_{CES}	max.	80	50	30	V
Collector-emitter voltage (open base)	V_{CEO}	max.	65	45	30	V
Collector current (peak value)	I_{CM}	max.	200	200	200	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	500	500	500	mW
Junction temperature	T_j	max.	150	150	150	^oC
D.C. current gain $I_C = 2$ mA; $V_{CE} = 5$ V	h_{FE}	$>$	110	110	110	
		$<$	450	800	800	
Transition frequency at f = 100 MHz $I_C = 10$ mA; $V_{CE} = 5$ V	f_T	$>$	100	100	100	MHz
Noise figure at $R_S = 2\ k\Omega$ $I_C = 200\ \mu A$; $V_{CE} = 5$ V f = 1 kHz; B = 200 Hz	F	typ.	2	2	2	dB

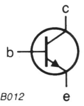
MECHANICAL DATA

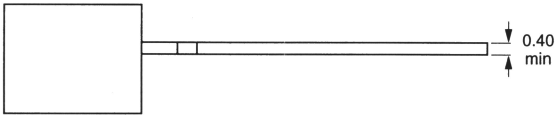
Dimensions in mm

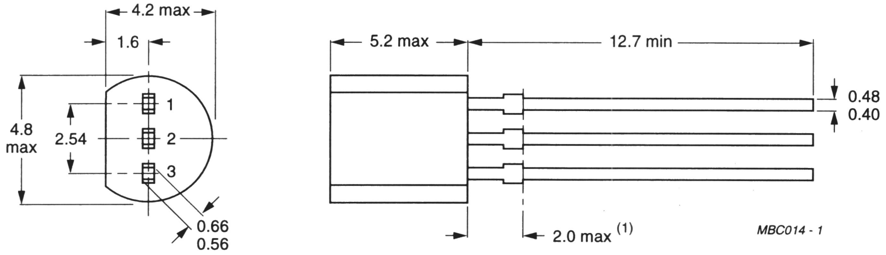
Fig. 1 TO-92.

Pinning

1 = emitter
2 = base







Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

General purpose p-n-p transistors in plastic TO-92 package.

QUICK REFERENCE DATA

			BC556	BC557	BC558	
Collector-emitter voltage (+ V_{BE} = 0 V)	$-V_{CES}$	max.	80	50	30	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	65	45	30	V
D.C. current gain $-I_C$ = 2 mA; $-V_{CE}$ = 5 V	h_{FE}	>	75	75	75	
		<	475	800	800	
Collector current (peak value)	$-I_{CM}$	max.	200			mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	500			mW
Junction temperature	T_j	max.	150			°C
Transition frequency at f = 100 MHz $-I_C$ = 10 mA; $-V_{CE}$ = 5 V	f_T	>	100			MHz
Noise figure at R_S = 2 kΩ $-I_C$ = 200 μA; $-V_{CE}$ = 5 V f = 1 kHz; B = 200 Hz	F	typ.	2			dB

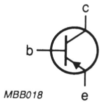
MECHANICAL DATA

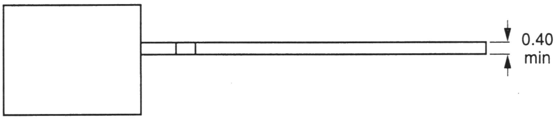
Dimensions in mm

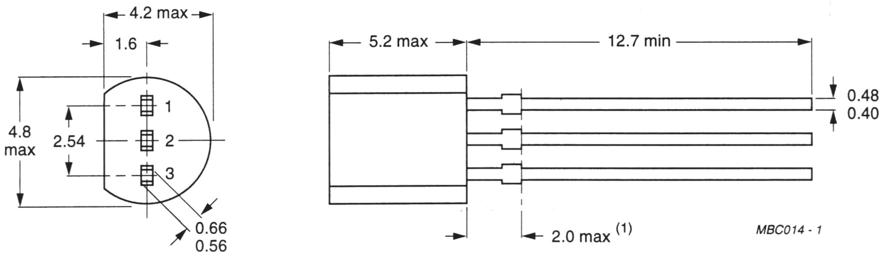
Fig. 1 TO-92

Pinning

1 = emitter
2 = base
3 = collector







Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

General purpose n-p-n transistors in a plastic SOT-23 package.

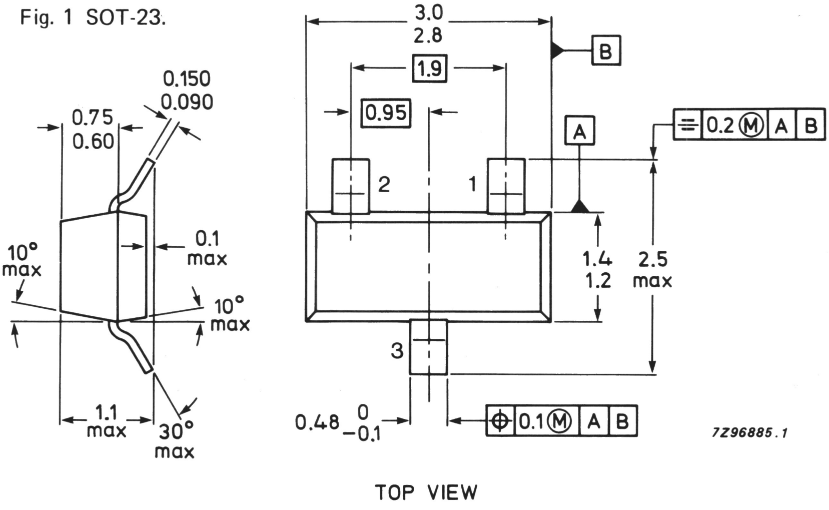
QUICK REFERENCE DATA

			BC846	BC847	BC848	
Collector-emitter voltage (V_{BE} = 0)	V_{CES}	max.	80	50	30	V
Collector-emitter voltage (open base)	V_{CEO}	max.	65	45	30	V
Collector current (peak value)	I_{CM}	max.	200	200	200	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	250	250	mW
Junction temperature	T_j	max.	150	150	150	°C
DC current gain I_C = 2 mA; V_{CE} = 5 V	h_{fe}	$>$ $<$	110 450	110 800	110 800	
Transition frequency at f = 100 MHz I_C = 10 mA; V_{CE} = 5 V	f_T	$>$	100	$>$ 100	$>$ 100	MHz
Noise figure at R_S = 2 kΩ I_C = 200 μA; V_{CE} = 5 V f = 1 kHz; B = 200 Hz	F	typ.	2	2	2	dB

MECHANICAL DATA

Fig. 1 SOT-23.

Dimensions in mm


3.0
2.8
B
1.9
0.95
A
0.2 Ⓜ A B
0.150
0.090
0.75
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2
1
0.1
max
10°
max
10°
max
1.4
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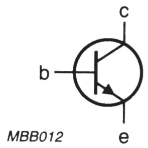
2.5
max
3
1.1
max
30°
max
0.48 0
−0.1
0.1 Ⓜ A B
7Z96885.1
TOP VIEW

Marking code:

BC846 = 1Dp
BC846A = 1Ap
BC846B = 1Bp
BC847 = 1Hp
BC847A = 1Ep
BC847B = 1Fp
BC847C = 1Gp
BC848 = 1Mp
BC848A = 1Jp
BC848B = 1Kp
BC848C = 1Lp

Pinning:

1 = base
2 = emitter
3 = collector



Reverse pinning types are available on request.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON PLANAR EPITAXIAL TRANSISTORS

P-N-P transistors, in a SOT-23 plastic package.

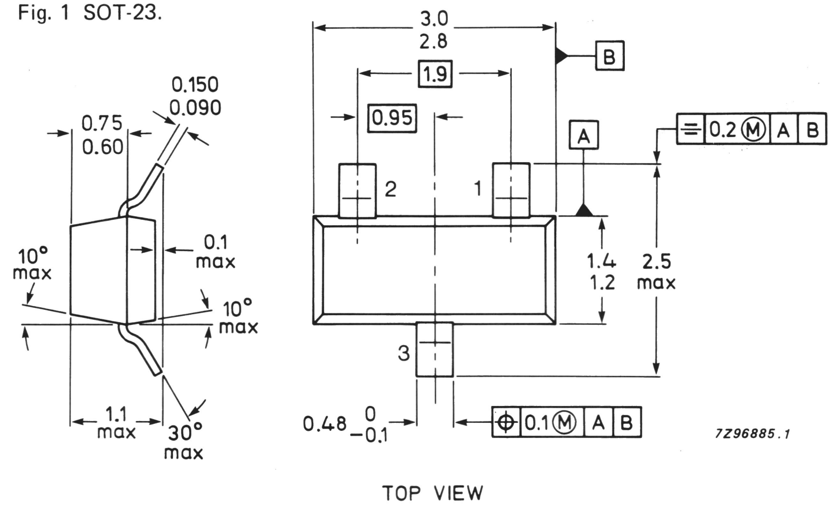
QUICK REFERENCE DATA

			BC856	BC857	BC858	
Collector-emitter voltage ($+V_{BE} = 1$ V)	$-V_{CEX}$	max.	80	50	30	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	65	45	30	V
Collector current (peak value)	$-I_{CM}$	max.		200		mA
Total power dissipation up to $T_{amb} = 60$ °C	P_{tot}	max.		250		mW
Junction temperature	T_j	max.		150		°C
DC current gain $-I_C = 2$ mA; $-V_{CE} = 5$ V	h_{fe}			75 to 800		
Transition frequency at f = 100 MHz $-I_C = 10$ mA; $-V_{CE} = 5$ V	f_T	>		100		MHz
Noise figure at $R_S = 2$ kΩ $-I_C = 200$ μA; $-V_{CE} = 5$ V f = 1 kHz; B = 200 Hz	F	<		10		dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.


0.150
0.090
0.75
0.60
0.1
max
10°
max
10°
max
1.1
max
30°
max
3.0
2.8
B
1.9
0.95
A
0.2 Ⓜ A B
2
1
1.4
1.2
2.5
max
3
0.48 0 −0.1
0.1 Ⓜ A B
7Z96885.1
TOP VIEW

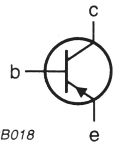
Reverse pinning types are available on request.

Marking code:

BC856	= 3Dp
BC856A	= 3Ap
BC856B	= 3Bp
BC857	= 3Hp
BC857A	= 3Ep
BC857B	= 3Fp
BC857C	= 3Gp
BC858	= 3Mp
BC858A	= 3Jp
BC858B	= 3Kp
BC858C	= 3Lp

Pinning:

1 = base
2 = emitter
3 = collector



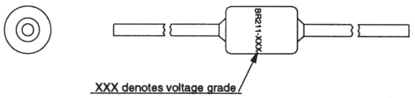
GENERAL DESCRIPTION

A range of bidirectional, breakover diodes in an axial, hermetically sealed, glass envelope. These devices feature controlled breakover voltage and high holding current together with high peak current handling capability. Typical applications include transient overvoltage protection in telecommunications equipment.

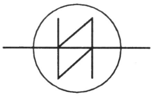
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
	BR211-100 to 280			
$V_{(BO)}$	Breakover voltage	100	280	V
I_H	Holding current	150	-	mA
I_{TSM}	Non-repetitive peak current	-	40	A

OUTLINE - SOD84



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_D	Continuous voltage		-	75% of $V_{(BO)typ}$	V
I_{TSM1}	Non repetitive peak current	10/320 µs impulse equivalent to 10/700 µs, 1.6 kV voltage impulse (CCITT K17)	-	40	A
I_{TSM2}	Non repetitive on-state current	half sine wave; t = 10 ms; T_j = 70 °C prior to surge	-	15	A
I^2t	I^2t for fusing	t_p = 10 ms	-	1.1	A^2s
dI_T/dt	Rate of rise of on-state current after $V_{(BO)}$ turn-on	t_p = 10 µs	-	50	A/µs
P_{tot}	Continuous dissipation	T_a = 25°C	-	1.2	W
P_{TM}	Peak dissipation	t_p = 1 ms; T_a = 25°C	-	50	W
T_{stg}	Storage temperature		-65	150	°C
T_a	Operating ambient temperature	off-state	-	70	°C
T_{vj}	Overload junction temperature	on-state	-	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC02 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistor

BS107

FEATURES

- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
V_{GSth}	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	150	mA
R_{DSon}	drain-source on-state resistance	28	Ω

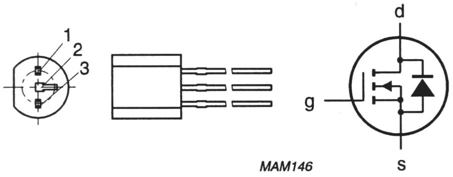


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.4 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	200 mS 350 mS

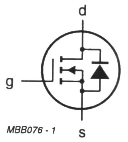
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92

Pinning

1 = source
2 = gate
3 = drain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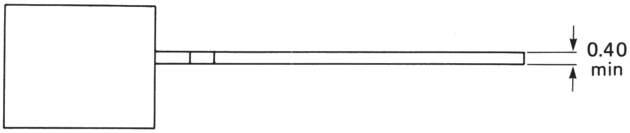

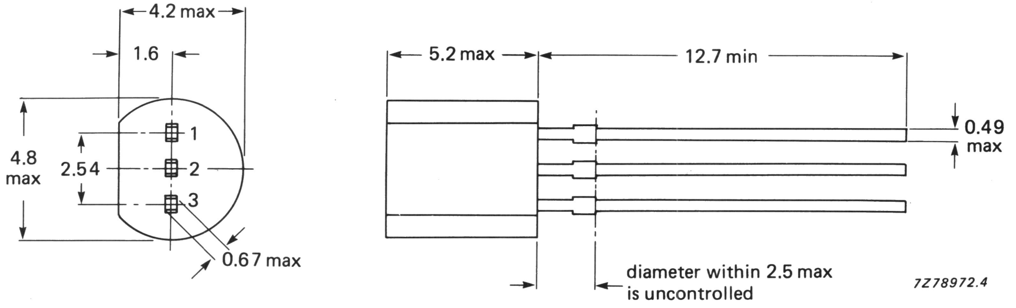
4.2 max
1.6
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max
2.54
1
2
3
0.67 max
5.2 max
12.7 min
0.49
max
diameter within 2.5 max
is uncontrolled
7Z78972.4

Note: Various pinnings are available.

N-channel enhancement mode vertical D-MOS transistor

BS108

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	source
2	gate
3	drain

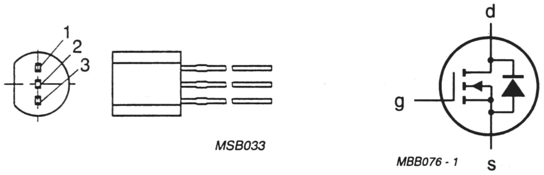


Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 x 10 mm

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830	mW
Junction temperature	T_j	max.	150	°C
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	max.	5	Ω

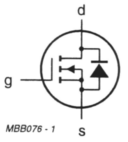
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain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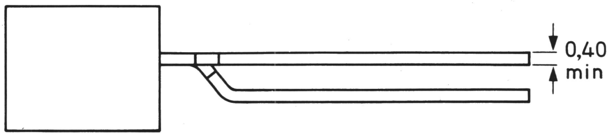
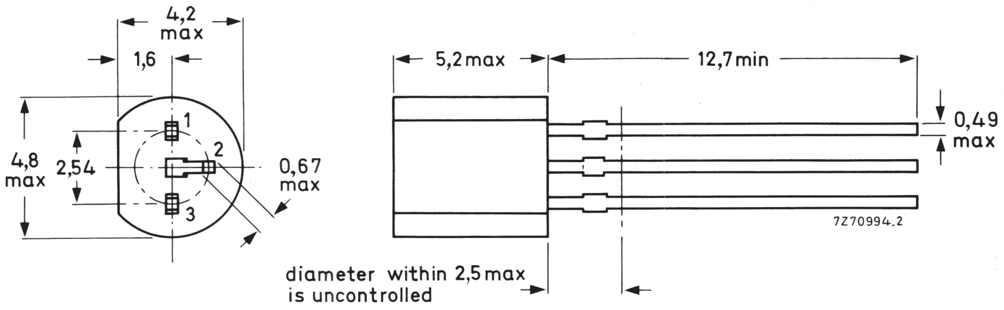



4,2
max
1,6
4,8
max
2,54
1
2
3
0,67
max
5,2max
12,7min
0,49
max
7Z70994.2
diameter within 2,5max
is uncontrolled

Note: Various pin configurations available.

N-channel enhancement mode vertical D-MOS transistors

BSN10; BSN10A

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use in general purpose fast switching applications.

PINNING

PIN	DESCRIPTION
BSN10	
1	gate
2	drain
3	source
BSN10A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	175	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

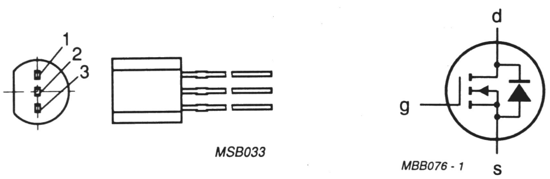


Fig.1 Simplified outline (TO-92) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	175	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm.

N-channel enhancement mode vertical D-MOS transistor

BSN20

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a surface-mounted device in thin and thick film circuits and in general purpose fast switching applications.

PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	100	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

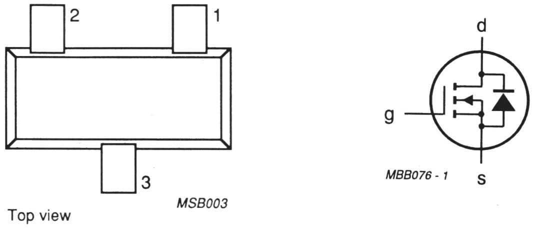


Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	300	mW
		up to T_{amb} = 25 °C (note 2)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430 K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500 K/W

Notes

1. Transistor mounted on a ceramic substrate, 10 x 8 x 0.7 mm.
2. Transistor mounted on a printed circuit board.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTORS

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

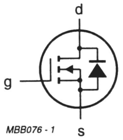
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92 variant.

Pinning (BSN254)

1 = gate
2 = drain
3 = source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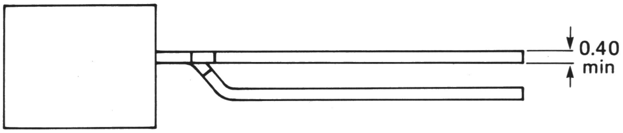
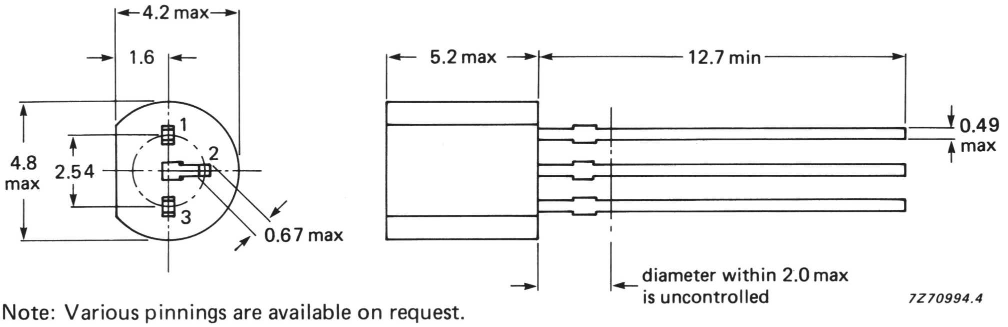
Pinning (BSN254A)

1 = source
2 = gate
3 = drain




4.2 max
1.6
4.8
max
2.54
1
2
3
0.67 max
5.2 max
12.7 min
0.49
max
diameter within 2.0 max
is uncontrolled
7Z70994.4

Note: Various pinnings are available on request.

Data sheet	
status	Product specification
date of issue	April 1995

BSN274/BSN274A

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	drain current (DC)	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	threshold voltage	2	V

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistors

BSN304; BSN304A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
BSN304	
1	gate
2	drain
3	source
BSN304A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	1	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 250$ mA; $V_{GS} = 10$ V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ mA; $V_{GS} = V_{DS}$	0.8	2	V

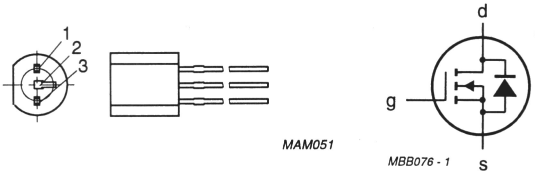


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

MECHANICAL DATA

Dimensions in mm

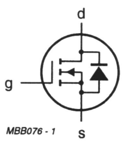
Marking code

BSP126

Fig.1 SOT223.

Pinning

1 = gate
2 = drain
3 = source
4 = drain



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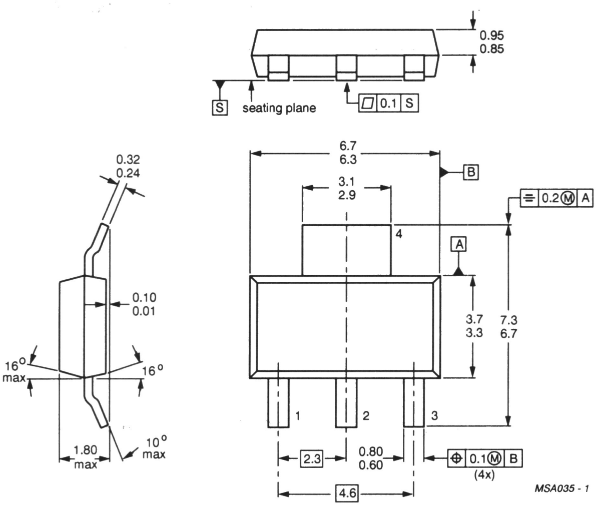
MBB076 - 1



0.95
0.85
S
seating plane
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0.10
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16°
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16°
1.80
max
10°
max
MSA035 - 1

N-channel enhancement mode vertical D-MOS transistor

BSP130

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

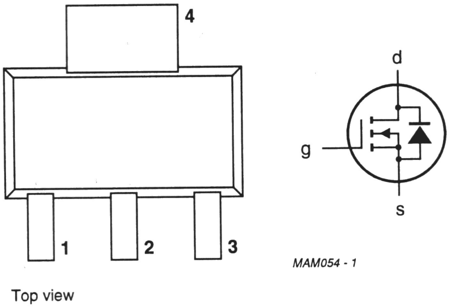
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	0.8	2	V



Marking code
BSP130.

Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-channel enhancement mode vertical D-MOS transistor

BSP145

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for applications in relay, high speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

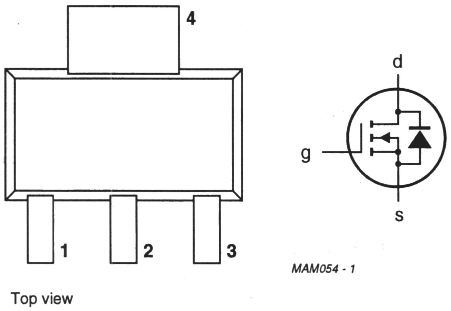


Fig.1 Simplified outline and symbol.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	450	V
V_{GSO}	gate-source voltage	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$	3	4	V
I_D	drain current		–	250	mA
R_{DSon}	drain-source on-state resistance	$I_D = 100$ mA; $V_{GS} = 10$ V	10	14	Ω
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	1.5	W

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

BSP225

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200$ mA $-V_{GS} = 10$ V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1$ mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

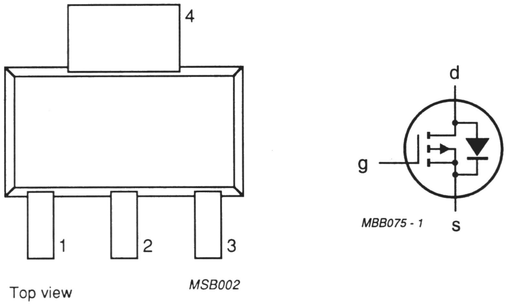


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

P-channel enhancement mode vertical D-MOS transistor

BSP254; BSP254A

FEATURES

- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant BSP254

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant BSP254A

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	–250	V
V_{GSO}	gate-source voltage	open drain	–	–	±20	V
$\lvert y_{fs} \rvert$	forward transfer admittance	ID = –200 mA; V_{DS} = –25 V	100	200	–	mS
I_D	drain current (DC)		–	–	–0.2	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –200 mA	–	10	15	Ω
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	–	1	W

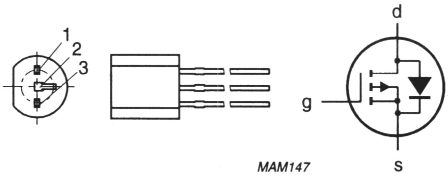


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A

FEATURES

- Direct interface to C-MOS, TTL etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
BSP304		
1	g	gate
2	d	drain
3	s	source
BSP304A		
1	s	source
2	g	gate
3	d	drain

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

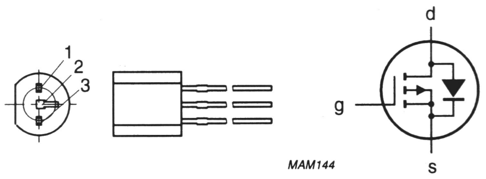


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1.7	–2.55	V
I_D	drain current (DC)		–	–170	mA
R_{DSon}	drain-source on-state resistance	$I_D = -170$ mA; $V_{GS} = -10$ V	–	17	Ω
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	1	W

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

P-channel enhancement mode vertical D-MOS transistor

BSP92

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

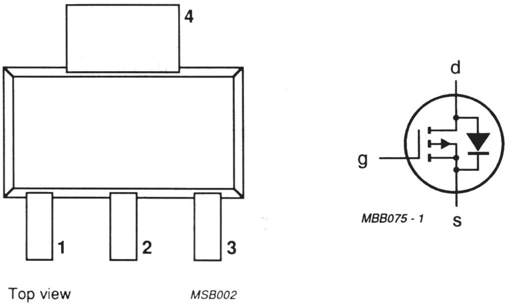


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and highspeed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

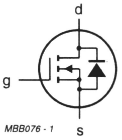
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1	W
Drain-source ON-resistance $I_D = 400$ mA; $V_{GS} = 10$ V	R_{DSon}	typ. max.	4.5 6	Ω Ω
Transfer admittance $I_D = 400$ mA; $V_{DS} = 25$ V	$\|y_{fs}\|$	min. typ.	140 350	mS mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = gate
2 = drain
3 = source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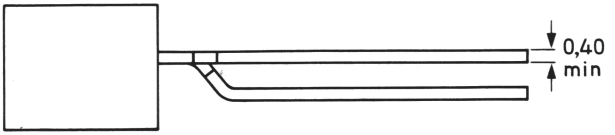

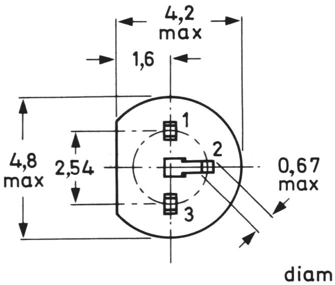
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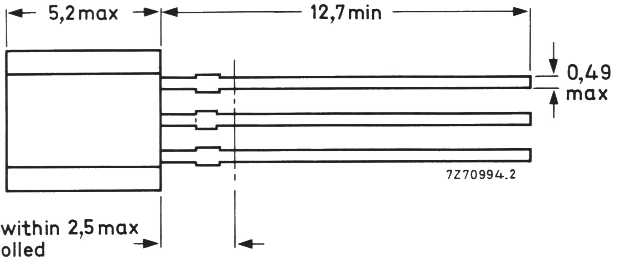
5,2 max
12,7 min
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7Z70994.2
diameter within 2,5 max
is uncontrolled

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers, and as a line current interruptor in telephony applications.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.15	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 20	Ω Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	60 200	mS mS

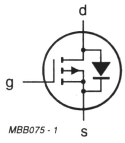
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = gate
2 = drain
3 = source



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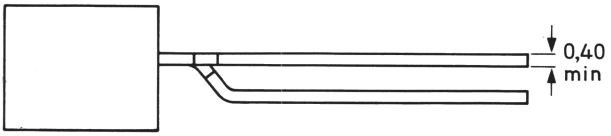

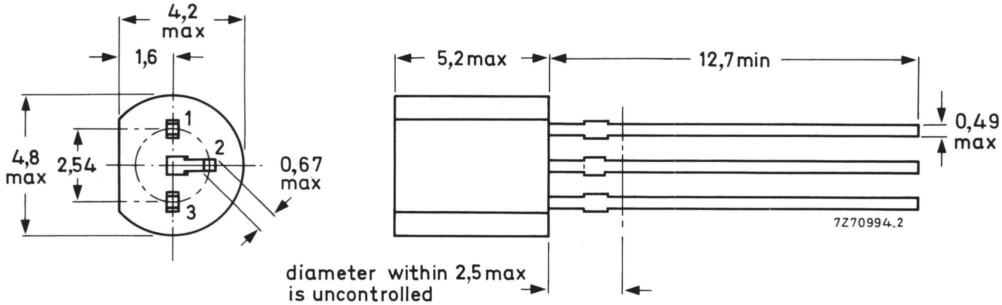

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max
5,2 max
12,7 min
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max
7Z70994.2
diameter within 2,5 max
is uncontrolled

N-channel depletion mode vertical D-MOS transistors

BST124

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a TO-126 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-126

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	450	mA
P_{tot}	total power dissipation	up to T_h = 120 °C	–	6	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	–1.65	–0.75	V

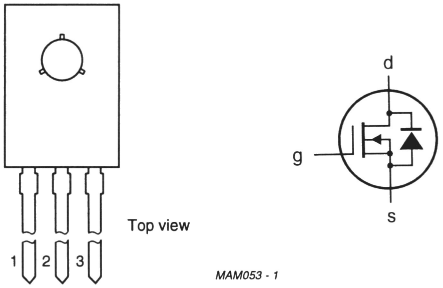


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	450	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_h = 120 °C	–	6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs}\rvert$	typ.	250 mS

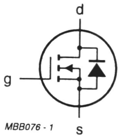
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain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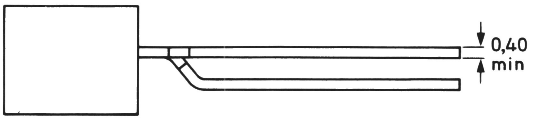

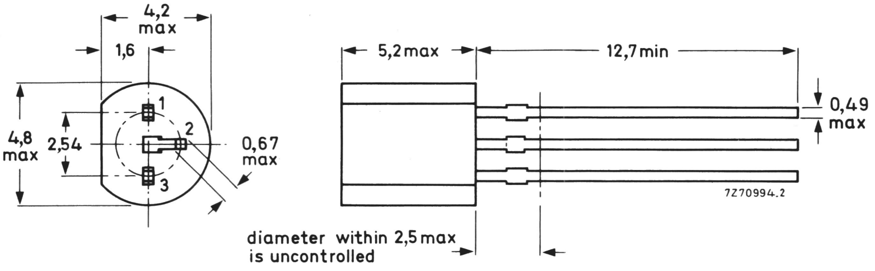
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3
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max
5,2 max
12,7 min
0,49
max
7Z70994.2
diameter within 2,5 max
is uncontrolled

Note: Various pinout configurations available.

Voltage regulator diodes BZW03 series

FEATURES

- Glass passivated
- High maximum operating temperature
- Low leakage current
- Excellent stability
- Zener working voltage range: 7.5 to 270 V for 38 types
- Transient suppressor stand-off voltage range: 6.2 to 430 V for 45 types
- Available in ammo-pack
- Also available with preformed leads for easy insertion.

DESCRIPTION

Rugged glass SOD64 package, using a high temperature alloyed construction. This package is hermetically sealed and fatigue free as coefficients of expansion of all used parts are matched.

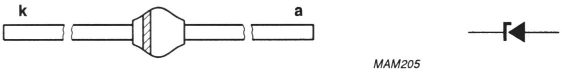


Fig.1 Simplified outline (SOD64) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
P_{tot}	total power dissipation	T_{tp} = 25 °C; lead length 10 mm	–	6.00	W
		T_{amb} = 45 °C; PCB mounted	–	1.75	W
P_{ZRM}	repetitive peak reverse power dissipation		–	20	W
P_{ZSM}	non-repetitive peak reverse power dissipation	t_p = 100 µs; square pulse; T_j = 25 °C prior to surge	–	1000	W
P_{RSM}	non-repetitive peak reverse power dissipation	10/1 000 µs exponential pulse; T_j = 25 °C prior to surge	–	500	W
T_{stg}	storage temperature		−65	+175	°C
T_j	junction temperature		−65	+175	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

TRANSIENT SUPPRESSOR DIODE

A double-diffused silicon glass passivated diode in a hermetically sealed axial-leaded glass envelope intended for transient suppression in telephony equipment.

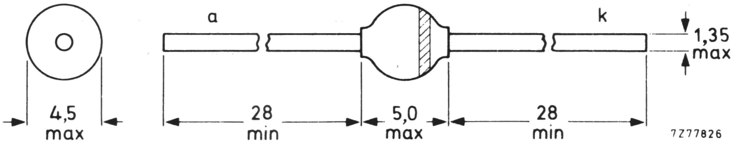
QUICK REFERENCE DATA

Stand-off voltage	V_R	max.	12 V
Non-repetitive peak reverse current	I_{RSM}	max.	50 A
Clamping voltage	$V_{(CL)R}$	<	28 V

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

HIGH VOLTAGE SILICON PLANAR TRANSISTORS

N-P-N high voltage silicon planar transistors in plastic TO-92 package for use in general purpose applications.

QUICK REFERENCE DATA

			MPSA42	MPSA43	
Collector-emitter voltage (open base)	V_{CEO}	max.	300	200	V
Collector-base voltage (open emitter)	V_{CBO}	max.	300	200	V
Collector current (d.c.)	I_C	max.	500		mA
Total device dissipation at T_{amb} = 25 °C	P_{tot}	max.	625		mW
Collector-emitter saturation voltage I_C = 20 mA; I_B = 2,0 mA	V_{CEsat}	max.	0,5		V
D.C. current gain I_C = 30 mA; V_{CE} = 10 V	h_{FE}	min.	40		

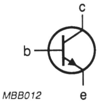
MECHANICAL DATA

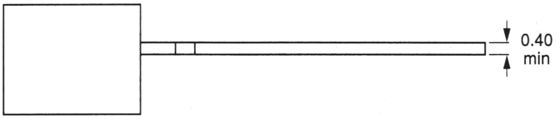
Dimensions in mm

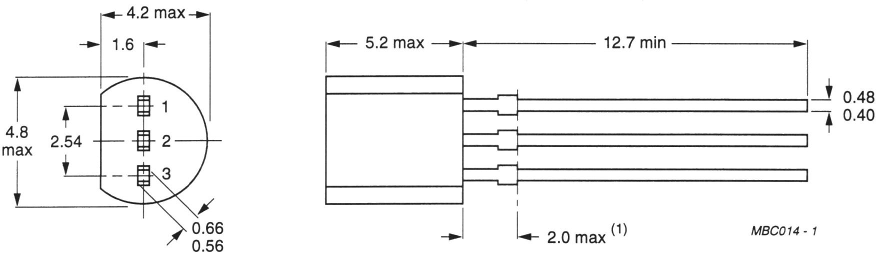
Fig. 1 TO-92.

Pinning

1 = collector
2 = base
3 = emitter







Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

NPN high voltage transistor MPSA44; MPSA45

FEATURES

- High voltage
- High current.

DESCRIPTION

High voltage NPN transistor in a SOT54 (TO-92) package, especially suitable for use in telecommunications applications.

PINNING - SOT54

PIN	DESCRIPTION
1	collector
2	base
3	emitter

PIN CONFIGURATION

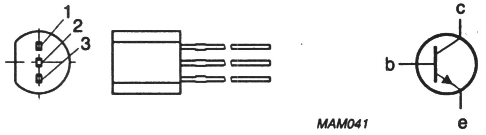


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	MPSA44		–	500	V
	MPSA45		–	400	V
V_{CEO}	collector-emitter voltage	open base			
	MPSA44		–	400	V
	MPSA45		–	350	V
$V_{CE(sat)}$	collector-emitter saturation voltage	$I_C = 50$ mA; $I_B = 5$ mA	–	750	mV
h_{FE}	DC current gain	$I_C = 100$ mA; $V_{CE} = 10$ V	40	–	
I_C	DC collector current		–	300	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	625	mW

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

HIGH VOLTAGE SILICON PLANAR TRANSISTORS

P-N-P high voltage silicon planar transistors in plastic TO-92 package for general purpose applications.

QUICK REFERENCE DATA

			MPSA92	MPSA93	
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	300	200	V
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	300	200	V
Collector current (d.c.)	$-I_C$	max.	500		mA
Total device dissipation at T_{amb} = 25 °C	P_{tot}	max.	625		mW
Collector-emitter saturation voltage $-I_C$ = 20 mA; $-I_B$ = 2,0 mA	$-V_{CEsat}$	max.	0,5		V
D.C. current gain $-I_C$ = 30 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	25		

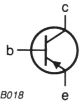
MECHANICAL DATA

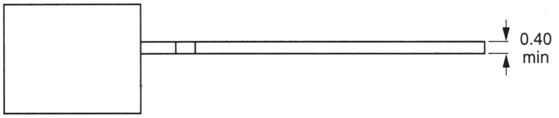
Dimensions in mm

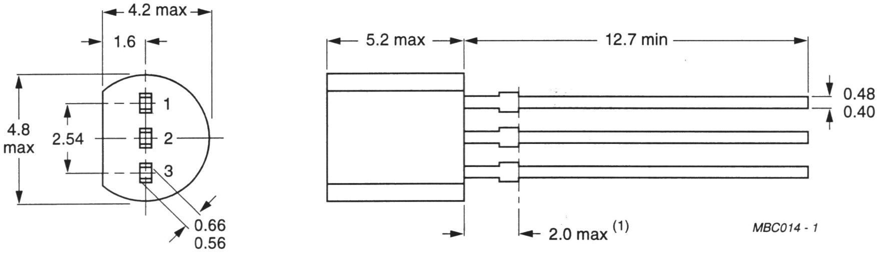
Fig. 1 TO-92.

Pinning

1 = collector
2 = base
3 = emitter







Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Tone decoder/phase-locked loop

NE/SE567

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor
- Military processing available

APPLICATIONS

- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging

PIN CONFIGURATIONS

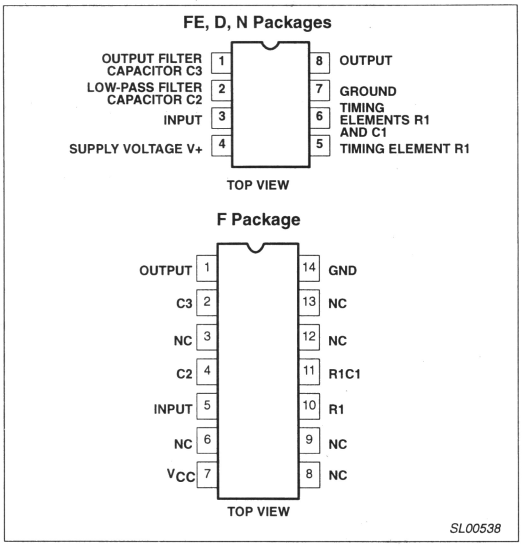
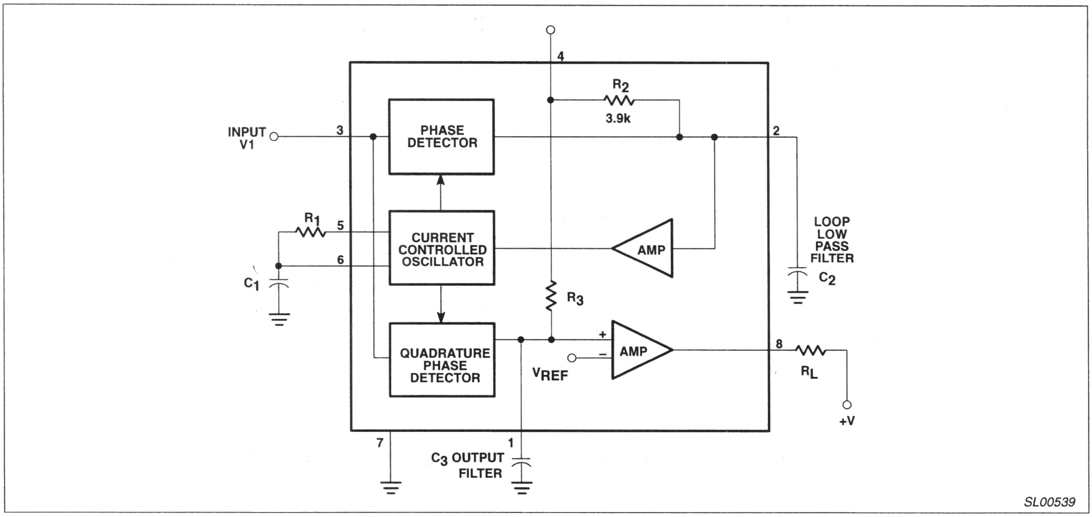

FE, D, N Packages
OUTPUT FILTER CAPACITOR C3 1
LOW-PASS FILTER CAPACITOR C2 2
INPUT 3
SUPPLY VOLTAGE V+ 4
8 OUTPUT
7 GROUND
6 TIMING ELEMENTS R1 AND C1
5 TIMING ELEMENT R1
TOP VIEW
F Package
OUTPUT 1
C3 2
NC 3
C2 4
INPUT 5
NC 6
VCC 7
14 GND
13 NC
12 NC
11 R1C1
10 R1
9 NC
8 NC
TOP VIEW
SL00538

Figure 1. Pin Configurations

- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

BLOCK DIAGRAM


4
R2
3.9k
INPUT V1
3
PHASE DETECTOR
2
R1
5
6
C1
CURRENT CONTROLLED OSCILLATOR
AMP
LOOP LOW PASS FILTER
C2
R3
QUADRATURE PHASE DETECTOR
VREF
+
-
AMP
8
RL
+V
7
1
C3 OUTPUT FILTER
SL00539

®Touch-Tone is a registered trademark of AT&T.

Figure 2. Block Diagram

EQUIVALENT SCHEMATIC

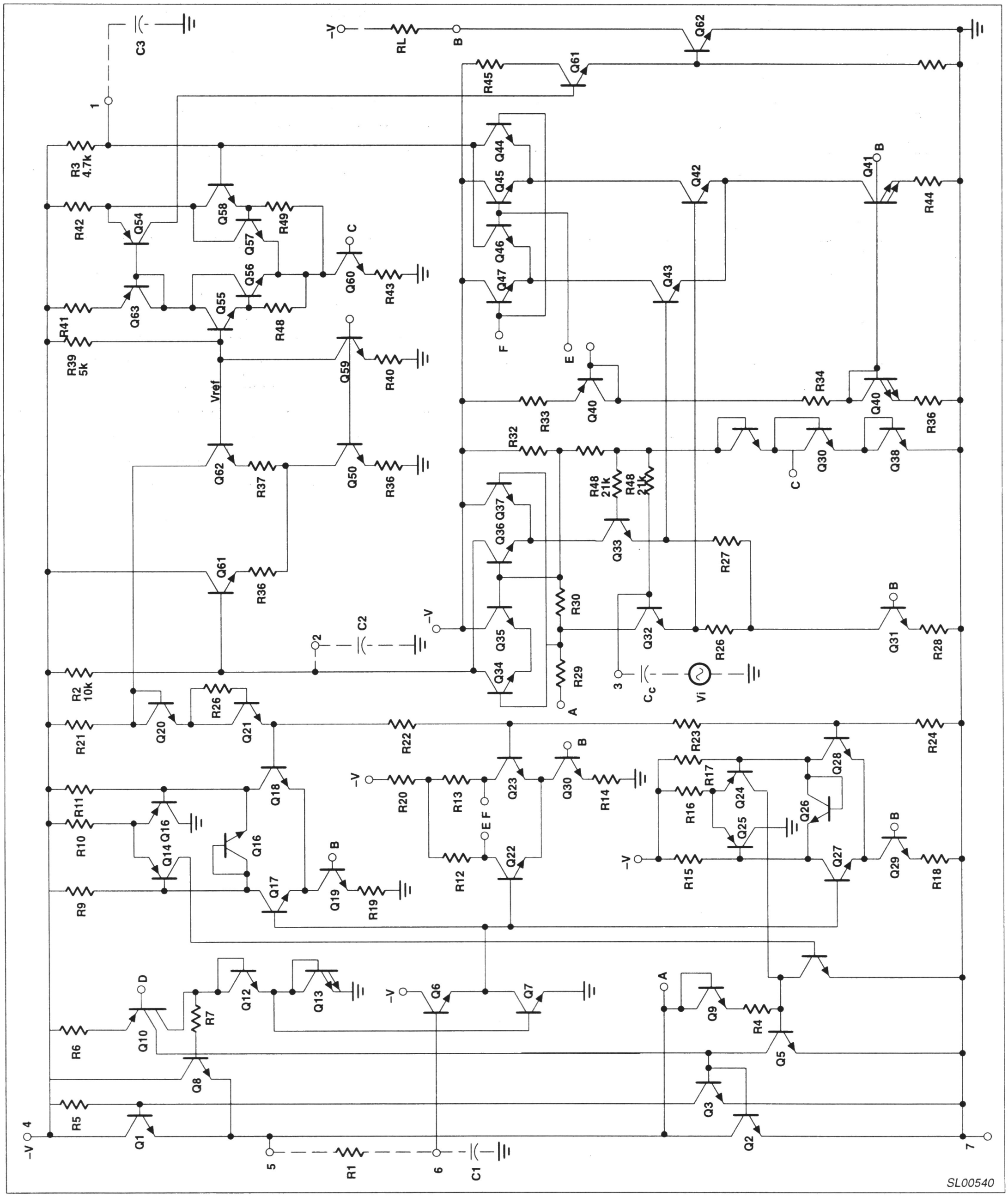

C3
1
–V
RL
B
Q62
R45
Q61
R3
4.7k
R42
Q54
Q58
Q57
R49
C
Q60
R43
Q56
Q55
R48
Q63
R41
R39
5k
Vref
Q59
R40
Q44
Q45
Q46
Q47
F
E
Q42
Q43
Q41
B
R44
Q40
R33
R34
R36
R32
R48
21k
Q30
Q38
C
Q62
R37
Q50
R36
Q36
Q37
Q33
R27
Q61
R36
C2
2
–V
Q35
Q34
R30
R29
A
Q32
R26
3
C_C
Vi
B
Q31
R28
R2
10k
R26
Q20
Q21
R21
R22
R23
R24
–V
R20
R13
Q23
Q30
R14
B
R17
R16
Q24
Q25
Q26
Q28
R11
R10
Q16
Q14
Q16
Q18
E F
R12
Q22
–V
R15
Q27
Q29
B
R18
R9
Q17
Q19
B
R19
D
Q10
R7
Q12
Q13
–V
Q6
Q7
A
Q9
R4
Q5
R6
Q8
Q3
R5
Q1
Q2
–V
4
5
R1
6
C1
7
SL00540

Figure 3. Equivalent Schematic

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic SO	0 to +70°C	NE567D	SOT96-1
14-Pin Cerdip	0 to +70°C	NE567F	0581B
8-Pin Plastic DIP	0 to +70°C	NE567N	SOT97-1
8-Pin Plastic SO	-55°C to +125°C	SE567D	SOT96-1
8-Pin Cerdip	-55°C to +125°C	SE567FE	0581B
8-Pin Plastic DIP	-55°C to +125°C	SE567N	SOT97-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature		
	NE567	0 to +70	°C
	SE567	-55 to +125	°C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 $+V_S$	V
V-	Negative voltage at input	-10	V_{DC}
V_{OUT}	Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

V +=5.0V; T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	-55 to +125°C 0 to +70°C		35 ±140 35 ±60			35 ±140 35 ±60		ppm/°C ppm/°C
f_O	Center frequency distribution	$f_O = 100\text{kHz} = \frac{1}{1.1R_1C_1}$	-10	0	+10	-10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100\text{kHz} = \frac{1}{1.1R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100\text{kHz} = \frac{1}{1.1R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth—variation with temperature	V_I=300mV$_{RMS}$		±0.1			±0.1		%/°C
BW	Largest detection bandwidth—variation with supply voltage	V_I=300mV$_{RMS}$		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	I_L=100mA, f_I=f_O		20	25		20	25	mV$_{RMS}$
	Largest no-output input voltage[4]	I_L=100mA, f_I=f_O	10	15		10	15		mV$_{RMS}$
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	B_n=140kHz		-6			-6		dB
Output									
	Fastest on-off cycling rate			f_O/20			f_O/20		
	"1" output leakage current	V_8=15V		0.01	25		0.01	25	μA
	"0" output voltage	I_L=30mA I_L=100mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V V
t_F	Output fall time[3]	R_L=50Ω		30			30		ns
t_R	Output rise time[3]	R_L=50Ω		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current—activated	R_L=20kΩ		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:

1. Frequency determining resistor R_1 should be between 2 and 20kΩ
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With R_2=130kΩ from Pin 1 to V+. See Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS

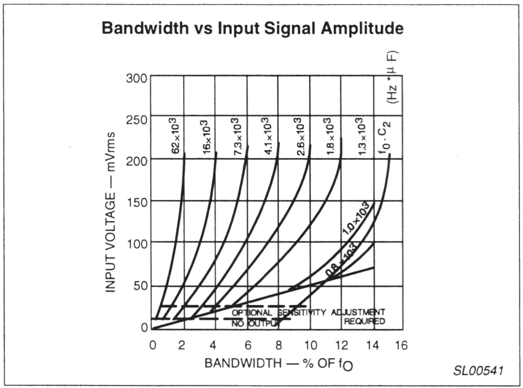


Figure 4.

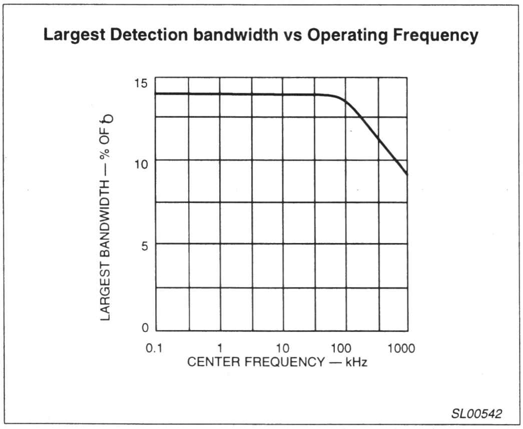


Figure 5.

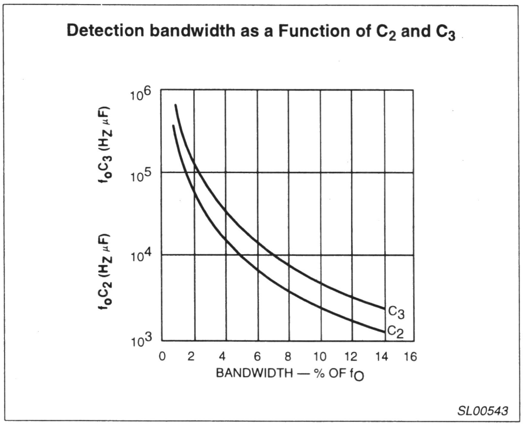


Figure 6.

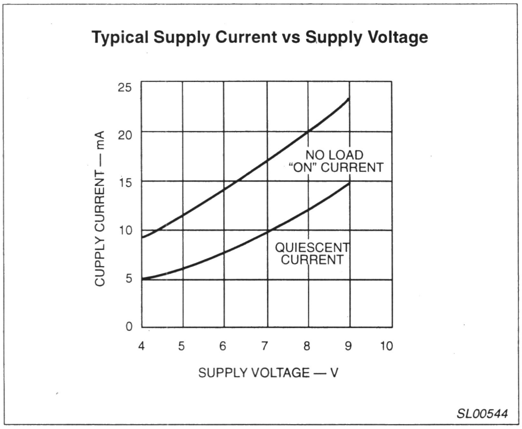


Figure 7.

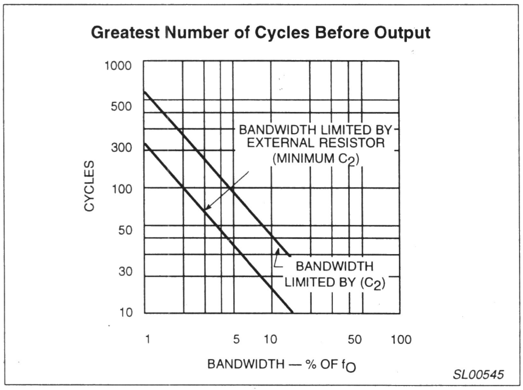


Figure 8.

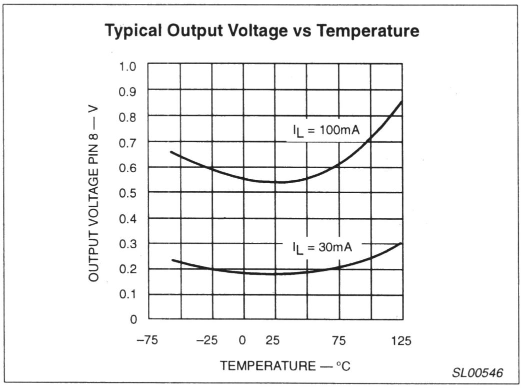


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

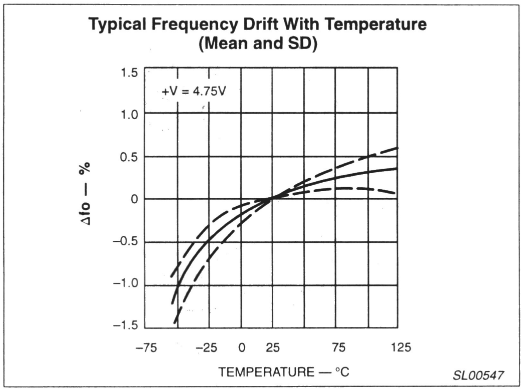

Typical Frequency Drift With Temperature (Mean and SD)

Figure 10.

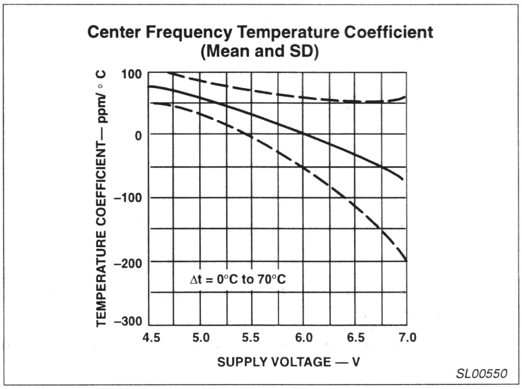

Center Frequency Temperature Coefficient (Mean and SD)

Figure 13.

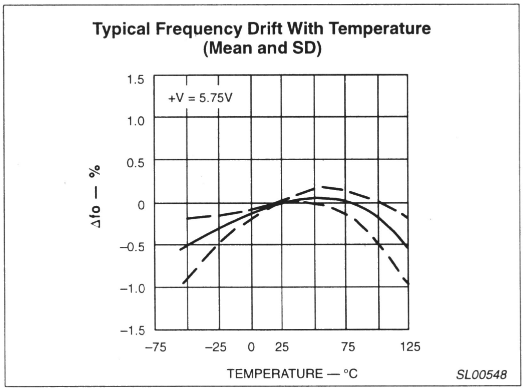

Typical Frequency Drift With Temperature (Mean and SD)

Figure 11.

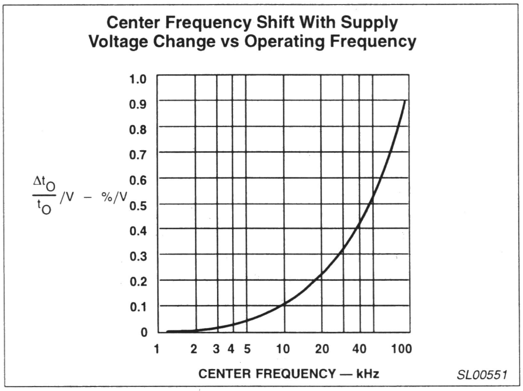

Center Frequency Shift With Supply Voltage Change vs Operating Frequency

Figure 14.

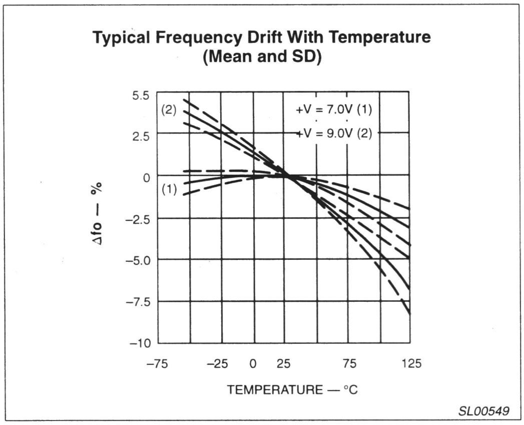

Typical Frequency Drift With Temperature (Mean and SD)

Figure 12.

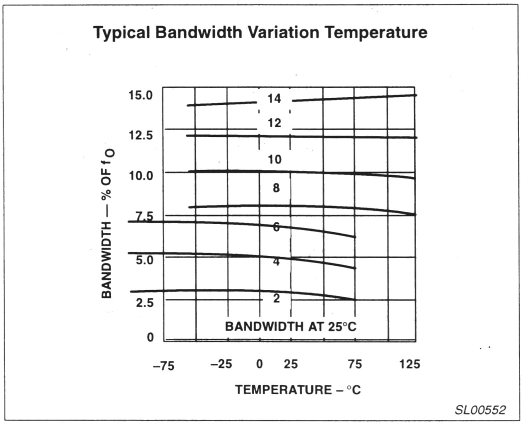

Typical Bandwidth Variation Temperature

Figure 15.

DESIGN FORMULAS

$$f_O \approx \frac{1}{1.1 R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_I}{f_O C_2}} \text{ in \% of } f_O$$

$$V_I \leq 200mV_{RMS}$$

Where

V_I=Input voltage (V_{RMS})

C_2=Low-pass filter capacitor (µF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

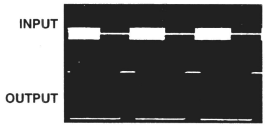
A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 17 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

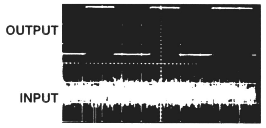
1. Select R1 and C1 for the desired center frequency. For best temperature stability, R1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R1C1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of $f_O \cdot C_2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above $200mV_{RMS}$. The bandwidth, as noted on the graph, is then controlled solely by the $f_O \cdot C_2$ product (f_O (Hz), C2(µF)).

TYPICAL RESPONSE



NOTE:
$R_L = 100\Omega$

Response to $100mV_{RMS}$ Tone Burst



NOTES:
S/N = –6dB
$R_L = 100\Omega$
Noise Bandwidth = 140Hz

Response to Same Input Tone Burst With Wideband Noise

SL00553

Figure 16. Typical Response

3. The value of C3 is generally non-critical. C3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

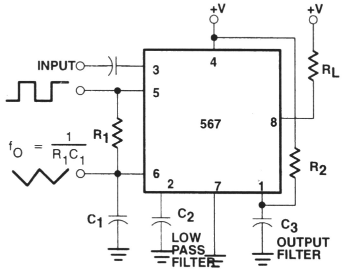


Figure 17.

4. Optional resistor R2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of $10mV_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

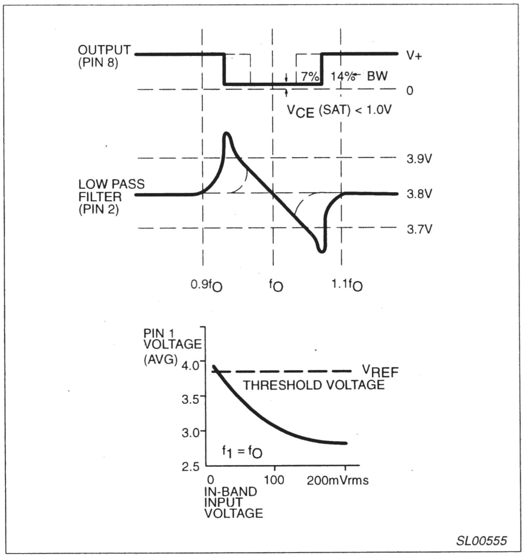


Figure 18. Typical Output Response

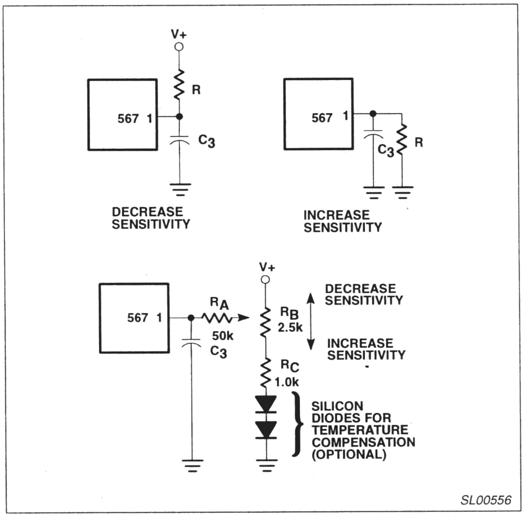


Figure 19. Sensitivity Adjust

AVAILABLE OUTPUTS (Figure 17)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V\ -2V_{BE}) \cong (+V-1.4V)$ having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_O/3$, $f_O/5$, etc.
2. The 567 will lock onto signals near (2n+1) f_O, and will give an output for signals near (4n+1) f_O where n=0, 1, 2, etc. Thus, signals at $5f_O$ and $9f_O$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below $200mV_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

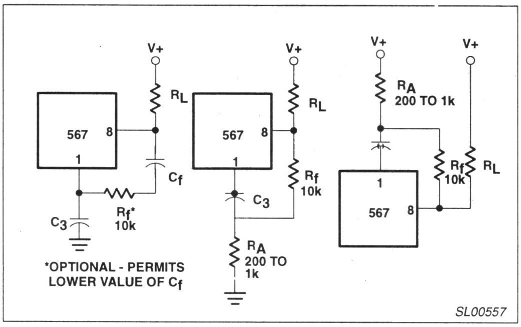

V+
V+
V+
V+
567
8
1
RL
Cf
Rf*
10k
C3
*OPTIONAL - PERMITS LOWER VALUE OF Cf
567
8
1
RL
Rf
10k
C3
RA
200 TO 1k
RA
200 TO 1k
Rf
10k
RL
1
567
8
SL00557

Figure 20. Chatter Prevention

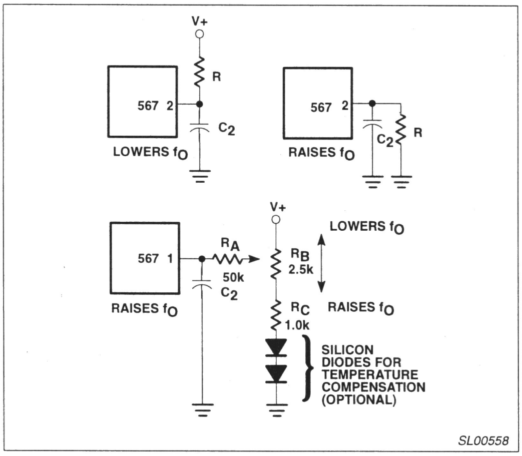

V+
567 2
R
C2
LOWERS fO
567 2
C2
R
RAISES fO
V+
LOWERS fO
567 1
RA
50k
C2
RB
2.5k
RAISES fO
RC
1.0k
RAISES fO
SILICON DIODES FOR TEMPERATURE COMPENSATION (OPTIONAL)
SL00558

Figure 21. Skew Adjust

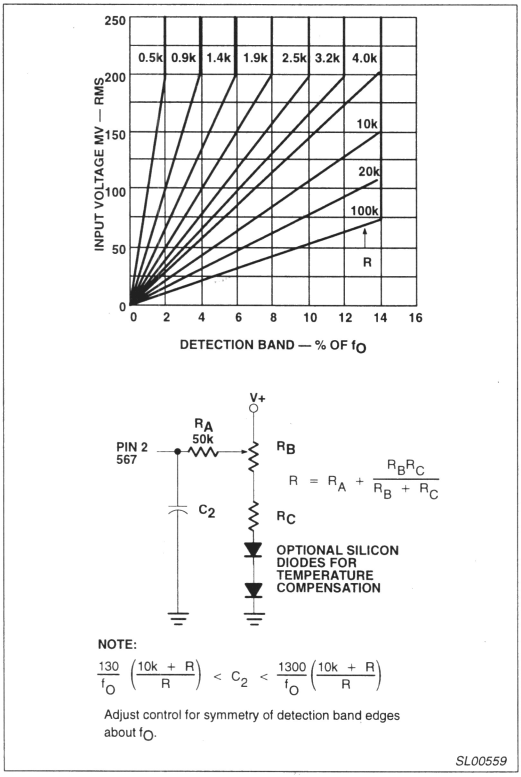
$$C_2 = \frac{130}{f_O}\ \mu F$$

$$C_3 = \frac{260}{f_O}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 19)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.



$$R = R_A + \frac{R_B R_C}{R_B + R_C}$$

NOTE:

$$\frac{130}{f_O}\left(\frac{10k + R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k + R}{R}\right)$$

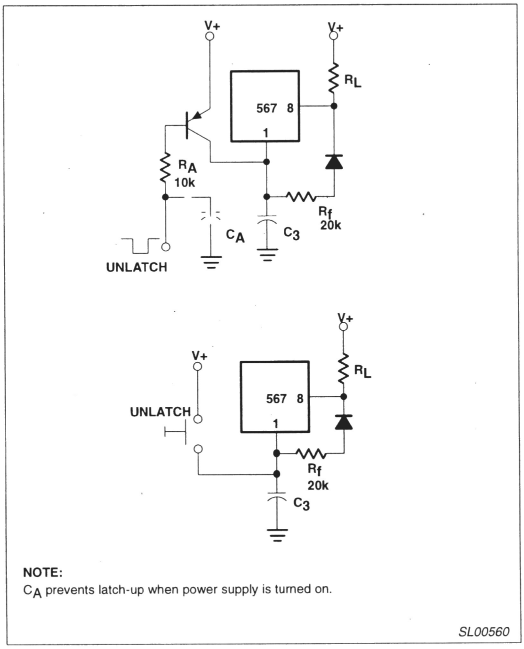
Adjust control for symmetry of detection band edges about f_O.

Figure 22. BW Reduction

SENSITIVITY ADJUSTMENT (Figure 19)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must



NOTE:
C_A prevents latch-up when power supply is turned on.

Figure 23. Output Latching

CHATTER PREVENTION (Figure 20)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 20. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT (Figure 21)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION (Figure 22)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff
frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 23)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

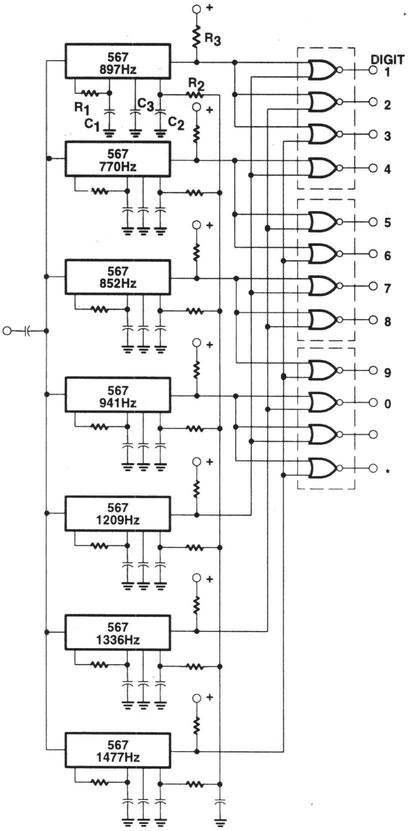
REDUCTION OF C1 VALUE

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.

TYPICAL APPLICATIONS


+
R_3
567
897Hz
R_2
R_1
C_1
C_3
C_2
567
770Hz
567
852Hz
567
941Hz
567
1209Hz
567
1336Hz
567
1477Hz
DIGIT
1
2
3
4
5
6
7
8
9
0
*

NOTES:

Component values (Typical)

R_1 = 26.8 to 15kΩ

R_2 = 24.7kΩ

R_3 = 20kΩ

C_1 = 0.10mF

C_2 = 1.0mF 5V

C_3 = 2.2mF 6V

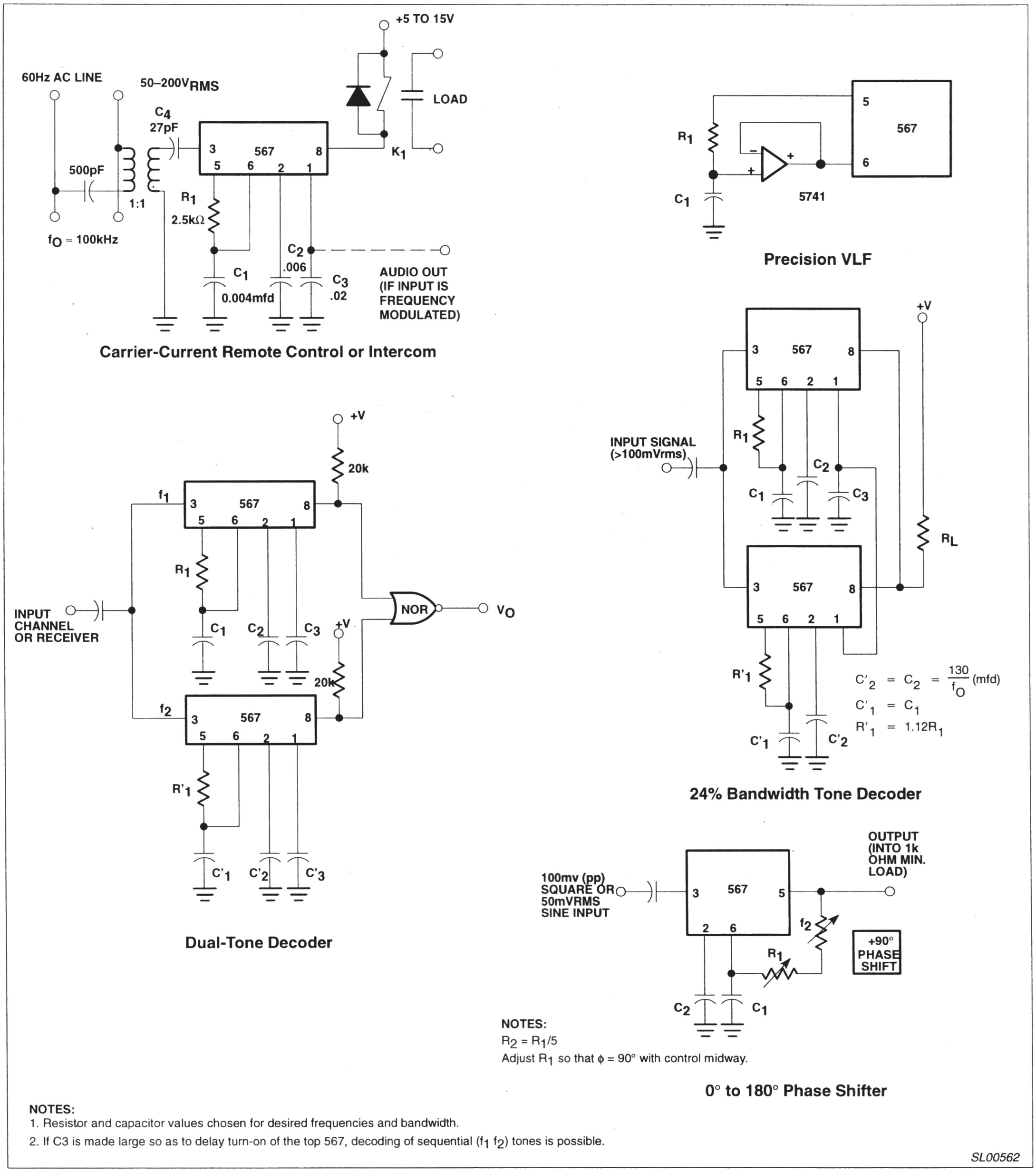
C_4 = 250µF 6V

Touch-Tone® Decoder

SL00561

Figure 24. Typical Applications

TYPICAL APPLICATIONS (Continued)


+5 TO 15V
60Hz AC LINE
50–200VRMS
C4
27pF
500pF
1:1
fO ≈ 100kHz
567
3
8
5
6
2
1
R1
2.5kΩ
C1
0.004mfd
C2
.006
C3
.02
LOAD
K1
AUDIO OUT
(IF INPUT IS
FREQUENCY
MODULATED)
R1
C1
5741
567
5
6
+V
20k
f1
f2
NOR
VO
INPUT
CHANNEL
OR RECEIVER
R'1
C'1
C'2
C'3
20k
INPUT SIGNAL
(>100mVrms)
RL
C'2 = C2 = 130/fO (mfd)
C'1 = C1
R'1 = 1.12R1
100mv (pp)
SQUARE OR
50mVRMS
SINE INPUT
OUTPUT
(INTO 1k
OHM MIN.
LOAD)
f2
+90°
PHASE
SHIFT
SL00562

Carrier-Current Remote Control or Intercom

Precision VLF

24% Bandwidth Tone Decoder

Dual-Tone Decoder

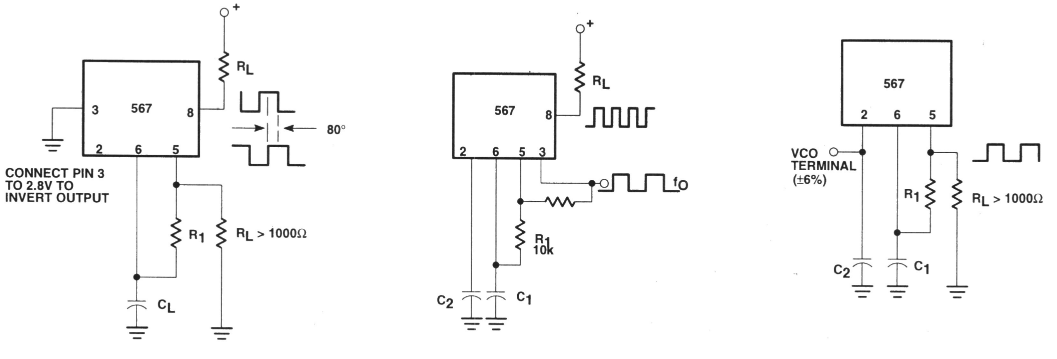
NOTES:
$R_2 = R_1/5$
Adjust R_1 so that ϕ = 90° with control midway.

0° to 180° Phase Shifter

NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

Figure 25. Typical Applications (cont.)

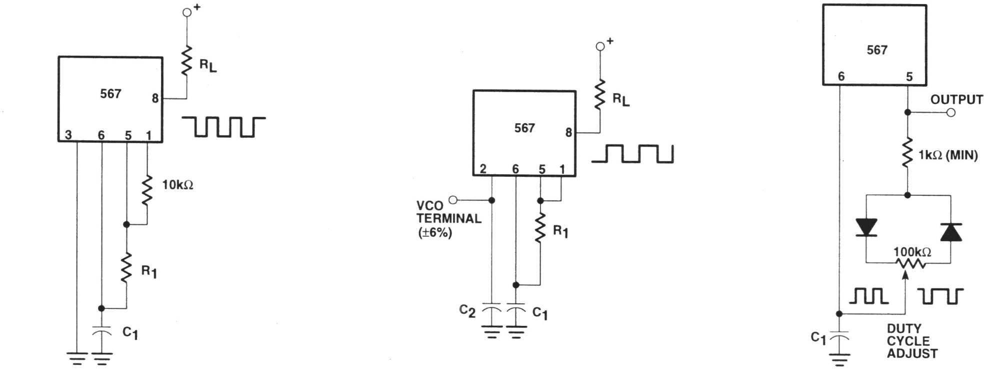
TYPICAL APPLICATIONS (Continued)


+
R_L
3
567
8
2
6
5
80°
CONNECT PIN 3
TO 2.8V TO
INVERT OUTPUT
R1
RL > 1000Ω
CL
+
RL
567
8
2
6
5
3
fo
R1
10k
C2
C1
567
2
6
5
VCO
TERMINAL
(±6%)
R1
RL > 1000Ω
C2
C1

Oscillator With Quadrature Output

Oscillator With Double Frequency Output

Precision Oscillator With 20ns Switching


+
RL
567
8
3
6
5
1
10kΩ
R1
C1
+
RL
567
8
2
6
5
1
VCO
TERMINAL
(±6%)
R1
C2
C1
567
6
5
OUTPUT
1kΩ (MIN)
100kΩ
C1
DUTY
CYCLE
ADJUST

Pulse Generator With 25% Duty Cycle

Precision Oscillator to Switch 100mA Loads

Pulse Generator

SL00563

Figure 26. Typical Applications (cont.)

Call progress decoder NE5900

DESCRIPTION

The NE5900 call progress decoder (CPD) is a low cost, low power CMOS integrated circuit designed to interface with a microprocessor-controlled smart telephone capable of making preprogrammed telephone calls. The call progress decoder information to permit microprocessor decisions whether to initiate, continue, or terminate calls. A tri-state, 3-bit output code indicates the presence of dial tone, audible ring-back, busy signal, or re-order tones.

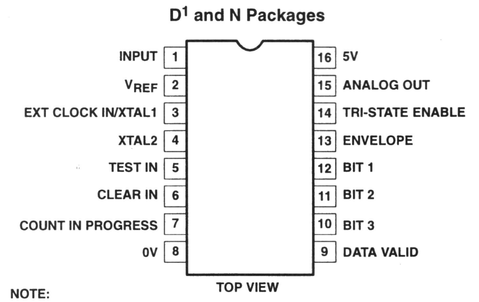
A front-end bandpass filter is accomplished with switched capacitors. The bandshaped signal is detected and the cadence is measured prior to output decoding. In addition to the three data bits, a buffered bandpass output and envelope output are available. All logic inputs and outputs can interface with LSTTL, CMOS and NMOS.

Circuit features include low power consumption and easy application. Few and inexpensive external components are required. A typical application requires a 3.58MHz crystal or clock, 470kΩ resistor, and two bypass capacitors. The NE5900 is effective where traditional call progress tones, PBX tones, and precision call progress tones must be correctly interpreted with a single circuit.

FEATURES

- Fully decoded tri-state call progress status output
- Works with traditional, precision, or PBX call progress tones
- Low power consumption
- Low cost 3.58MHz crystal or clock
- No calibration or adjustment
- Interfaces with LSTLL, CMOS, NMOS
- Easy application

PIN CONFIGURATION



NOTE:
1. SOL — Released in large SO package only.

SR01142

Figure 1. Pin Configuration

APPLICATIONS

- Modems
- PBXs
- Security equipment
- Auto dialers
- Answering machines
- Remote diagnostics
- Pay telephones

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SOL) Package	0 to +70°C	NE5900DK	SOT162-1
16-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5900N	SOT38-4

BLOCK DIAGRAM

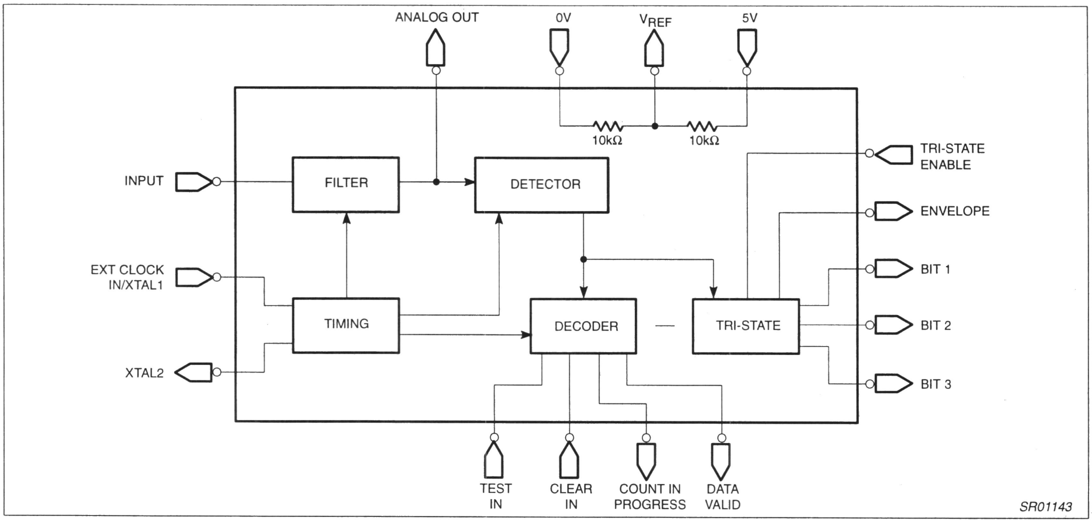

ANALOG OUT
0V
V_{REF}
5V
10kΩ
10kΩ
INPUT
FILTER
DETECTOR
TRI-STATE ENABLE
ENVELOPE
EXT CLOCK IN/XTAL1
TIMING
DECODER
TRI-STATE
BIT 1
BIT 2
BIT 3
XTAL2
TEST IN
CLEAR IN
COUNT IN PROGRESS
DATA VALID
SR01143

Figure 2. NE5900 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	9	V
V_{IN}	Logic control input voltages	-0.3 to +16	V
V_{IN}	All other input voltages[1]	-0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltages	-0.3 to V_{CC} + 0.3	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10s)	+300	°C
T_{JMAX}	Junction temperature	+150	°C

NOTE:

1. Includes Pin 3 — Ext Clock In

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{DD}	Power supply voltage	Pin 16 Pin 14 = V_{DD} Pin 5, 6 = 0V	4.5	5.0	5.5	V
	Quiescent current	As above with no output loads		2.0	4.0	mA
	Input threshold	Pin 1 level, frequency = 460Hz, V_{DD} = V_{REF} Output Pin 13 = V_{DD}		-39	-35	dB[1]
	Signal rejection	Pin 1 level, frequency = 300Hz, V_{DD} = V_{REF} Output Pin 13 = 0V			-50	dB[1]
	Low frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V			180	Hz
	High frequency[2] rejection	Pin 1 frequency, 0dB max., V_{DC} = V_{REF} Output Pin 13 = 0V	800			Hz
V_{IH}	Logic 1 level	Pins 6, 14	2.0		15	V
V_{IL}	Logic 0 level	Pins 6, 14	0		0.8	V
I_{IH}	Logic 1 input current	Pins 3, 6, 14 = V_{DD}	-1.0		1.0	µA
I_{IL}	Logic 0 input current	Pins 3, 6, 14 = 0V	-1.0		1.0	µA
V_{IH}	Logic 1 input voltage	Pin 3 External Clock In/XTAL	V_{DD} – 1		V_{DD}	V
V_{IL}	Logic 0 input voltage	Pin 3 External Clock In/XTAL	0		1.0	V
V_{OL}	Logic 0 output voltage	I_{SINK} = 1.6mA Pins 7, 9, 10, 11, 12, 13	0		0.4	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 0.5mA Pins 7, 9, 10, 11, 12, 13	V_{DD} – 0.4		V_{DD}	V
I_{OZ}	Tri-state leakage	V_{OUT} = V_{DD} or 0V Pins 10, 11, 12, 13, Pin 14 = 0V	-3.0		3.0	µA
	Filter output gain	Input Pin 1, 460Hz – 20dB, V_{DC} = V_{REF} Output Pin 15, R_{LOAD} = 1MΩ	6.5	8.5	10.5	dB
	Filter frequency response	As above from 300Hz to 630Hz, referenced to 460Hz	-1.0		1.0	dBmo
	Input impedance	Pin 1, frequency = 460MHz	1			MΩ
V_{REF}	Reference voltage	Pin 2, V_{DD} = 5V	2.4	2.5	2.6	V
R_{REF}	Reference resistance	Pin 2		5		Ω
	Envelope response time	Time from removal or application of 460Hz – 20dB (V_{DC} = V_{REF} on Pin 1) to response of Pin 13		38		ms

NOTE:

1. 0dB = 0.775V_{RMS}
2. By design; not tested.

The NE5900 uses the signal in the call progress tone passband and the cadence of interrupt rate of the signal to determine which call progress tone is present.

Figure 3 shows a detailed block diagram of the NE5900.

The signal input from the phone line is coupled through a 470kΩ resistor which, together with two internal capacitors and an internal resistor, form an anti-aliasing filter. This passive low pass filter strongly rejects AM radio interference. Insertion loss is typically 1.5dB at 460Hz. The 470kΩ resistor also provides protection from the transients. The input (Pin 1) DC voltage can be derived from V_{REF} (Pin 2) or allowed to self-bias through a series coupling capacitor (10nF minimum).

Following this is a switched capacitor bandpass filter which accepts call progress tones and inhibits tones not in the call progress band of 300Hz to 630Hz. The bandpass limits are determined by the input clock frequency of 3.58MHz. An on-board inverter between Pins 3 and 4 can be used either as a crystal oscillator or as a buffer for an external 3.58MHz clock signal. The switched capacitor filters provide typical rejection of greater than 40dB for frequencies below 120Hz and above 1.6kHz.

The decoder responds to signals between 300Hz and 630Hz with a threshold of -39dB typical (0dB = 0.775V_{RMS}). The decoder will not respond to any signal below -50dB or to tones up to 0dB which are below 180Hz or above 800Hz. Dropouts of 20ms or bursts of only 20ms duration are ignored. A gap of 40ms or a valid tone of 40ms is detected.

The buffered output of the switched capacitor filter is available at the analog output, Pin 15. A logic output representing the detected envelope of this signal is available at the envelope output, Pin 13.

At the start of an in-band tone (envelope output goes high), a 2.3 second interval is timed out. Transitions of the envelope during this interval are counted to determine the signal present. At 2.3 seconds, the three bits of data representing this decision are stored in the latch and appear at the outputs. A data valid signal goes high at this time, signaling that the data bits, Pins 10 – 12, can be read.

The output code is as follows:

	Pin 12	Pin 11	Pin 10
Dial Tone	0	0	0
Ringing Signal	1	0	0
Busy Signal	0	1	0
Re-order Tone	0	0	1
Overflow	1	1	1

The overflow condition occurs in the event that too many transitions occur during the 2.3 second interval. This can result from noise, voice, or other line disturbances not normally present during the post-dialing interval. Note that the end of dial tone in interpreted as a valid ringing signal.

The clear input resets all internal registers and the output latch, and is to be set low after the completion of dialing. The clear input should be pulsed high for proper operation. Recommended pulse width is between 0.2μs and 20ms. If clear is held high when envelope is high, a false output pulse (Pin 13) can result when clear is returned low.

For applications where dialing is done by a person rather than by a microprocessor, an uncertainty exists about the number of digits to be dialed (local vs long distance). In such situations it is possible to clear the NE5900 by application of the DTMF signal or dial pulses to the clear pin (Pin 6). When dialing is complete, the device is cleared and ready to respond to the next call progress unit.

Enable is held at 5V to enable Pins 10, 11, 12 and 13. When enable is brought low, data valid is also set low. Enable must remain high while the data is also set low. Enable must remain high while the data is being read. The test pin is for production test only and must be kept low in all user applications.

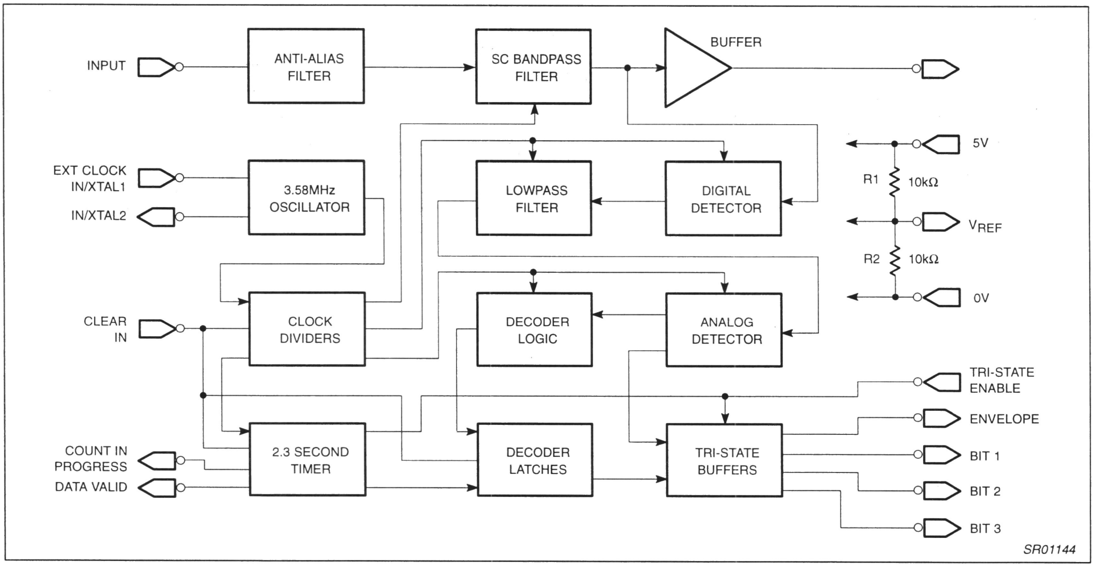


Figure 3. Detailed Block Diagram CPD

Figure 4 shows a typical application of the call progress decoder.

In this application only one external component is needed an no microprocessor activity other than clear is required.

Figure 5 shows the recommended direct interface to the telephone line. Bus connection is possible by utilizing tri-state, and internal timing is accomplished with a 3.58MHz crystal.

The designer can utilize the input signal, clock, bus, or microprocessor interface which best serves the application. Figure 6 gives a typical timing diagram for the application of Figures 4 and 5.

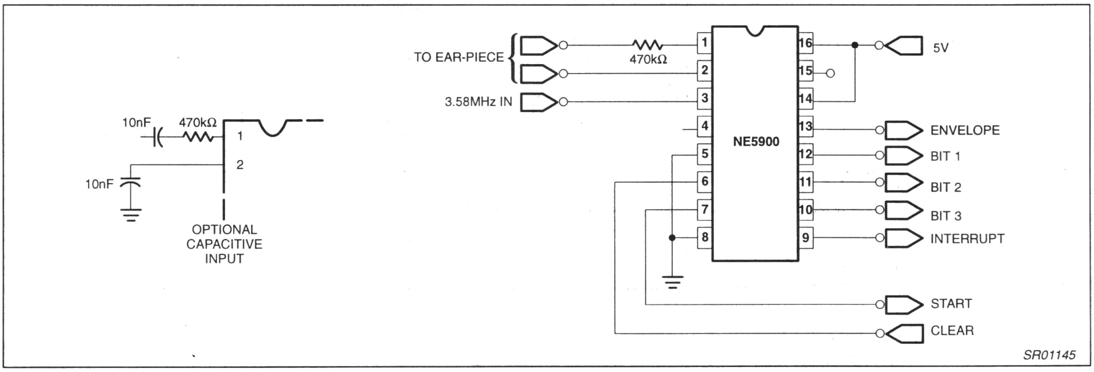

10nF
470kΩ
1
2
10nF
OPTIONAL CAPACITIVE INPUT
TO EAR-PIECE
3.58MHz IN
470kΩ
NE5900
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
5V
ENVELOPE
BIT 1
BIT 2
BIT 3
INTERRUPT
START
CLEAR
SR01145

Figure 4. Typical Application

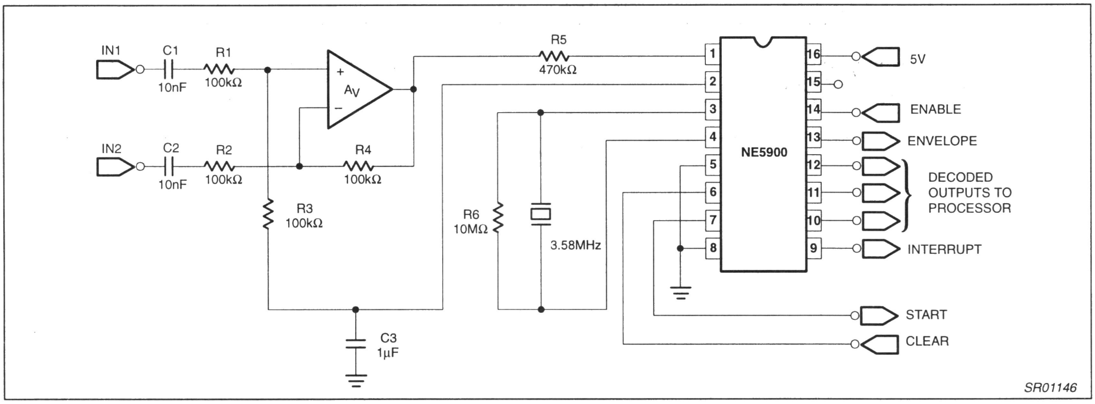

IN1
C1
10nF
R1
100kΩ
IN2
C2
10nF
R2
100kΩ
+
AV
–
R4
100kΩ
R3
100kΩ
R5
470kΩ
R6
10MΩ
3.58MHz
C3
1μF
NE5900
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
5V
ENABLE
ENVELOPE
DECODED OUTPUTS TO PROCESSOR
INTERRUPT
START
CLEAR
SR01146

Figure 5. Typical Two-Wire Application

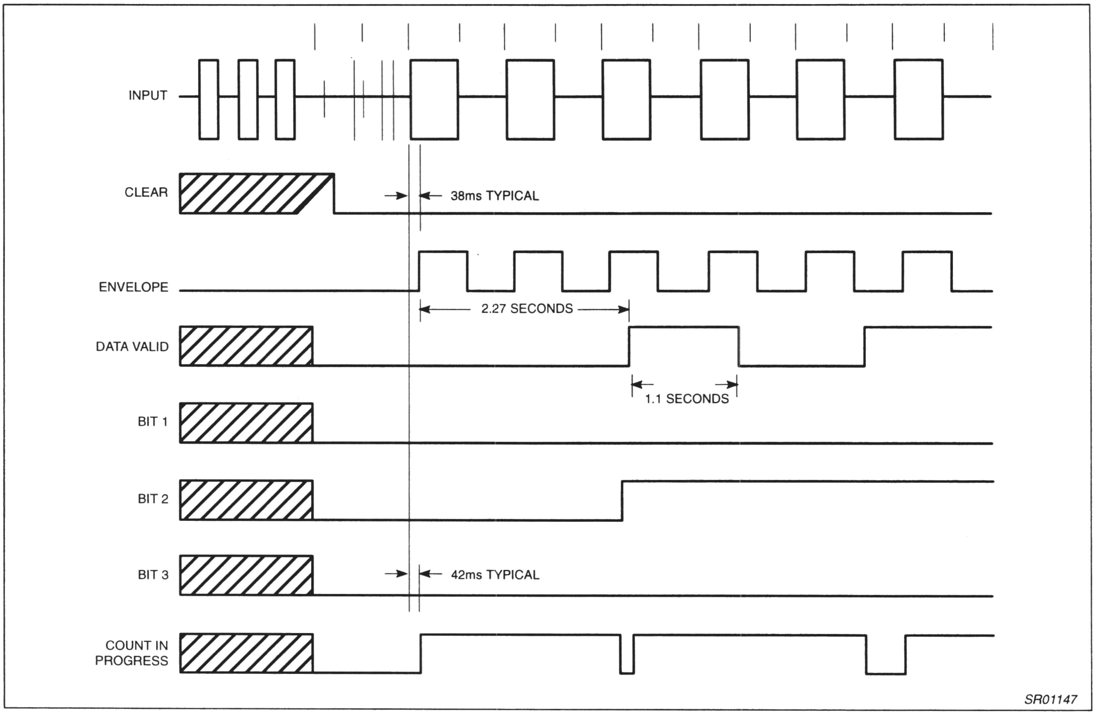

INPUT
CLEAR
38ms TYPICAL
ENVELOPE
2.27 SECONDS
DATA VALID
1.1 SECONDS
BIT 1
BIT 2
BIT 3
42ms TYPICAL
COUNT IN PROGRESS
SR01147

Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS

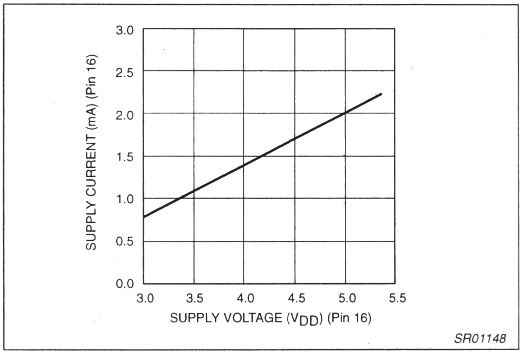


Figure 7. Power Supply Current vs V_{DD}

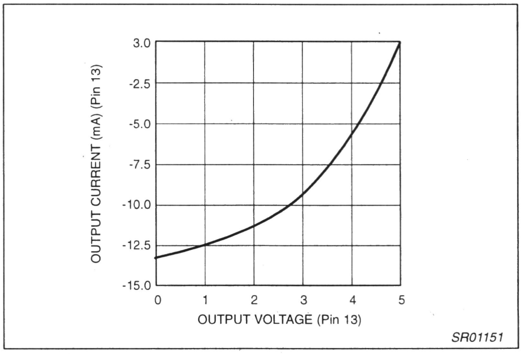


Figure 10. Output Voltage Current Curve Digital Output High

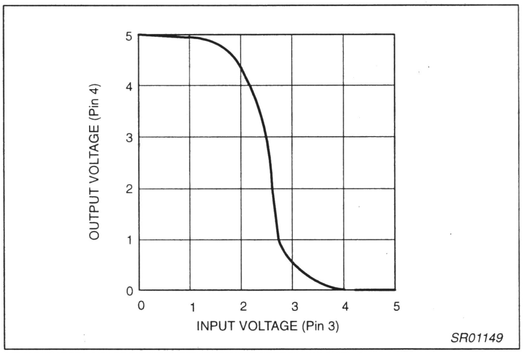


Figure 8. Voltage Transfer Curve

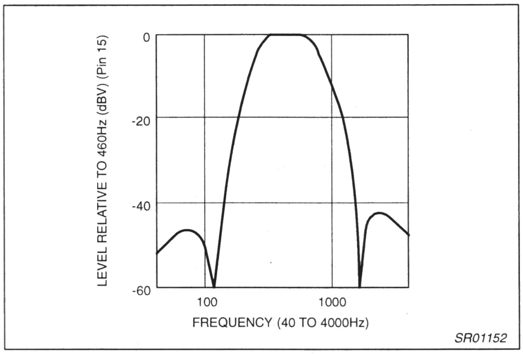


Figure 11. Filter Frequency Response

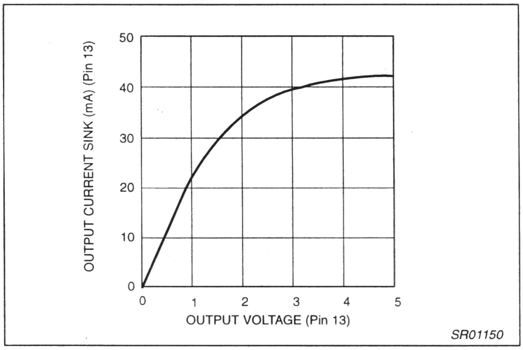


Figure 9. Digital Output Low

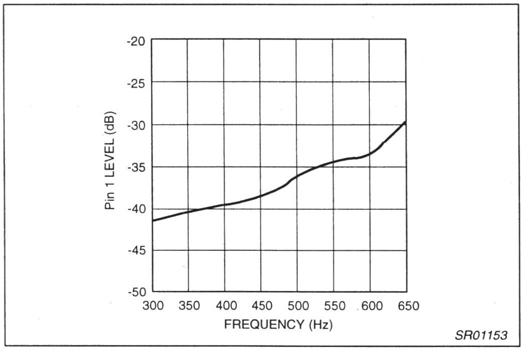


Figure 12. Typical Threshold

Multistandard Programmable Analog CMOS Transmission IC

PCA1070

FEATURES

- Line interface with:
  - Voltage regulator with programmable DC voltage drop
  - Programmable set impedance
  - Output to control an external switching MOS transistor for pulse dialling
  - Programmable DC voltage during pulse dialling
  - Circuitry for short DC settling time
- Interface to peripheral circuits with:
  - Supply for microcontroller and DTMF diallers
  - Input to sense supply voltage of microcontroller and output for reset of microcontroller
  - I^{2}C-bus (programming of parameters, control of all logic signals)
  - High impedance DTMF signal input
  - Input for external oscillator signal with on-chip DC blocking
  - Power-down via I^{2}C-bus
  - Stabilized supply for electret microphone
- Microphone and DTMF amplifiers:
  - Low-noise microphone preamplifier suitable for various types of microphones
  - Symmetrical high impedance microphone preamplifier inputs
  - Programmable gain for microphone and DTMF channels
  - Sending mute via I^{2}C-bus to disable microphone amplifier and enable DTMF amplifier
  - Sending mute also to be used as privacy switch
  - Dynamic limiting (speech controlled) to prevent distortion of line signal and sidetone; programmable maximum sending level
- Receive amplifier:
  - Suitable for various types of earpieces (including piezo)
  - Programmable gain and hearing protection level
  - Receive mute via I^{2}C-bus to disable receive amplifier and enable DTMF confidence tone
  - On-chip anti-sidetone circuit with programmable sidetone balance
  - Confidence tone in the earpiece during DTMF dialling
- Facility to regulate parameters with line current:
  - Value of DC line current (bit code) readable via I^{2}C-bus
  - Line loss compensation with fully software programmable characteristics (control range, stop current) of microphone/earpiece/DTMF amplifiers
  - Fully software programmable control of sidetone balance and DC voltage drop as a function of line length.

APPLICATIONS

- Wired telephony (basic till feature phones)
- Combi-terminals (e.g. telephone and answering machine or FAX)
- Modems and base units of cordless telephones.

GENERAL DESCRIPTION

The PCA1070 is a CMOS integrated circuit performing all speech and line interface functions in fully electronic telephone sets. The device requires a minimum of external components. The transmission parameters are programmable via the I^{2}C-bus. This makes the IC adaptable to nearly all worldwide country requirements and to a various range of speech transducers, without changing the (few) external components.

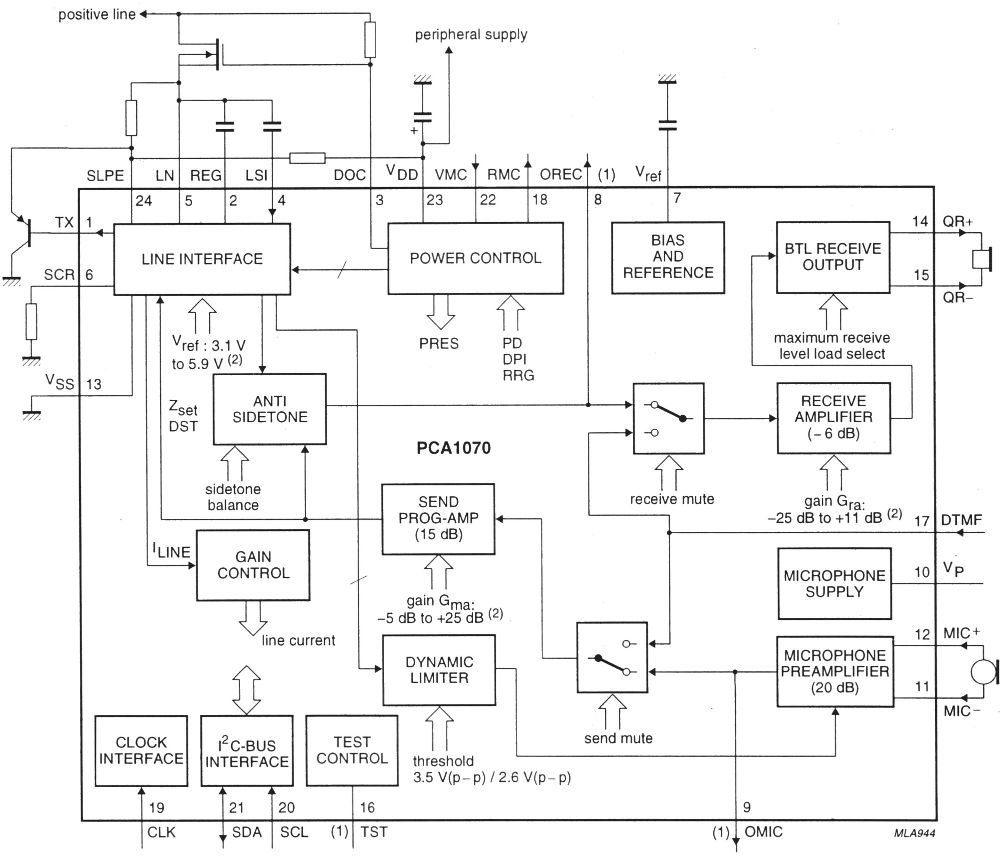
The parameters are stored in the EEPROM of a microcontroller and are loaded into the PCA1070 during the start-up phase of the transmission IC after hook-off.

The PCA1070 also allows adaptation to the connected telephone line by reading the line current via the I^{2}C-bus and processing it in the microcontroller.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA1070P	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
PCA1070T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM


positive line
peripheral supply
+
SLPE
LN
REG
LSI
DOC
VDD
VMC
RMC
OREC
(1)
Vref
24
5
2
4
3
23
22
18
8
7
TX
1
SCR
6
VSS
13
LINE INTERFACE
POWER CONTROL
BIAS AND REFERENCE
BTL RECEIVE OUTPUT
14
QR+
15
QR−
PRES
PD
DPI
RRG
Vref : 3.1 V to 5.9 V (2)
maximum receive level load select
Zset
DST
ANTI SIDETONE
PCA1070
RECEIVE AMPLIFIER (− 6 dB)
sidetone balance
receive mute
gain Gra: −25 dB to +11 dB (2)
17
DTMF
SEND PROG-AMP (15 dB)
ILINE
GAIN CONTROL
MICROPHONE SUPPLY
10
VP
gain Gma: −5 dB to +25 dB (2)
12
MIC+
line current
DYNAMIC LIMITER
MICROPHONE PREAMPLIFIER (20 dB)
11
MIC−
send mute
CLOCK INTERFACE
I2C-BUS INTERFACE
TEST CONTROL
threshold 3.5 V(p−p) / 2.6 V(p−p)
19
21
20
16
9
CLK
SDA
SCL
(1)
TST
(1)
OMIC
MLA944

(1) Test pins.

(2) Default value.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TX	1	drive output
REG	2	voltage regulator decoupling
DOC	3	dial output connection
LSI	4	line signal input
LN	5	positive line terminal
SCR	6	sending current resistor
V_{ref}	7	voltage reference decoupling
OREC	8	output receive preamplifier; to be left open-circuit in application
OMIC	9	output microphone preamplifier; to be left open-circuit in application
V_P	10	supply for electret microphones
MIC−	11	inverting input microphone preamplifier
MIC+	12	non-inverting input microphone preamplifier
V_{SS}	13	negative line terminal
QR+	14	non-inverting output for receiving output amplifier
QR−	15	inverting output for receiving output amplifier
TST	16	test pin; to be connected to V_{SS} in application
DTMF	17	dual tone multi-frequency input
RMC	18	reset output for microcontroller
CLK	19	clock signal input
SCL	20	serial clock line input; I^2C-bus
SDA	21	serial data line input/output; I^2C-bus
VMC	22	input to sense supply voltage microcontroller
V_{DD}	23	positive supply decoupling
SLPE	24	slope (DC resistance) adjustment

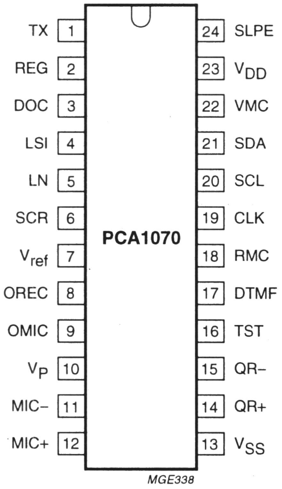

TX 1
REG 2
DOC 3
LSI 4
LN 5
SCR 6
Vref 7
OREC 8
OMIC 9
VP 10
MIC− 11
MIC+ 12
PCA1070
24 SLPE
23 VDD
22 VMC
21 SDA
20 SCL
19 CLK
18 RMC
17 DTMF
16 TST
15 QR−
14 QR+
13 VSS
MGE338

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Line interface

DC VOLTAGE DROP

Power for the PCA1070 and its peripheral circuits is obtained from the telephone line. The IC develops its own supply voltage at V_{DD} and regulates its DC voltage drop between pins SLPE and V_{SS}. The DC voltage V_{SLPE} can be programmed via the I^2C-bus interface between 3.1 to 5.9 V and is default at 4.7 V (see Table 1).

The DC line voltage at pin LN can be calculated using the following equation:

$$V_{LN} = V_{SLPE} + (I_{line} - I_{LN}) \times R_{LN\text{-}SLPE}$$

where

I_{LN} = DC bias current flowing into pin LN ($\approx$ 3 mA if $I_{line} > 17$ mA)

$R_{LN\text{-}SLPE}$ = external 20 Ω resistor between LN and SLPE.

At line currents below 6 mA (typ.) the DC voltage V_{SLPE} is automatically adjusted to a lower value. This means that the operation of more sets, connected in parallel, is possible with reduced sending and receiving levels and relaxed performance. At line currents below 16 mA (typ.) (17 mA max.) the DC bias current I_{LN} is reduced from ≈ 3 mA to a lower value to ensure maximum possible transmit level capability under all line current conditions.

SET IMPEDANCE

In normal conditions $I_{line} \geq I_{LN}$ and the static behaviour is equivalent to a voltage regulator diode with a series resistor $R_{LN\text{-}SLPE}$ (fixed value 20 Ω). In the audio frequency range the dynamic impedance Z_{LN} is determined mainly by internal components $Z_S = R_a + (R_b//C)$. The equivalent impedance Z_{LN} is shown in Fig.3. The values of R_a, R_b and C can be programmed via the I^2C-bus interface (see Tables 9, 10 and 11).

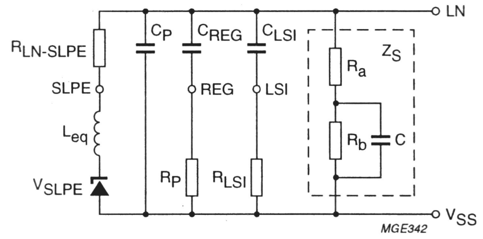


Fig.3 Equivalent impedance Z_{LN}.

Where:

R_P = internal resistor [1 075 kΩ (typ.) with V_{SLPE} = 4.7 V]

R_{LSI} = internal resistor (240 kΩ typ.)

C_{REG} = capacitor at pin REG (470 nF)

$L_{eq} = R_P \times R_{LN\text{-}SLPE} \times C_{REG}$ = 10.1 H (typ.) with V_{SLPE} = 4.7 V (artificial inductor)

C_{LSI} = capacitor at pin LSI (100 nF)

C_P = internal capacitor (12 nF typ.).

SUPPLY FOR PERIPHERAL CIRCUITS

The supply voltage V_{DD} can be used for peripheral circuitry. The supply capabilities depend on the programmed DC voltage drop V_{SLPE} and on several other parameters as given in the following equation:

$$V_{DD} = V_{SLPE} - (I_{DD} + I_p + I_{VP}) \times R_{SLPE-VDD}$$

where

I_{DD} = internal current consumption PCA1070 (2.3 mA typ.)

I_p = current to peripheral circuitry

I_{VP} = current taken from V_P for electret microphone

$R_{SLPE-VDD}$ = external resistor between SLPE and V_{DD} (250 Ω).

DC STARTING AND SETTLING TIME

The IC is equipped with circuitry for fast DC start-up. This circuit is automatically activated as soon as V_{DD} reaches 3 V (typ.) after hook-off, and is deactivated when V_{SLPE} drops below 5.9 V (typ.). This ensures that only a relatively short time is needed to reach the default DC setting (V_{SLPE}) of the circuit and that V_{DD} will not exceed the maximum permitted voltage of 6 V.

The start-up circuit can also be activated under software control by setting bit code DST to logic 1 via the I^2C-bus. The start-up time can be optimized by programming the bit code DST to logic 1 during the start-up procedure. In practice this is possible as soon as the microcontroller has become operational. The DST bit can also be used to quickly restore the DC settings (V_{SLPE}) after long line breaks or during reprogramming of the DC voltage drop V_{SLPE}.

It should be noted that the AC impedance into pin LN is reduced considerably when DST = 1.

Power control

INTERNAL RESET PCA1070

The PCA1070 has an internal reset circuit that monitors the supply voltage V_{DD}. If V_{DD} is below the threshold level (V_{DD} = 1.2 V ±0.2 V) then the circuit is in reset-mode. In the reset mode the current consumption is low and the internal reset is active and writes the default values into all registers. The status bit PRES will also be set to logic 1. The microcontroller can read this bit via the I^2C-bus interface; once read it will be set to logic 0 again.

When V_{DD} passes the threshold (increasing V_{DD}), the circuit becomes partly active and the internal ring/speech detector will be activated (see Section "Start-up and switch-off behaviour").

RESET OUTPUT FOR MICROCONTROLLER

The voltage at pin VMC (microcontroller supply voltage) is monitored by a reset circuit. If VMC is below the threshold level the output RMC is set to logic 1.

The threshold level in the normal operating mode and in the power-down mode is 2 V ±0.2 V (2.1 V ±0.3 V in standby mode).

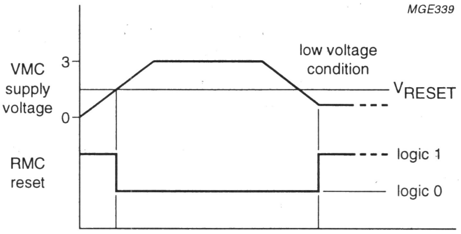


Fig.4 VMC timing diagram.

POWER-DOWN/STANDBY MODES

The circuit can be set in power-down mode or in standby mode. These modes are intended for use with pulse dialling, during long line breaks, and applications with memory retention.

With control bits PDx = 01, the circuit is in the power-down mode; the current consumption at pin V_{DD} is reduced from I_{DD} = 2.3 mA (typ.) to <100 μA (typ.); the current consumption at pin VMC is 4 μA (typ.)(<10 μA). When PDx = 11 the circuit goes into the standby mode and I_{DD} = < 5 μA, I_{VMC} is reduced from 4 μA (typ.) to 2 μA (typ.)(< 5 μA). In both conditions (power-down and standby) the voltage stabilizer will be disabled.

START-UP AND SWITCH-OFF BEHAVIOUR

This description refers to the basic application where V_{DD} and VMC are connected together and one supply capacitor is used (see Fig.8).

Speech condition

After hook-off, line current will be applied to the line input LN. The supply capacitor connected to V_{DD} and VMC will be charged.

The internal reset signal will change from logic 1 to logic 0 when V_{DD} passes the threshold level (1.2 V ±0.2 V) and the circuit becomes partly active [the line interface part is kept in power-down mode, so that all of the line current is available to charge the supply capacitor(s)];

PCA1070 can receive data via the I^2C-bus (standard I^2C specifications are fulfilled for $V_{DD} \geq 2.5$ V; for $V_{DD} = 1.8$ to 2.5 V relaxed performance).

When VMC passes the microcontroller reset level 2 V ±0.2 V (2.1 V ±0.3 V in standby mode) the output RMC changes from logic 1 to logic 0 and the circuit is switched to the normal operating mode.

Hook-on

By decreasing VMC the output RMC will change from logic 0 to logic 1 when VMC passes the threshold level 2 V ±0.2 V (2.1 V ±0.3 V in standby mode), however the PCA1070 will stay in the normal operating mode until the internal reset takes place.

By decreasing V_{DD} the internal reset signal will change from logic 0 to logic 1 when V_{DD} passes the threshold (1.2 V ±0.2 V) and the circuit will go into the reset mode (line interface part in power-down and all programmable parameters are reset to default values).

Ringer condition

In this condition the supply capacitor connected to V_{DD} and VMC is charged by the ringer signal; no line current is applied to pin LN.

V_{DD} and VMC are increasing and when V_{DD} passes the internal reset threshold (1.2 V ±0.2 V), the internal ring/speech-detector will be activated and the circuit will switch to the standby condition ($I_{DD} < 5\ \mu A$; $I_{VMC} < 5\ \mu A$) before the voltage at VMC reaches the threshold level for microcontroller reset. When VMC passes this threshold level (2.1 V ±0.3 V) output RMC changes from logic 1 to logic 0 and the circuit will stay in the stand-by mode until line current is applied to pin LN. By setting the 'Reset RinG' control bit (RRG) to logic 1 via the I^2C-bus interface, the ring/speech detector will be disabled.

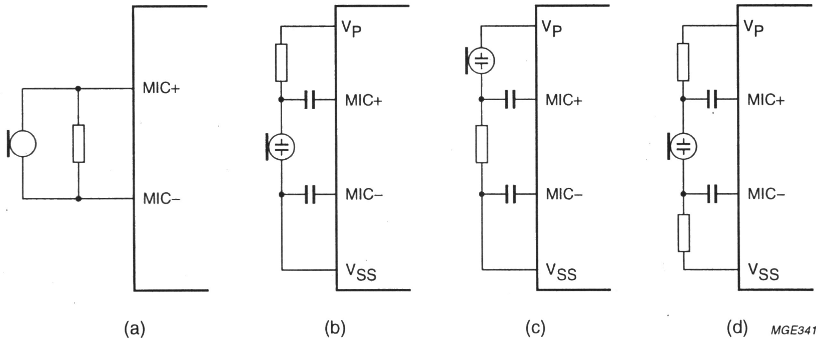
DIAL PULSE INPUT

The DPI bit controls output DOC (open-drain) that drives the gate of an external MOS interrupter transistor. DPI is controlled via the I^2C-bus interface.

If DPI is set to logic 1, pin DOC will be pulled down to switch off the MOSFET to generate a line break. If DPI = 0 pin DOC is HIGH and the interrupter transistor will conduct the line current.

Microphone channel

The PCA1070 has symmetrical microphone inputs and accepts input signals of maximum 70 mV (peak) for THD = 2% ($V_{DD} \geq 2.5$ V). Its input impedance is 100 kΩ and its voltage gain is default 41 dB (typ.). Dynamic, magnetic, piezoelectric and electret (with built-in FET source follower) microphones can be used. Some possible microphone arrangements are shown in Fig.5.



(a) Dynamic or piezo.
(b) Low impedance electret with built-in pre-amplifier.
(c) High impedance electret with built-in pre-amplifier.
(d) Symmetrical connection of electret.

Fig.5 Microphone arrangements.

The gain of the microphone channel can be programmed between 30 dB and 51 dB in 1 dB steps using bit code GMAx (6 bits). The gain of the microphone preamplifier is fixed at 20 dB and GMAx sets the gain of the “send prog-amp” (allowed range G_{ma} = 4 to 25 dB, see Fig.1). The gain of the line interface is 6 dB.

The total gain of the microphone channel (G_M) is as follows:

$G_M = 20 + G_{ma} + 6$ (dB)

Default: $G_M = 20 + 15 + 6 = 41$ (dB)

where G_{ma} = Gain “send prog-amp”

Programming for the gain G_{ma} of the “send prog-amp” is given in Table 14.

Dynamic limiter

To prevent distortion of the transmitted speech signal, the gain of the microphone amplifier is reduced rapidly when signal peaks on the line exceed an internally determined threshold level. The time in which gain reduction is affected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined on the chip (release time). The threshold level of the AC peak-to-peak line voltage on pin LN is default at 3.5 V (p-p). A lower level [2.6 V (p-p)] can be programmed by setting bit code DLT to logic 1.

The internal threshold is lowered automatically if the DC voltage setting of the circuit (V_{SLPE}) is not high enough to reach the programmed level. When the DC current in the transmit output stage is also insufficient to drive the line load, the internal threshold level is lowered automatically.

Dynamic limiting considerably improves sidetone performance in over-drive conditions (less distortion and limited sidetone level).

Program amplifier

A programmable amplifier called “prog-amp” is used both in the sending channel and in the receiving channel. The bit codes GMAx and GRAx are given in Tables 13 and 14 The permitted adjustment range differs for the two amplifiers. This is indicated in the corresponding sections.

DTMF channel

The PCA1070 has an asymmetrical DTMF input. Its input impedance is 200 kΩ//45 pF (typ.) and its voltage gain is default to 21 dB (typ.).

DTMF signals can be sent to the line by setting control bit SM (send mute) to logic 1 (default SM = 0); by setting the receive mute (RM) also to logic 1 (default RM = 0), the dialling tones are also sent to the receive output to generate a confidence tone in the earpiece.

The gain between the DTMF input and the line LN can be programmed between 1 dB and 21 dB in 1 dB steps using bit code GMAx (6 bits). The confidence tone gain (between DTMF input and earpiece outputs QR) can be programmed between −40 dB and −19 dB (symmetrical drive of earpiece) using bit code GRAx (6 bits). GMAx sets the gain of the “send prog-amp” (recommended range in DTMF mode for G_{ma} = −5 to 15 dB; see Fig.1) and GRAx sets the gain of the “rec prog-amp” (allowed range G_{ra} = −25 to 0 dB; see Fig.1).

The total gain of the DTMF channel between the DTMF input and the line LN is as follows:

$G_{DTMF} = G_{ma} + 6$ (dB]

Default $G_{DTMF} = 15 + 6 = 21$ (dB)

The confidence tone gain (DTMF to QR outputs) is:

With symmetrical drive of earpiece $G_{CTs} = G_{ra} - 19$ (dB)

Default $G_{CTs} = -6 - 19 = -25$ (dB)

At low gain settings ($G_{ra} < -10$ dB), the confidence tone gain will be slightly higher than the calculated value. This is caused by a residual signal.

Programming the gain of the “send prog-amp” and the “rec prog-amp” is given in Table 13.

Receive channel

The PCA1070 has an on-chip anti-sidetone circuit. The gain of the receive channel is defined between the line connection LN and the earpiece outputs QR+ and QR−. Its voltage gain is default to −6 dB (typ.) (differential drive). The LN terminal accepts receive signals up to 1 V (RMS) (typ.) for THD = 2%. The outputs may be used to connect dynamic, magnetic or piezoelectric earpieces with single-ended or differential drive. The load select bit RFC is default to logic 1 to guarantee stable operation in the event of a capacitive load (piezoelectric earpiece). With a resistive load (dynamic capsule) RFC should be set to logic 0 via the I^2C-bus interface to obtain optimum performance with respect to distortion and bandwidth. Two levels for hearing protection can be selected via the I^2C-bus interface with control bit HPL.

The earpiece arrangements are illustrated in Fig.6.

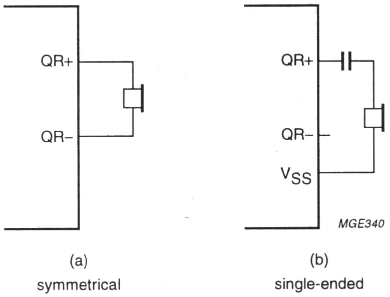


Fig.6 Earpiece arrangements.

The gain of the receive channel can be programmed between −19 dB and +11 dB (symmetrical drive) in 1 dB steps using bit code GRAx (6 bits).

GRAx sets the gain of the "rec prog-amp" (allowed range G_{ra} = −19 dB to +11 dB; default G_{ra} = −6 dB).

The total gain of the receiving channel is as follows:

Symmetrical drive $G_{rs} = G_{ra}$ (dB)

Default $G_{rs} = -6$ (dB)

Asymmetrical or single-ended drive $G_{ra} = G_{ra} - 6$ (dB)

Default $G_{ra} = -6 - 6$ (dB) $= -12$ (dB)

Programming the gain G_{ra} of the "rec prog-amp" is given in Table 13.

Sidetone balance

The PCA1070 has an on-chip anti-sidetone circuit. An internal balance impedance Z_{oss} can be programmed via the I²C-bus interface to match the external line impedance Z_{line} to give optimum sidetone suppression.

$$Z_{oss} = R_{sa} + (R_s//C_s);\ f_{ps} = \frac{1}{(2\pi \times R_s \times C_s)}.$$

Programming for the sidetone balance is given in Tables 15, 16 and 17.

Line current control

The DC line current can be read via the I²C-bus interface. This gives information about the line current and can be used to change several parameters with line current (for example line loss compensation, sidetone balance and DC characteristics).

The bit code LCx as a function of line current is given in Table 18.

I^{2}C-BUS PROGRAMMING

Table 1 Programmable parameters

The following parameters (see Fig.1) can be programmed by means of a bit code via the I^{2}C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
VDCx	V_{ref}	line interface	3	DC voltage SLPE-V_{SS}
ZSAx	Z_{set}	line interface	3	AC set impedance R_a
ZSBx	Z_{set}	line interface	3	AC set impedance R_b
ZSPx	Z_{set}	line interface	4	AC set impedance f_p (pole frequency)
DST	DST	line interface	1	DC Start Time
PDx	PD	power control	2	Power-Down
DPI	DPI	power control	1	Dial Pulse Input
RRG	RRG	power control	1	Reset RinG detector
HPL	maximum receive level	BTL receive output	1	Hearing Protection Level
RFC	load select	BTL receive output	1	Resistive/Capacitive load
ZOSAx	sidetone balance	anti-sidetone	4	Z Optimum Sidetone R_{sa}
ZOSBx	sidetone balance	anti-sidetone	4	Z Optimum Sidetone R_{sb}
ZOSPx	sidetone balance	anti-sidetone	4	Z Optimum Sidetone C_s
RM	receive mute	receive mute	1	Receive Mute
GRAx	gain G_{ra}	receive prog-amp	6	Gain Receive prog-amp
GMAx	gain G_{ma}	send prog-amp	6	Gain send prog-amp
SM	send mute	send mute	1	Send Mute
DLT	threshold	dynamic limiter	1	Dynamic Limiter Threshold

Table 2 Readable parameters

The following parameters (see also Fig.1) can be read as a bit code via the I^{2}C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
PRES	PRES	power control	1	PCA1070 Reset
LCx	line current	gain control	5	Line Current

I^{2}C interface

The I^{2}C-bus interface (see *"The I^{2}C-bus and how to use it"* 12NC: 9398 393 40011) is used to program the transmission parameters and control functions.

Table 3 Device address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	1	0	0	0	1	0	X

All functions can be accessed by writing an 8-bit word to the PCA1070. In order to set up the PCA1070, a control message consisting of the device address, a R/$\overline{W}$ bit, a subaddress byte and one or more data bytes must be written to the PCA1070. If more than one data byte follows the subaddress, these bytes are stored in the successive registers by the automatic increment feature.

Table 4 The control word format for the slave receiver

	DEVICE ADDRESS									SUB ADDRESS									DATA/CONTROL BYTE									
S	0	1	0	0	0	1	0	0(1)	A	I7	I6	I5	I4	I3	I2	I1	I0	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

Note

1. This bit is $R/\overline{W}$.

Table 5 Bit arrangement of each data byte used in the control word: PCA1070 receiver (see note 1)

FUNCTION	SUB ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
DC voltage	H00		VDC2	VDC1	VDC0				DST
Sidetone and set impedance	H01	ZOSB3	ZOSB2	ZOSB1	ZOSB0	ZOSA3	ZOSA2	ZOSA1	ZOSA0
	H02	ZOSP3	ZOSP2	ZOSP1	ZOSP0		ZSA2	ZSA1	ZSA0
	H03		ZSB2	ZSB1	ZSB0	ZSP3	ZSP2	ZSP1	ZSP0
Send channel	H04	DLT		GMA5	GMA4	GMA3	GMA2	GMA1	GMA0
Receive channel	H05	RFC	HPL	GRA5	GRA4	GRA3	GRA2	GRA1	GRA0
Control	H06	PD1	PD0		RRG	RM	SM		DPI

Note

1. The bits that are not indicated must be set to logic 0.

Table 6 The control word format for the slave transmitter

	DEVICE ADDRESS									DATA/STATUS BYTE									
S	0	1	0	0	0	1	0	1(1)	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

Note

1. Change in direction of $R/\overline{W}$ bit.

Table 7 PCA1070 send bits

FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
PCA1070 status	PRES(1)	–	–	LC4(2)	LC3(2)	LC2(2)	LC1(2)	LC0(2)

Notes

1. Indicates if PCA1070 has received internal reset; PRES will be set to logic 1 with internal reset and is set to logic 0 after reading the register via the I^2C-bus.
2. Information about value of line current.

WRITE AND READ TABLES

DC voltages

Table 8 DC voltage at pin SLPE

VDC2	VDC1	VDC0	V_{SLPE}	REMARK
0	0	0	3.1	
0	0	1	3.5	
0	1	0	3.9	
0	1	1	4.3	
1	**0**	**0**	**4.7**	**default**
1	0	1	5.1	
1	1	0	5.5	
1	1	1	5.9	

Set impedance

Programming the impedance in the audio frequency range seen at pin LN: $R_a + (R_b//C)$ where the pole frequency

$$f_p = \left(\frac{1}{(2\pi \times R_b \times C)}\right)$$

Table 9 Programming R_a

ZSA2	ZSA1	ZSA0	R_a (Ω)	REMARK
0	0	0	0	
0	0	1	100	
0	**1**	**0**	**200**	**default**
0	1	1	300	
1	0	0	400	
1	0	1	500	note 1
1	1	X	600	notes 1 and 2

Notes

1. For Z_s combinations where $R_a \geq 500\ \Omega$ it is obligatory that $R_b = 0$. This is to safeguard stable operation of the line interface under all practical conditions.
2. X = don't care.

Table 10 Programming R_b

ZSB2	ZSB1	ZSB0	R_b (Ω)	REMARK
0	0	0	0	note 1
0	0	1	600	
0	1	0	700	
0	**1**	**1**	**800**	**default**
1	X	0	900	note 2
1	X	1	1000	note 2

Notes

1. For Z_s combinations where $R_a \geq 500\ \Omega$ it is obligatory that $R_b = 0$. This is to safeguard stable operation of the line interface under all practical conditions.
2. X = don't care.

Table 11 Programming pole frequency:

ZSP3	ZSP2	ZSP1	ZSP0	f_p (Hz)	C (nF)					REMARK
					$R_b = 600$ (Ω)	$R_b = 700$ (Ω)	$R_b = 800$ (Ω)	$R_b = 900$ (Ω)	$R_b = 1000$ (Ω)	
0	0	0	0	828	320	275	240	214	192	
0	0	0	1	1095	242	207	182	161	145	
0	0	1	0	1448	183	157	137	122	110	
0	**0**	**1**	**1**	**1915**	**139**	**119**	**104**	**92**	**83**	**default**
0	1	0	0	2533	105	90	79	70	63	
0	1	0	1	3350	79	68	59	53	48	
0	1	1	0	4430	60	51	45	40	36	
0	1	1	1	5859	45	39	34	30	27	
1	X	X	X	12000	22	19	17	15	13	note 1

Note

1. X = don't care.

Reset functions

Monitoring of internal reset PCA1070.

Table 12 Status bit PRES

PRES	DESCRIPTION
1	internal reset has occurred; default values in all registers
0	register has been read via the I^2C-bus interface

Programmable amplifier (prog-amp)

A programmable amplifier called "prog-amp" is used both in the sending channel and in the receiving channel. The bit codes GMAx and GRAx are given in Tables 13 and 14. The permitted adjustment range differs for the two amplifiers and is different for the DTMF mode and the speech mode. This is indicated in the corresponding sections.

Table 13 Bit code of rec prog-amp

GAIN (dB)	INPUT CODE				
	MSB				LSB
−25	1	1	1	0	0	1
−24	1	1	1	0	0	0
−23	1	1	0	1	1	1
−22	1	1	0	1	1	0
−21	1	1	0	1	0	1
−20	1	1	0	1	0	0
−19	1	1	0	0	1	1
−18	1	1	0	0	1	0
−17	1	1	0	0	0	1
−16	1	1	0	0	0	0
−15	1	0	1	1	1	1
−14	1	0	1	1	1	0
−13	1	0	1	1	0	1
−12	1	0	1	1	0	0
−11	1	0	1	0	1	1
−10	1	0	1	0	1	0
−9	1	0	1	0	0	1
−8	1	0	1	0	0	0
−7	1	0	0	1	1	1
−6(1)	**1**	**0**	**0**	**1**	**1**	**0**
−5	1	0	0	1	0	1
−4	1	0	0	1	0	0
−3	1	0	0	0	1	1
−2	1	0	0	0	1	0
−1	1	0	0	0	0	1
−0	1	0	0	0	0	0

Notes

1. Default value “rec prog-amp” GRAx.

Table 14 Bit code of send prog-amp

GAIN (dB)	INPUT CODE				
	MSB				LSB
+25	0	1	1	0	0	1
+24	0	1	1	0	0	0
+23	0	1	0	1	1	1
+22	0	1	0	1	1	0
+21	0	1	0	1	0	1
+20	0	1	0	1	0	0
+19	0	1	0	0	1	1
+18	0	1	0	0	1	0
+17	0	1	0	0	0	1
+16	0	1	0	0	0	0
+15(1)	**0**	**0**	**1**	**1**	**1**	**1**
+14	0	0	1	1	1	0
+13	0	0	1	1	0	1
+12	0	0	1	1	0	0
+11	0	0	1	0	1	1
+10	0	0	1	0	1	0
+9	0	0	1	0	0	1
+8	0	0	1	0	0	0
+7	0	0	0	1	1	1
+6	0	0	0	1	1	0
+5	0	0	0	1	0	1
+4	0	0	0	1	0	0
+3	0	0	0	0	1	1
+2	0	0	0	0	1	0
+1	0	0	0	0	0	1
+0	0	0	0	0	0	0

Notes

1. Default value “send prog-amp” GMAx.

Sidetone balance

Internal balance impedance Z_{oss} to match the external line impedance Z_{line} to give optimum sidetone suppression.

$$Z_{oss} = R_{sa} + (R_{sb}//C_s);\ f_{ps} = \frac{1}{(2\pi \times R_{sb} \times C_s)}$$

Table 15 Programming R_{sa}

ZOSA				R_{sa} (Ω)
MSB			**LSB**	
0	0	0	0	134
0	0	0	1	153
0	0	1	0	193
0	0	1	1	221
0	1	0	0	246
0	1	0	1	277
0	1	1	0	295
0	1	1	1	341
1	0	0	0	369
1	0	0	1	443
1	**0**	**1**	**0**	**492**(1)
1	0	1	1	–
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

Note

1. default value.

Table 16 Programming R_{sb}

ZOSB				R_{sb} (Ω)
MSB			**LSB**	
0	0	0	0	465
0	0	0	1	637
0	0	1	0	710
0	0	1	1	803
0	1	0	0	893
0	1	0	1	1003
0	**1**	**1**	**0**	**1259**(1)
0	1	1	1	1410
1	0	0	0	1572
1	0	0	1	1773
1	0	1	0	1978
1	0	1	1	2216
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

Note

1. default value.

Table 17 Programming C_s

ZOSP				C_s (nf)
MSB			LSB	
0	0	0	0	5
0	0	0	1	55
0	0	1	0	58
0	0	1	1	69
0	1	0	0	76
0	1	0	1	85
0	1	1	0	96
0	1	1	1	105
1	0	0	0	121
1	**0**	**0**	**1**	**134**(1)
1	0	1	0	145
1	0	1	1	166
1	1	0	0	186
1	1	0	1	207
1	1	1	0	232
1	1	1	1	259

Note

1. default value.

The optimum setting of R_{sa} depends on the value of the set impedance. To safeguard stable operation of the anti-sidetone circuit under all practical conditions, the following condition must be fulfilled: $R_{sa} \geq 0.5R_a$.

Line current control

Table 18 Bit code LCx and DC line current

BIT CODE LCx					I_{line} (typ.) (mA)
LC4	LC3	LC2	LC1	LC0	
0	0	0	0	0	<12.5
0	0	0	0	1	15.0
0	0	0	1	0	17.5
0	0	0	1	1	20.0
0	0	1	0	0	22.5
0	0	1	0	1	25.0
0	0	1	1	0	27.5
0	0	1	1	1	30.0
0	1	0	0	0	32.5
0	1	0	0	1	35.0
0	1	0	1	0	37.5
0	1	0	1	1	40.0
0	1	1	0	0	42.5
0	1	1	0	1	45.0
0	1	1	1	0	47.5
0	1	1	1	1	50.0
1	0	0	0	0	52.5
1	0	0	0	1	55.0
1	0	0	1	0	58.0
1	0	0	1	1	61.0
1	0	1	0	0	64.0
1	0	1	0	1	66.5
1	0	1	1	0	69.0
1	0	1	1	1	71.5
1	1	0	0	0	74.0
1	1	0	0	1	77.5
1	1	0	1	0	80.0
1	1	0	1	1	82.5
1	1	1	0	0	85.0
1	1	1	0	1	88.0
1	1	1	1	0	91.0
1	1	1	1	1	>94.0

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{LN}	positive line voltage at pin LN	−0.8	12	V
V_i	input voltage on pins SLPE, DOC, REG, TX and LSI	−0.8	12	V
V_{DD}	supply voltage	−0.8	+7.0	V
V_n	voltage on all other pins	−0.8	+7.0	V
I_i	input current	−	±10	mA
P_{tot}	total power dissipation	−	250	mW
T_{stg}	storage temperature	−40	+125	°C
T_{amb}	operating ambient temperature	−10	+60	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		K/W

CHARACTERISTICS

I_{line} = 20 mA; V_{SS} = 0 V; f = 1000 Hz; I_p = 0 mA; I_{VP} = 0 mA; f_{clk} = 3.579545 MHz; T_{amb} = 25 °C; all programmable parameters at default values; control bits set at default: DST = 0; DLT = 0; PDx = 00; RRG = 0; HPL = 0; RM = 0; SM = 0; DPI = 0; control bit not set at default: RFC = 0; AC load impedance at pin LN is Z_{line} = 220 Ω + (820 Ω//115 nF); load impedance at earpiece output R_t = 150 Ω; source impedance at microphone input R_m = 150 Ω; measured in test circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC line interface: LN, TX, SLPE and REG						
I_{line}	line current operating range	normal operation	17	–	140	mA
		reduced sending level	12	–	17	mA
V_{SLPE}	reference DC voltage at SLPE, DST = 0 with or without clock	VDCx = 100 default	4.3	4.7	5.1	V
$V_{SLPE(min)}$	minimum selectable value	VDCx = 000; note 1	2.8	3.1	3.4	V
$V_{SLPE(max)}$	maximum selectable value	VDCx = 111; note 1	5.4	5.9	6.4	V
$V_{SLPE(step)}$	step resolution		–	0.4	–	V
V_{SLPE}	reference DC voltage at SLPE, DST = 1 with or without clock	VDCx = 100 default	–	4.7	–	V
$V_{SLPE(min)}$	minimum selectable value	VDCx = 000; note 1	–	3.1	–	V
$V_{SLPE(max)}$	maximum selectable value	VDCx = 111; note 1	–	5.9	–	V
$V_{SLPE(step)}$	step resolution		–	0.4	–	V
ΔV_{SLPE}	reference DC voltage at SLPE variation with temperature	at –10°C and +60 °C with respect to T_{amb} = 25 °C; DST = 0	–	±20	–	mV
V_{LN}	DC line voltage at LN (slope = 20 Ω); with or without clock at default	VDCx = 100; DST = 0; I_{line} = 12 mA	–	4.83	–	V
		VDCx = 100; DST = 0; I_{line} = 20 mA	4.6	5.0	5.4	V
		VDCx = 100; DST = 0; I_{line} = 120 mA	6.5	7.0	7.5	V
V_{LN}	DC line voltage at LN at low line current with or without clock	DST = 0; I_{line} = 0.25 mA	–	1	–	V
		DST = 0; I_{line} = 2 mA	–	1.9	–	V
		DST = 0; I_{line} = 4 mA	–	3.4	–	V
		DST = 0; I_{line} = 7 mA	–	4.73	5.2	V
t_{DC}	DC start-up time	C_{VDD} = 470 μF; I_{line} = 20 mA; (no clock; V_{clk} = 0); note 2	–	145	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TX: DRIVE OUTPUT (EXTERNAL pnp)						
V_{TX}	output drive voltage with TX disconnected from external pnp	V_{SLPE} = 2 V; V_{REG} = 1.5 V; V_{DD} = VMC = 2.5 V; I_{TX} = 0 mA	–	1.45	–	V
		V_{SLPE} = 3 V; V_{REG} = 2.5 V; V_{DD} = VMC = 2.5 V; I_{TX} = 1.6 mA	–	2.2	–	V
t_{SW}	switching time DC voltage at SLPE	V_{SLPE} = 5.9 V to 3.1 V; DST = 0; note 3	–	65	–	ms
		V_{SLPE} = 3.1 V to 5.9 V; DST = 0; note 3	–	65	–	ms
		V_{SLPE} = 5.9 V to 3.1 V; DST = 1; note 3	–	1	–	ms
		V_{SLPE} = 3.1 V to 5.9 V; DST = 1; note 3	–	0.5	–	ms
Supplies: V_{DD}, VMC, V_P and SLPE						
V_{DD}	operating supply voltage	normal operation; note 4	2.5	–	6	V
		relaxed performance; note 5	1.8	–	2.5	V
V_{DD}; SUPPLY PIN						
I_{DD}	current consumption	PDx = 00 default; V_{DD} = 2.5 V; normal operation	–	2.3	–	mA
$I_{DD(int)}$	internal current in power-down or standby mode; I^{2}C-bus in idle mode	power-down; PDx = 01; SCL = 1; SDA = 1	–	30	100	μA
		standby; PDx = 11; SCL = 1; SDA = 1	–	2	5	μA
V_{DD}: PERIPHERAL SUPPLY						
I_p	current available for peripheral circuitry	V_{DD} = 2.9 V; SM = 1; RM = 1; V_{SLPE} = 4.7 V (default); $R_{SLPE\text{-}VDD}$ = 250 Ω external	–	4.9	–	mA
		V_{DD} = 2.5 V; SM = 1; RM = 1; V_{SLPE} = 4.7 V (default); $R_{SLPE\text{-}VDD}$ = 250 Ω external	–	6.5	–	mA
VMC; SENSE INPUT MICROCONTROLLER SUPPLY VOLTAGE						
I_{VMC}	input current	VMC = 2.5 V in normal operation; PDx = 00 default	–	4	10	μA
I_{VMC}	input current in power-down or standby mode; I^{2}C-bus in idle mode	VMC = 2.5 V in power-down; PDx = 01; SCL = 1; SDA = 1	–	4	10	μA
		VMC = 2.5 V in standby; PDx = 11; SCL = 1; SDA = 1	–	2	5	μA
V_P; SUPPLY OUTPUT FOR ELECTRET MICROPHONE						
V_P	voltage available	I_{VP} = 500 μA	1.6	1.9	–	V
Z_o	output impedance	f = 300 Hz	–	40	–	Ω
PSR	power supply rejection	f = 300 Hz; note 6	–	65	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset functions: V_{DD}, VMC and RMC						
INTERNAL RESET PCA1070: note 7						
$V_{DD(SW)}$	switching level of V_{DD} below which internal reset is active	T_{amb} = −10 to +60 °C	1.0	1.2	1.4	V
RMC: RESET OUTPUT FOR MICROCONTROLLER						
$V_{VMC(SW)}$	voltage switching level at pin VMC where RMC changes state	normal operation; PDx = 00; T_{amb} = 25 °C; note 8	1.8	2.0	2.2	V
		power-down; PDx = 01; T_{amb} = 25 °C; note 8	1.8	2.0	2.2	V
		standby; PDx = 11; T_{amb} = 25 °C; note 8	1.8	2.1	2.4	V
$\Delta V_{VMC}/T$	sense voltage variation with temperature	normal operation; PDx = 00; T_{amb} = −10 to +60 °C	–	0	–	mV/°C
		power-down; PDx = 01; T_{amb} = −10 to +60 °C	–	0	–	mV/°C
		standby; PDx = 11; T_{amb} = −10 to +60 °C	–	3	–	mV/°C
Sending channel: MIC+, MIC–, DTMF, OMIC, LN, SCR, REG and LSI						
MIC+, MIC–: MICROPHONE INPUTS						
Z_i	input impedance	differential	60	100	–	kΩ
		single-ended	30	50	–	kΩ
CMRR	common mode rejection ratio	f = 1000 Hz; note 9	–	72	–	dB
$V_{i(peak)}$	allowed input signal voltage level (peak value)		–	–	70	mV
$G_{v(MIC)}$	voltage gain MIC+/MIC– to LN	GMAx = 001111 default	39.5	41	42.5	dB
$G_{v(min)}$	minimum selectable voltage gain	GMAx = 000100; note 1	28.5	30	31.5	dB
$G_{v(max)}$	maximum selectable voltage gain	GMAx = 011001; note 1	49.5	51	52.5	dB
G_{step}	step resolution		–	1	–	dB
ΔG_v	frequency response	gain variation at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 10	–	–	+0.3/−0.7	dB
ΔG_v	voltage gain variation with temperature	at −10 to +60 °C with respect to T_{amb} = 25 °C	–	±0.2	–	dB
ΔG_v	voltage gain variation with line current	at 100 mA with respect to 20 mA; note 10	–	0	±0.5	dB
t_{AC}	AC start-up time (with clock V_{clk})	C_{VDD} = 470 μF; I_{line} = 20 mA; note 11	–	150	–	ms
Send mute/privacy switch						
ΔG_v	voltage gain reduction from MIC+/MIC– to LN	SM = 1; note 1	–	100	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF: dual tone multi-frequency input						
Z_{IRp}	input impedance $R_p//C_p$	single-ended	100	200	–	kΩ
Z_{ICp}	input impedance $R_p//C_p$	single-ended	–	45	–	pF
$G_{v(LN)}$	voltage gain from DTMF to LN	SM = 1 default; GMAx = 001111	20	21	22	dB
$G_{v(min)}$	minimum selectable voltage gain	SM = 1 default; GMAx = 100101; note 1	0	1	2	dB
$G_{v(max)}$	maximum selectable voltage gain	SM = 1 default; GMAx = 001111; note 1	20	21	22	dB
G_{step}	step resolution		–	1	–	dB
ΔG_v	frequency response	SM = 1; gain variation at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 10	–	–	+0.3/–0.7	dB
ΔG_v	voltage gain variation with temperature	SM = 1; at –10 to +60 °C with respect to T_{amb} = 25 °C	–	±0.2	–	dB
ΔG_v	voltage gain variation with line current	SM = 1; at 100 mA with respect to 20 mA; note 10	–	0	±0.5	dB
Confidence tone; note 12						
$G_{v(QR)}$	voltage gain from DTMF to QR+ or QR–	GRAx = 100110 default; SM = 1; RM = 1; differential load RT = 150 Ω	–	–25	–	dB
$G_{v(min)}$	minimum selectable voltage gain	GRAx = 111001; SM = 1; RM = 1; differential load RT = 150 Ω; note 1	–	–40	–	dB
$G_{v(max)}$	maximum selectable voltage gain	GRAx = 100000; SM = 1; RM = 1; differential load RT = 150 Ω; note 1	–	–19	–	dB
G_{step}	step resolution		–	0.5 to 1	–	dB
LN: sending channel output						
Z_{LN}	impedance between LN and V_{SS}; $f_p = 1/(2\pi \times R_b \times C)$ $Z_{LN} \approx Z_s = R_a + (R_b//C)$;	ZSAx = 010 default; no Z_{line}; notes 13 and 14	–	200	–	Ω
		ZSBx = 011 default; no Z_{line}; notes 13 and 14	–	800	–	Ω
		ZSPx = 0011 default; no Z_{line}; notes 13 and 14	–	1915	–	Hz
BRL	balance return loss Z_{LN} with respect to Z_{ref}; Z_{ref} = 220 Ω + (820 Ω//115 nF)	Z_s = default; f = 300 Hz; note 15	20	37	–	dB
		Z_s = default; f = 1 kHz; note 15	20	35	–	dB
		Z_s = default; f = 3.4 kHz; note 15	20	27	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SELECTABLE VALUES FOR Z_S; note 1						
$R_{a(min)}$	minimum selectable value for R_a	$R_b = 0$; $f_p = 12$ kHz; ZSAx = (001); note 16	–	100	–	Ω
$R_{a(max)}$	maximum selectable value for R_a	$R_b = 0$; $f_p = 12$ kHz; ZSAx = (11x); note 16	–	600	–	Ω
$R_{a(step)}$	step resolution for R_a		–	100	–	Ω
$R_{b(min)}$	minimum selectable value for R_b	$R_a = 0$; $f_p = 12$ kHz; ZSBx = (001); note 16	–	600	–	Ω
$R_{b(max)}$	maximum selectable value for R_b	$R_a = 0$; $f_p = 12$ kHz; ZSBx = (1x1); note 16	–	1000	–	Ω
$R_{b(step)}$	step resolution for R_b		–	100	–	Ω
$f_{p(min)}$	minimum selectable pole frequency	$R_a = 0$; $R_b = 1$ kΩ; ZSPx = (0000); note 17	–	828	–	Hz
$f_{p(max)}$	maximum selectable pole frequency	$R_a = 0$; $R_b = 1$ kΩ; ZSPx = (0111); note 17	–	5859	–	Hz
n	multiplication factor for pole frequency	$f_p(x + 1) = n \times [f_p(x)]$	–	1.322	–	
$V_{no(rms)}$	noise output voltage (RMS value)	150 Ω between MIC+ and MIC-; psophometrically weighted (O41 curve)	–	–76	–	dBmp
Dynamic limiter; note 1						
$V_{LN(p-p)}$	voltage threshold level at which dynamic limiter reduces send gain (peak-to-peak value)	V_{SLPE} = default (4.7 V ±0.4 V); DLT = 0 default	3.1	3.5	3.9	V
		V_{SLPE} = default (4.7 V ±0.4 V); DLT = 1 default	2.2	2.6	3.0	V
THD	total harmonic distortion	$V_i = 12$ mV (RMS) + 10 dB	–	2.5	5.0	%
Dynamic behaviour of limiter; note 18						
t_{att}	attack time	V_i jumps from 12 to 38 mV (RMS)	–	1.5	–	ms
t_{rel}	release time	V_i jumps from 38 to 12 mV (RMS)	–	90	–	ms
$V_{LN(p-p)}$	voltage threshold level at which dynamic limiter reduces send gain	low voltage conditions; DLT = 0; $V_{SLPE} = 3.1$ V; $I_{line} = 20$ mA	–	2.4	–	V
		low current conditions; DLT = 0; $V_{SLPE} = 4.7$ V; $I_{line} = 9$ mA	–	2.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCR: pin for sending current resistor						
V_{SCR}	voltage at pin SCR	I_{line} = 20 mA; GMAx = 001111; G_M = 41 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.28	–	V
		I_{line} = 20 mA; GMAx = 000100; G_M = 30 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.26	–	V
		I_{line} = 12 mA; GMAx = 001111; G_M = 41 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.22	–	V
		I_{line} = 7 mA; GMAx = 001111; G_M = 41 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.13	–	V
Receive channel: LN, LSI, OREC, QR+ and QR–						
QR+, QR–: RECEIVING AMPLIFIER OUTPUTS						
Z_o	output impedance	single-ended	–	4	–	Ω
$G_{v(rec)}$	voltage gain from LN to QR	RFC = 0 default; R_t = 150 Ω; GRAx = 100110; single-ended	–13.5	–12	–10.5	dB
		RFC = 0 default; R_t = 150 Ω; GRAx = 100110; differential	–7.5	–6	–4.5	dB
$G_{v(min)}$	minimum selectable voltage gain	GRAx = 110011; R_t = 150 Ω; single-ended	–26.5	–25	–23.5	dB
		GRAx = 110011; R_t = 150 Ω; differential	–20.5	–19	–17.5	dB
$G_{v(max)}$	maximum selectable voltage gain	GRAx = 001011; R_t = 150 Ω; single-ended	3.5	5.0	6.5	dB
		GRAx = 001011; R_t = 150 Ω; differential	9.5	11.0	12.5	dB
$G_{v(step)}$	voltage gain step resolution		–	1	–	dB
ΔG_v	frequency response	R_t = 150 W; RFC = 0; gain variation at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 10	–	–	±0.5	dB
ΔG_v	voltage gain variation with temperature	R_t = 150 Ω; RFC = 0 at –10 to +60 °C with respect to T_{amb} = 25 °C	–	±0.2	–	dB
ΔG_v	voltage gain variation with line current	R_t = 150 Ω; RFC = 0; 100 mA with respect to 20 mA; note 10	–	0	±0.5	dB
t_{ACsu}	AC start-up time (with clock V_{clk})	C_{VDD} = 470 μF; I_{line} = 20 mA; note 11	–	140	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(p-p)}$	hearing protection output voltage swing (peak-to-peak value)	V_{DD} = 5 V; receive gain set to +11 dB differential; $R_t = \infty\ \Omega$; RFC = 1; V_{LN} = 2 V (RMS); HPL = 0 default	–	2.3	–	V
		V_{DD} = 5 V; receive gain set to +11 dB differential; $R_t = \infty\ \Omega$; RFC = 1; V_{LN} = 2 V (RMS); switchable HPL = 1; note 1	–	5.9	–	V
$V_{o(rms)}$	output voltage (RMS value); THD = 2%	single-ended; RFC = 0; HPL = 1; Z_t = 150 Ω + 100 μF at QR; (+3 dB receiver gain); GRAx = 001001; note 19	0.45	–	–	V
		differential; RFC = 0; HPL = 1; R_t = 150 Ω; (+3 dB receiver gain); GRAx = 000011; note 19	0.45	–	–	V
		differential; RFC = 0; HPL = 1; R_t = 450 Ω; (+3 dB receiver gain); GRAx = 000011; note 19	0.84	–	–	V
		differential; RFC = 1; C_t = 80 nF; f = 3.4 kHz; (+3 dB receiver gain); GRAx = 000011; note 19	0.9	–	–	V
$V_{no(rms)}$	noise output voltage (RMS value); Z_{line} = 220 Ω + (820 Ω//115 nF)	differential; 150 Ω between MIC+ and MIC–; R_t = 150 Ω; psophometrically weighted (O41 curve); (–6 dB receiver gain); GRAx = 100110	–	–82	–	dBmp
V_{DCos}	DC offset voltage between QR+/QR–	(–6 dB receiver gain); GRAx = 100110	–	–	±100	mV
Sidetone balance adjustment						
Z_{oss}	internal balance impedance Z_{oss} to match the external load impedance at pin LN ($Z_{line} = Z_{oss}$) for optimum sidetone suppression; $Z_{oss} = R_{sa} + (R_{sb}//C_s)$; [$f_{ps} = 1/(2\pi \times R_{sb} \times C_s)$]	ZOSAx = 1010 default; note 20	–	492	–	Ω
		ZOSBx = 0110 default; note 20	–	1259	–	Ω
		ZOSPx = 1001 default; note 20	–	134	–	nF
$R_{sa(min)}$	minimum selectable value Z_{oss} for range R_{sa}	ZOSAx = 0000; notes 1 and 21	–	134	–	Ω
$R_{sa(max)}$	maximum selectable value Z_{oss} for range R_{sa}	ZOSAx = 1010; notes 1 and 21	–	492	–	Ω
$R_{sb(min)}$	minimum selectable value Z_{oss} for range R_{sb}	ZOSBx = 0000; notes 1 and 21	–	465	–	Ω
$R_{sb(max)}$	maximum selectable value Z_{oss} for range R_{sb}	ZOSBx = 1011; notes 1 and 21	–	2216	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{s(min)}$	minimum selectable value Z_{oss} for range C_s	ZOSPx = 0000; note 22	–	55	–	nF
$C_{s(max)}$	maximum selectable value Z_{oss} for range C_s	ZOSPx = 1111; note 22	–	259	–	nF
Sidetone suppression						
$G_{v(st)}$	voltage gain from MIC+/MIC– to QR outputs; Z_{line} = 492 Ω + (1259 Ω//134 nF)	differential output; R_t = 150 Ω; f = 300 Hz; Z_{oss} = default; note 23	–	11	15	dB
		differential output; R_t = 150 Ω; f = 1 kHz; Z_{oss} = default; note 23	–	5	10	dB
		differential output; R_t = 150 Ω; f = 3.4 kHz; Z_{oss} = default; note 23	–	9	15	dB
Dial output connection: DOC (open-drain output)						
$I_{DOCsink}$	output sink current	V_{DOC} = 12 V; DPI = 0	–	0	100	nA
		V_{DOC} = 0.4 V; V_{DD} = 2.5 V; DPI = 1	200	400	–	μA
Line current control: LN and SLPE						
$I_{line(min)}$	typical minimum value of DC line current that can be read as a bit code via the I²C-bus	LCx = 00001; note 1	–	15	–	mA
$I_{line(max)}$	typical maximum value of DC line current that can be read as a bit code via the I²C-bus	LCx = 11110; note 1	–	91	–	mA
$I_{line(step)}$	DC line current step resolution	note 24	–	≈2.5	–	mA
I²C-bus inputs/outputs: SDA and SCL						
	in accordance with standard	note 25				
Clock input: CLK						
$V_{clk(p-p)}$	input signal voltage level (peak-to-peak value)	f_i = 3.579545 MHz	200	–	VMC–V_{SS}	mV
Δf/f	input frequency tolerance with respect to f_i = 3.579545 MHz	note 26	–	–	±0.5	%
R_i	input resistance		–	800	–	Ω
C_i	input capacitance		–	4	–	pF

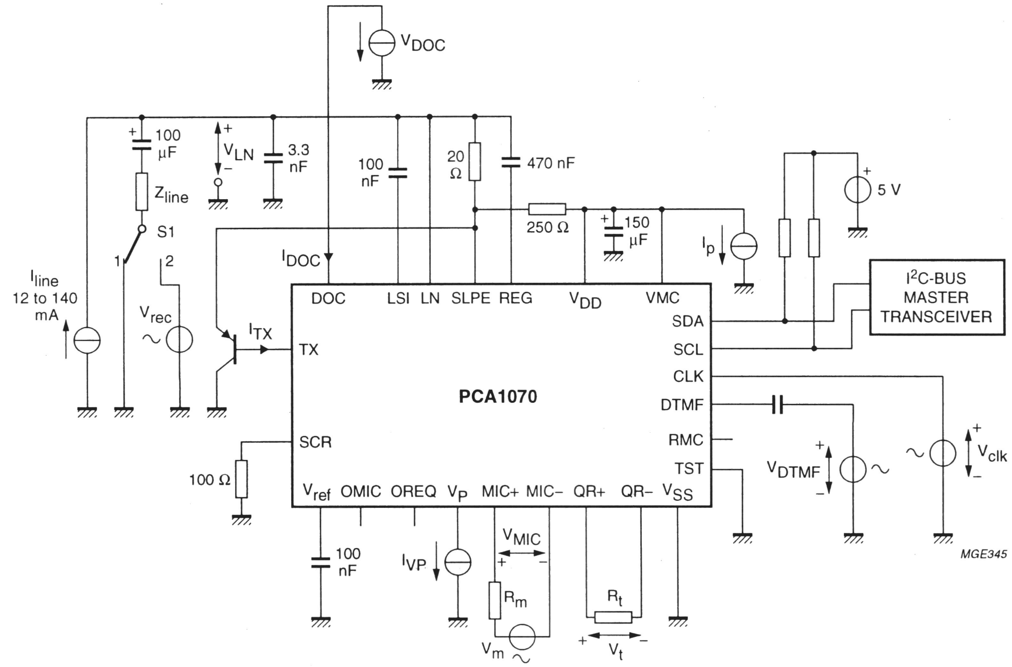
Notes to the characteristics

1. Programmable via the I^2C-bus; bit codes are given in Chapter "I^2C-BUS PROGRAMMING".
2. Time needed to reach default DC reference voltage V_{SLPE} (±10% from final value);
   a) Time depends strongly on the value of the capacitor(s) at V_{DD} and VMC; with a lower value of C_{VDD} the DC start-up time decreases.
   b) The start-up time can be reduced considerably by programming the bit code DST = 1 during the start-up procedure. In practice this is possible as soon as the microcontroller has become operational.
3. Time needed to reach DC reference voltage V_{SLPE} (±10% from final value).
4. The supply voltage V_{DD} is determined by the regulated DC voltage at pin SLPE and by the voltage drop between pin SLPE and V_{DD}; see Chapter "Functional description".
5. Relaxed performance means: parameters can deviate from their specified values.
6. Rejection between supply pin V_{DD} and V_P. Rejection between pin LN and V_P can be calculated by adding the attenuation of the first-order low-pass filter ($R = 250\ \Omega$, $C = 150\ \mu F$) between SLPE and V_{DD}.
7. Switching level of V_{DD} below which the internal reset is active. If V_{DD} is above this level, the default values have been loaded into the internal registers.
8. RMC changes from logic 1 to logic 0 when voltage on pin VMC is increasing; RMC changes from logic 0 to logic 1 when voltage on pin VMC is decreasing; see Fig.4.
9. Common mode signal is applied via $2 \times 470\ \Omega$ external resistors connected to pins MIC+ and MIC–.
10. Not tested, guaranteed by design.
11. Time needed to reach default gain settings (± 3 dB value).
12. At low gain settings the confidence tone gain will be slightly higher than the calculated value.
13. The set impedance between pin LN and V_{SS} consists of $R_a + (R_b//C)$ in parallel with an artificial inductor L_{eq} and internal resistors R_p and R_{LSI} and internal capacitor C_p. See Chapter "Functional description".
14. Without clock the set impedance is automatically set to $Z_s = 600\ \Omega$ (typ.).
15. Balance Return Loss indicates the deviation of an impedance with respect to a reference impedance.
    $BRL = 20 \log|(Z_{LN} + Z_{ref})/(Z_{LN} - Z_{ref})|$ where $Z_{LN} \approx R_a + (R_b//C)$ is the impedance seen into pin LN
    $Z_{ref} = R_{a(ref)} + (R_{b(ref)}//C_{ref})$ is the reference impedance.
16. Value '0' can also be programmed.
17. Value $f_p = 12$ kHz can also be programmed.
18. Attack and release times are also valid under low current and low voltage conditions.
19. The maximum possible output swing depends on the DC conditions (the programmed voltage V_{SLPE} and the load on the supply pin V_{DD}) and on the gain setting of the receive channel.
20. Without clock the sidetone balance impedance is automatically set to $Z_{oss} = 600\ \Omega$ (typ.).
21. Exact values can be found in Tables 15, 16 and 17.
22. value $C_s = 5$ nF can also be programmed.
23. Gain microphone channel G_M = default (typ. 41 dB); gain receive channel G_{rec} = default (typ. –6 dB); sidetone gain G_{st} minimum sidetone suppression at f = 300 Hz and 3400 Hz is: $G_M + G_R - G_{st(max)} = 41 - 6 - 15 = 20$ dB.
24. Indication only; exact values can be found in Table 17.
25. Standard I^2C specifications are valid for $V_{DD} \geq 2.5$ V. Relaxed specifications for $V_{DD} = 1.8$ to 2.5 V.
26. Recommended accuracy of input frequency; a higher tolerance will cause parameters to deviate from their specified values; note that all parameters are specified with the reference input clock frequency $f_{clk} = 3.579545$ MHz.

TEST AND APPLICATION INFORMATION

The test circuit is illustrated in Fig.7. The basic application circuit is illustrated in Fig.8. An interrupter with an N-channel depletion MOS transistor (e.g. BSD254A or BSP124) is shown. It is intended for applications where a low DC line voltage is required. An interrupter with an N-channel enhancement MOS transistor (e.g. BSN304A or BSP130) can be used for applications where a relatively high DC line voltage is allowed.

An application circuit for applications where a low DC line voltage and long line interrupts are required, is illustrated in Fig.9 (interrupter with an N-channel depletion MOS transistor).


V_{DOC}
100 µF
V_{LN}
3.3 nF
100 nF
20 Ω
470 nF
Z_{line}
S1
1
2
250 Ω
150 µF
I_p
5 V
I_{DOC}
I_{line} 12 to 140 mA
V_{rec}
I_{TX}
DOC
LSI
LN
SLPE
REG
V_{DD}
VMC
SDA
SCL
CLK
DTMF
RMC
TST
TX
SCR
PCA1070
I²C-BUS MASTER TRANSCEIVER
100 Ω
V_{ref}
OMIC
OREQ
V_P
MIC+
MIC−
QR+
QR−
V_{SS}
V_{DTMF}
V_{clk}
100 nF
I_{VP}
V_{MIC}
R_m
V_m
R_t
V_t
MGE345

Definitions:

Gain microphone channel $G_M = 20\log(V_{LN}/V_M)$ with S1 in position 1; $V_{DTMF} = 0$.

Gain DTMF amplifier $G_{DTMF} = 20\log(V_{LN}/V_{DTMF})$ with S1 in position 1; $V_m = 0$.

Gain receive channel $G_{rec} = 20\log(V_T/V_{LN})$ with S1 in position 2; $V_m = 0$.

Sidetone gain $G_{st} = 20\log(V_T/V_M)$ with S1 in position 1; $V_{DTMF} = 0$.

Fig.7 Test circuit of the PCA1070.

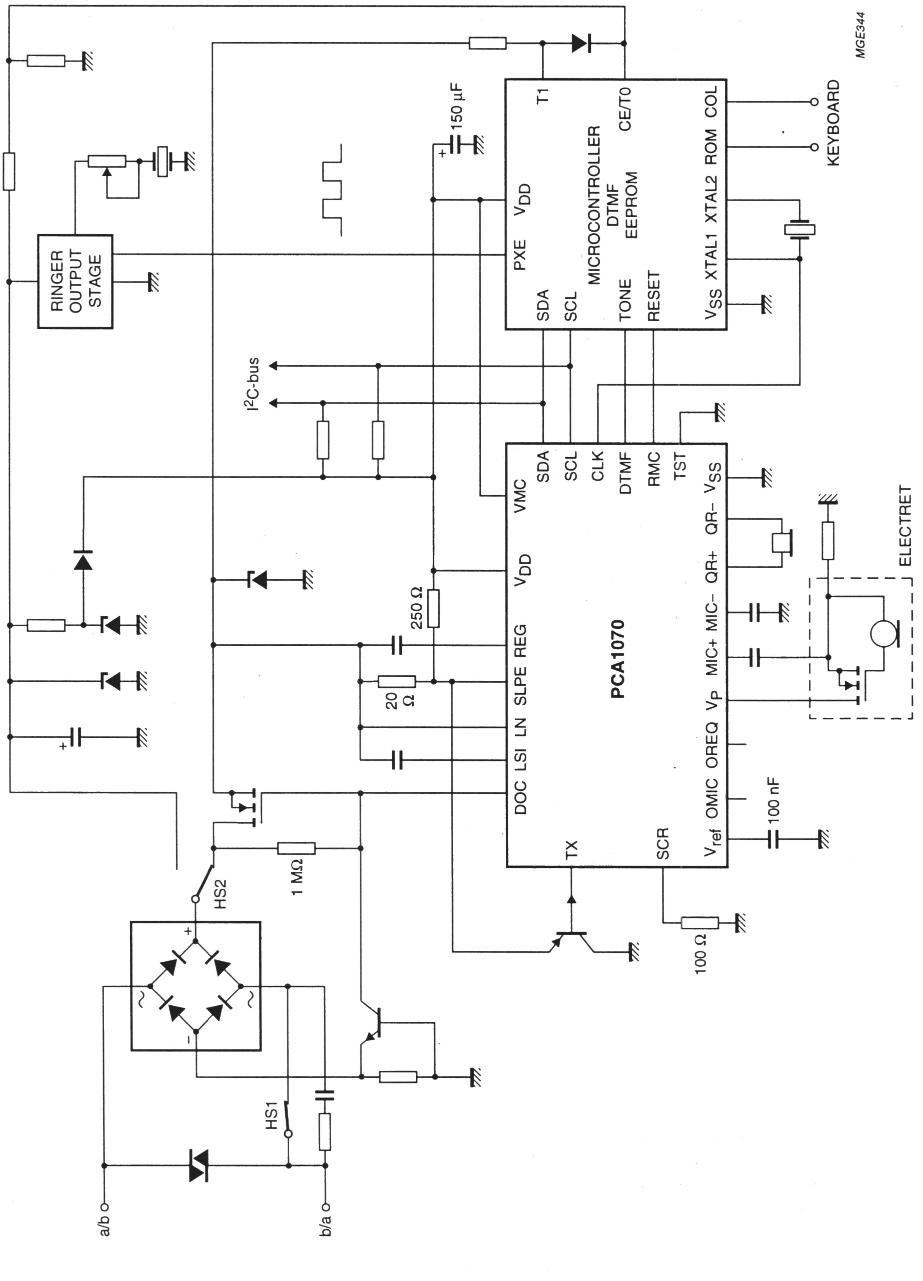

MGE344
T1
CE/T0
MICROCONTROLLER
DTMF
EEPROM
150 μF
KEYBOARD
COL
ROM
XTAL2
XTAL1
V_{DD}
PXE
SDA
SCL
TONE
RESET
V_{SS}
RINGER OUTPUT STAGE
I^2C-bus
VMC
SDA
SCL
CLK
DTMF
RMC
TST
V_{SS}
QR−
QR+
MIC−
MIC+
V_P
OREQ
OMIC
V_{ref}
V_{DD}
REG
SLPE
LN
LSI
DOC
PCA1070
250 Ω
20 Ω
ELECTRET
100 nF
TX
SCR
100 Ω
1 MΩ
HS2
HS1
a/b
b/a

Fig.8 Basic application diagram.

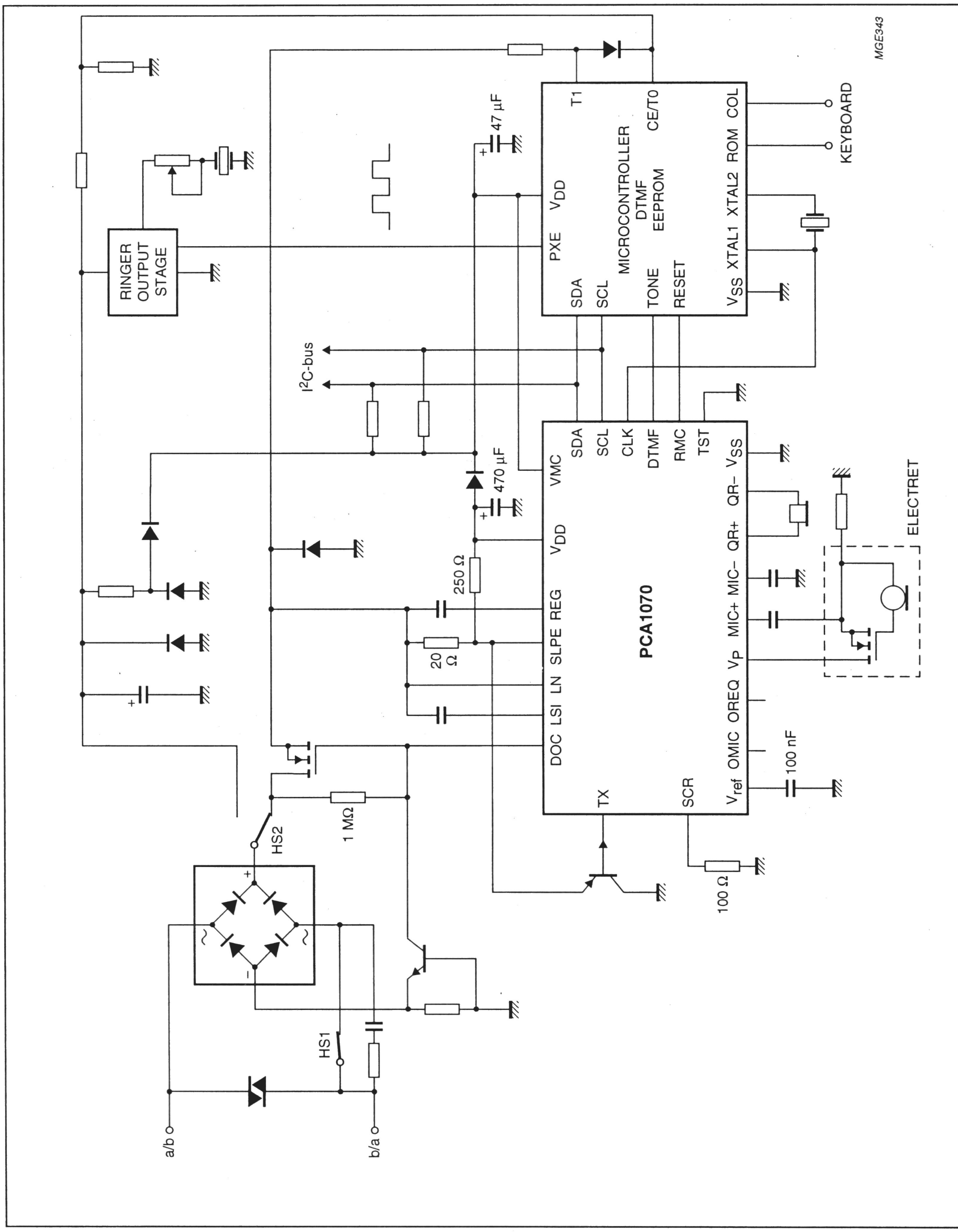

MGE343
T1
CE/T0
MICROCONTROLLER
DTMF
EEPROM
PXE
V_{DD}
SDA
SCL
TONE
RESET
V_{SS}
XTAL1
XTAL2
ROM
COL
KEYBOARD
47 μF
RINGER OUTPUT STAGE
I^2C-bus
470 μF
250 Ω
20 Ω
PCA1070
VMC
SDA
SCL
CLK
DTMF
RMC
TST
V_{SS}
QR−
QR+
MIC−
MIC+
V_P
OREQ
OMIC
V_{ref}
V_{DD}
REG
SLPE
LN
LSI
DOC
TX
SCR
ELECTRET
100 nF
100 Ω
1 MΩ
HS2
HS1
a/b
b/a
+
−
~

Fig.9 Application diagram.

128 × 8-bit EEPROM with I^{2}C-bus interface PCA8581; PCA8581C

FEATURES

- Operating supply voltage:
  - 4.5 to 5.5 V (PCA8581)
  - 2.5 to 6.0 V (PCA8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current; maximum 10 μA
- 8-byte page write mode
- Serial input/output bus (I^{2}C-bus)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for minimum 10000 write cycles per byte
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582
- Operating temperature: –25 to +85 °C.

GENERAL DESCRIPTION

The PCA8581 and PCA8581C are low power CMOS EEPROMs with standard and wide operating voltages:

4.5 to 5.5 V (PCA8581)
2.5 to 6.0 V (PCA8581C).

In the following text, the generic term ‘PCA8581’ is used to refer to both types in all packages except when otherwise specified.

The PCA8581 is organized as 128 words of 8-bytes.

Addresses and data are transferred serially via a two-line bidirectional bus (I^{2}C-bus). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to 8 bytes can be written in one operation, reducing the total write time per byte. Three address pins, A0, A1 and A2 are used to define the hardware address, allowing the use of up to 8 devices connected to the bus without additional hardware.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	PCA8581		4.5	5.5	V
	PCA8581C		2.5	6.0	V
I_{DD}	supply current (standby)	f_{SCL} = 0 Hz	–	10	μA
T_{amb}	operating ambient temperature		–25	+85	°C
T_{stg}	storage temperature	without EEPROM retention	–65	+150	°C
		with EEPROM retention	–65	+85	°C

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA8581P	8	DIP	plastic	SOT97-1
PCA8581CP	8	DIP	plastic	SOT97-1
PCA8581T	8	SO8	plastic	SOT96-1
PCA8581CT	8	SO8	plastic	SOT96-1

BLOCK DIAGRAM

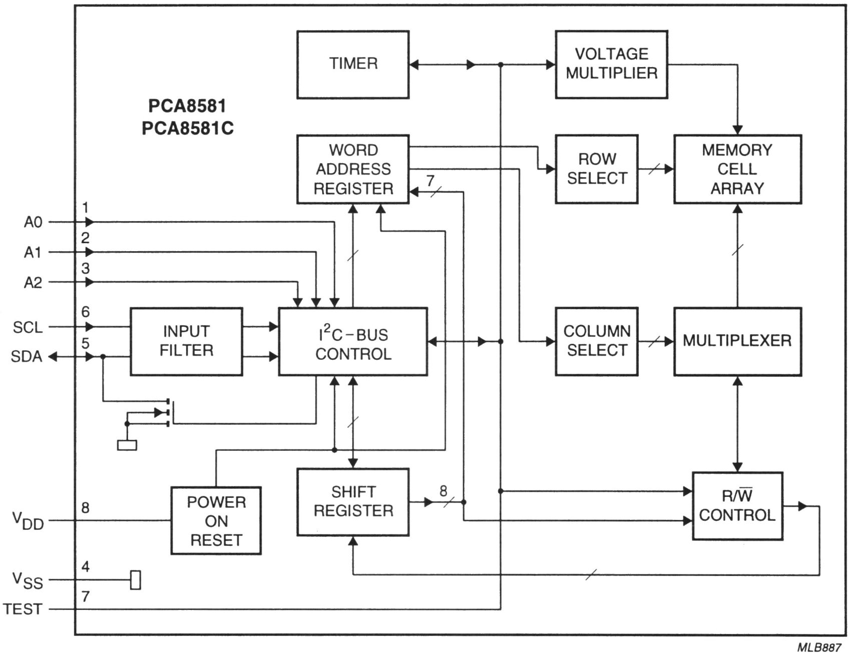

TIMER
VOLTAGE MULTIPLIER
PCA8581
PCA8581C
WORD ADDRESS REGISTER
ROW SELECT
MEMORY CELL ARRAY
7
A0
A1
A2
1
2
3
SCL
SDA
6
5
INPUT FILTER
I²C-BUS CONTROL
COLUMN SELECT
MULTIPLEXER
VDD
8
POWER ON RESET
SHIFT REGISTER
8
R/W̄ CONTROL
VSS
4
TEST
7
MLB887

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	hardware address input 0
A1	2	hardware address input 1
A2	3	hardware address input 2
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
TEST	7	test output can be connected to V_{SS}, V_{DD} or left open-circuit
V_{DD}	8	supply

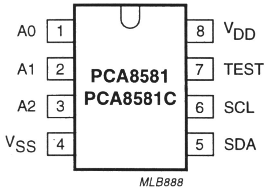

A0
1
A1
2
A2
3
VSS
4
PCA8581
PCA8581C
8
VDD
7
TEST
6
SCL
5
SDA
MLB888

Fig.2 Pin configuration.

Pulse and DTMF dialler with redial

PCD3310 family

FEATURES

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed-mode dialling: start with $\overline{\text{PD}}$ and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys: program, flash, redial and $\overline{\text{PD}}$ to DTMF (mixed dialling)
- DTMF timing:
  - manual dialling
  - minimum duration for bursts and pauses redialling
  - calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (*CEPT CS 203* compatible)
- On-chip oscillator uses low-cost 3.58 MHz (TV colour burst) crystal or piezo resonator
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output.

GENERAL DESCRIPTION

The PCD3310 family are single-chip silicon gate CMOS integrated circuits with on-chip oscillators suitable for use with 3.58 MHz crystals. They are dual-standard dialling ($\overline{\text{PD}}$) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either the DP or DTMF mode.

Numbers up to 23 digits can be retained in RAM for redial and notepad facilities.

In the DTMF mode bursts and pauses are timed to a minimum. In manual dialling the maximum depends on the key depression time. For data communication mixed mode dialling is also possible.

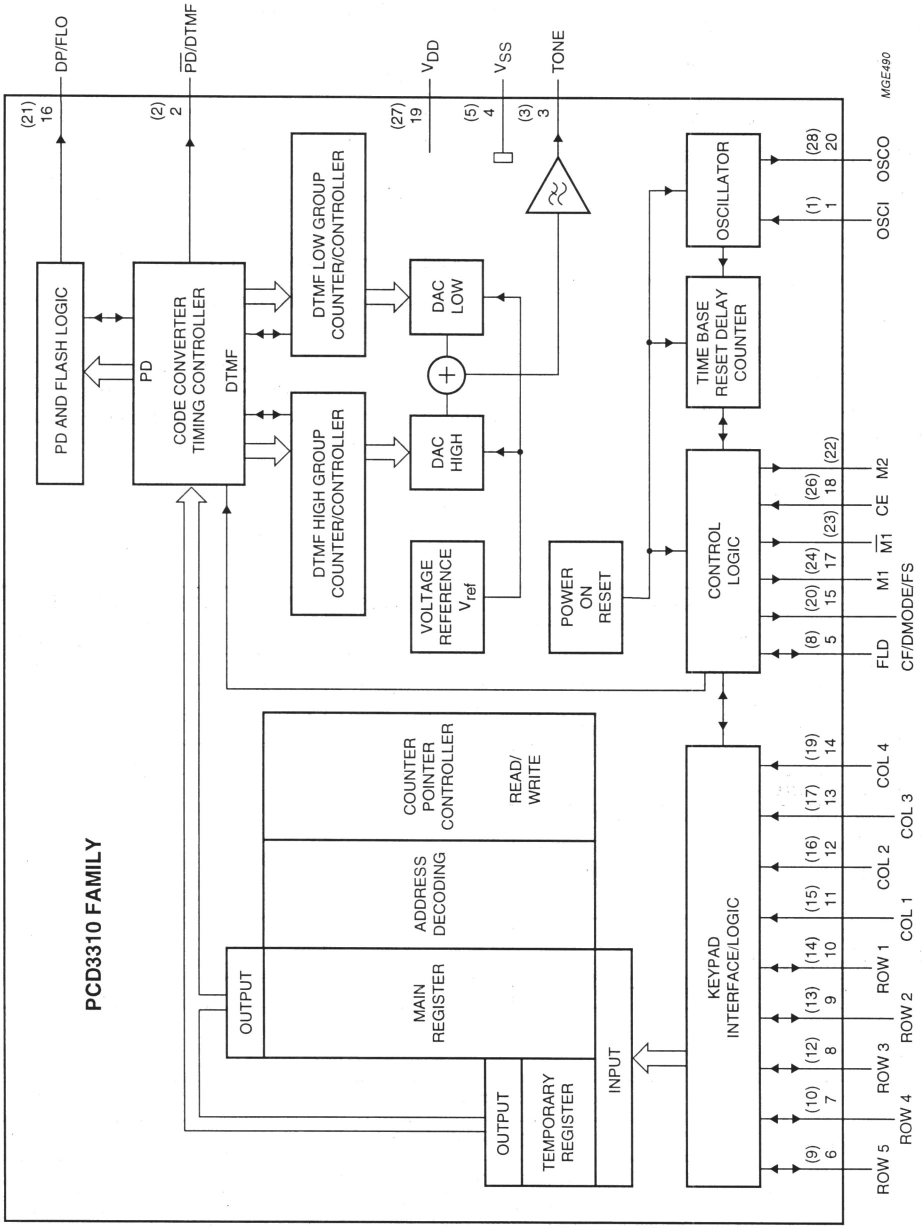
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		2.5	–	6.0	V
V_{DDO}	standby supply voltage		1.8	–	6.0	V
I_{DDO}	low standby current (on hook)	V_{DDO} = 1.8 V	–	–	2	μA
I_{DDC}	operating current in conversation mode	V_{DD} = 3 V	–	–	150	μA
I_{DDP}	operating current in pulse dialling mode	V_{DD} = 3 V	–	–	200	μA
I_{DDF}	operating current in DTMF dialling mode	V_{DD} = 3 V	–	0.6	0.9	mA
$V_{HG(rms)}$	DTMF output voltage level for HIGH group (RMS value)		–	192	–	mV
$V_{LG(rms)}$	DTMF output voltage level for LOW group (RMS value)		–	150	–	mV
ΔV_G	pre-emphasis of group		–	2.1	–	dB
THD	total harmonic distortion		–	–25	–	dB
T_{amb}	operating ambient temperature		–25	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3310P	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCD3310AP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCD3310T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3310AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM


DP/FLO
(21)
16
$\overline{PD}$/DTMF
(2)
2
V$_{DD}$
(27)
19
V$_{SS}$
(5)
4
TONE
(3)
3
MGE490
PD AND FLASH LOGIC
CODE CONVERTER
TIMING CONTROLLER
PD
DTMF
DTMF LOW GROUP
COUNTER/CONTROLLER
DTMF HIGH GROUP
COUNTER/CONTROLLER
DAC
LOW
DAC
HIGH
+
VOLTAGE
REFERENCE
V$_{ref}$
POWER
ON
RESET
OSCILLATOR
TIME BASE
RESET DELAY
COUNTER
CONTROL
LOGIC
(28)
20
OSCO
(1)
1
OSCI
(22)
M2
(26)
18
CE
(23)
$\overline{M1}$
(24)
17
M1
(20)
15
CF/DMODE/FS
(8)
5
FLD
PCD3310 FAMILY
COUNTER
POINTER
CONTROLLER
READ/
WRITE
ADDRESS
DECODING
MAIN
REGISTER
OUTPUT
OUTPUT
TEMPORARY
REGISTER
INPUT
KEYPAD
INTERFACE/LOGIC
(19)
14
COL 4
(17)
13
COL 3
(16)
12
COL 2
(15)
11
COL 1
(14)
10
ROW 1
(13)
9
ROW 2
(12)
8
ROW 3
(10)
7
ROW 4
(9)
6
ROW 5

The pin numbers given in parenthesis refer to the PCD3310T.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	DIP20	SO28	
OSCI	1	1	oscillator input
$\overline{PD}$/DTMF	2	2	select pin; pulse or DTMF dialling output
TONE	3	3	single or dual tone frequency output
n.c.	–	4	not connected
V_{SS}	4	5	negative supply
n.c.	–	6	not connected
n.c.	–	7	not connected
FLD	5	8	flash duration control input/output
ROW 5	6	9	scanning row 5 keyboard input/output
ROW 4	7	10	scanning row 4 keyboard input/output
n.c.	–	11	not connected
ROW 3	8	12	scanning row 3 keyboard input/output
ROW 2	9	13	scanning row 2 keyboard input/output
ROW 1	10	14	scanning row 1 keyboard input/output
COL 1	11	15	sense column 1 keyboard input (with internal pull-up resistor)
COL 2	12	16	sense column 2 keyboard input (with internal pull-up resistor)
COL 3	13	17	sense column 3 keyboard input (with internal pull-up resistor)
n.c.	–	18	not connected
COL 4	14	19	sense column 4 keyboard input (with internal pull-up resistor)
CF/DMODE/FS	15	20	confidence tone/dialling mode/frequency select outputs
DP/FLO	16	21	dialling pulse and flash output
M2	–	22	muting output 2
$\overline{M1}$	–	23	muting output 1 (active LOW)
M1	17	24	muting output 1
n.c.	–	25	not connected
CE	18	26	chip enable input
V_{DD}	19	27	positive supply voltage
OSCO	20	28	oscillator output

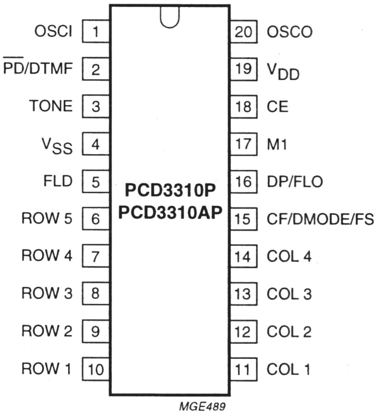

OSCI 1
$\overline{PD}$/DTMF 2
TONE 3
V_{SS} 4
FLD 5
ROW 5 6
ROW 4 7
ROW 3 8
ROW 2 9
ROW 1 10
20 OSCO
19 V_{DD}
18 CE
17 M1
16 DP/FLO
15 CF/DMODE/FS
14 COL 4
13 COL 3
12 COL 2
11 COL 1
PCD3310P
PCD3310AP
MGE489

Fig.2 Pin configuration (DIP20).

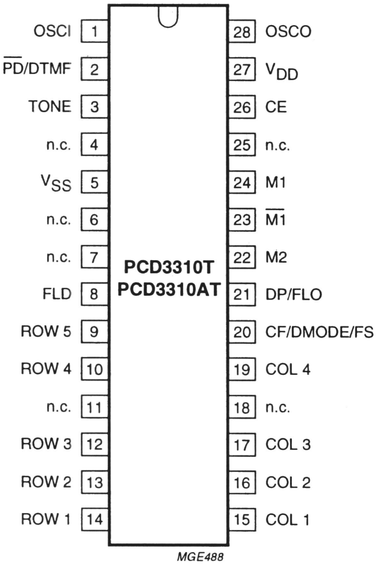

OSCI 1
$\overline{PD}$/DTMF 2
TONE 3
n.c. 4
V_{SS} 5
n.c. 6
n.c. 7
FLD 8
ROW 5 9
ROW 4 10
n.c. 11
ROW 3 12
ROW 2 13
ROW 1 14
28 OSCO
27 V_{DD}
26 CE
25 n.c.
24 M1
23 $\overline{M1}$
22 M2
21 DP/FLO
20 CF/DMODE/FS
19 COL 4
18 n.c.
17 COL 3
16 COL 2
15 COL 1
PCD3310T
PCD3310AT
MGE488

Fig.3 Pin configuration (SO28).

Table 1 The PCD3310 family of ICs

TYPE NUMBER	DESCRIPTION
PCD3310	P/T dialler with redial, notepad, 4 × 5 keypad, flash, mark/space ratio 2 : 1, PABX register, automatic access pause control access to the cursor method
PCD3310A	item PCD3310 with 3 : 2 mark/space ratio

Table 2 PCD3310 family survey

FUNCTION	PCD3310	PCD3310A
Redial key	R	R
Notepad keys; note 1	P/R	P/R
Mixed mode entry $\overline{PD}$/DTMF + tone	* # A – D	* # A – D
Mixed mode entry $\overline{PD}$/DTMF no tone	>	>
Keypad (4 × 5, A – D)	3 × 5	3 × 5
Pulse dial; break/make 10 Hz, t_{id} = 840 ms; 20 Hz, t_{id} = 504 ms	67, 33	60, 40
DTMF dial; tone/pause (ms)	70, 70	70, 70
DTMF dial; mute hold-over	80	80
Flash (ms)	100+	100+
Pin 15 (SOT146-1)	CF	CF
Pin 20 (SOT136-1)	CF	CF
Memory main, data	23	23
Memory PABX	5	5
SOT146-1 package	20	20
SOT136-1 package	28	28

Note

1. P = program, R = dial.

FUNCTIONAL DESCRIPTION

Power supply (V_{DD} and V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the Chapter “Characteristics”. To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum standby supply voltage of 1.8 V the power-on reset circuit inhibits redialling after hook-off. The power-on reset signal has the highest priority; it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI and OSCO)

The timebase for the circuit for both $\overline{PD}$ and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3.58 MHz crystal or ceramic resonator between the OSCI and OSCO pins. Recommended resonator type:

- 3.58 MHz PXE - Murata; CSA 3.58MG310VA.

Chip enable (CE)

The CE input enables the circuit and is used to initialize the device.

When CE is LOW it provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary Write Address Counter (TWAC) which point to the last entered digit (see Fig.6). The keyboard input is inhibited, but data previously entered is saved in the redial register provided V_{DD} is higher than $V_{DDO(min)}$. The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

When CE is HIGH it activates the clock oscillator and the circuit changes from static standby condition to the conversion mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for longer than time period t_{rd} (see Fig.11, Fig.12 and Chapter “Timing characteristics”) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of < t_{rd} will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{\text{PD}}$/DTMF)

$\overline{\text{PD}}$ MODE

If $\overline{\text{PD}}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF MODE

If $\overline{\text{PD}}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function key activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations. Harmonic content is filtered out thus meeting the *CEPT CS 203* recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual key depression time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

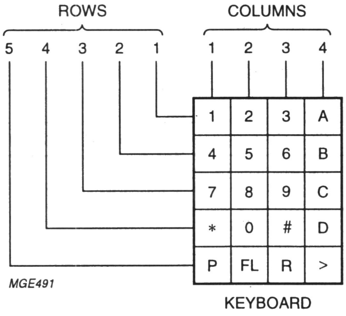
MIXED MODE

When the $\overline{\text{PD}}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (Flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric key (A, B, C, D, *, # or >) is activated. The circuit then changes to DTMF dialling for data communication and remains in this state until FL is activated or a after a static standby condition when CE is re-activated.

A connection between the $\overline{\text{PD}}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{\text{PD}}$/DTMF pin to V_{SS} sets the circuits back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the circuit are connected to the keyboard as shown in Fig.4. All keyboard entries are debounced on both the leading and trailing edges for approximately time period t_e as shown in Figs 11, 12, 13 and 14. Each entry is tested for validity. When a key is depressed, keyboard scanning starts and only returns to the sense mode after release of that key.



1	2	3	A
4	5	6	B
7	8	9	C
*	0	#	D
P	FL	R	>

Fig.4 Keyboard organization.

ROW 5 of the keyboard contains the following special function keys:

- P = memory clear and programming (notepad)
- FL = flash or register recall
- R = redial
- > = change of dial mode from $\overline{\text{PD}}$ to DTMF in mixed dialling mode.

In the pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, R and FL.

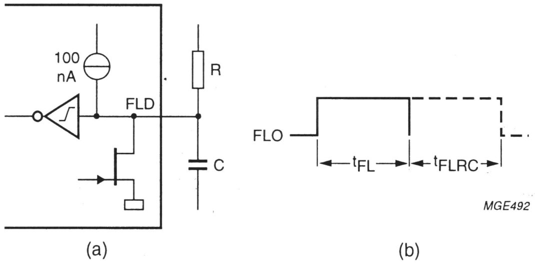
In the DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, FL and R.

In the mixed mode all key entries are valid and executed accordingly.

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling modes.

Pressing the FL key will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. The flash pulse duration (t_{fl}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig.5). The flash pulse resets the Read Address Counter (RAC). Later redial is possible (see Fig.9). The counter of the reset delay time is held during the period of t_{FL}.



Where $t_{FLRC} \approx R \times C$.

Fig.5 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched capacitor filter, followed by an on-chip active RC low-pass filter. Hence, the total harmonic distortion of the DTMF tones meets the *CEPT CS 203* recommendations. The tone output has the following states:

- tone OFF; 3-state
- tone ON; the associated frequencies are superimposed on a DC level of $\frac{1}{2}V_{DD}$.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency.

High group frequencies are generated by connecting the column to V_{SS} and LOW group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

An on-chip reference voltage provides output tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling.

Table 3 Frequency tolerance of the output tones for DTMF signalling; f_{xtal} = 3.579545 MHz

ROW/COLUMN	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION	
			%	Hz
ROW 1	697	607.90	+0.13	+0.90
ROW 2	770	770.46	+0.06	+0.46
ROW 3	852	850.45	−0.18	−1.55
ROW 4	941	943.23	+0.24	+2.23
COL 1	1209	1206.45	−0.21	−2.55
COL 2	1336	1341.66	+0.42	+5.66
COL 3	1477	1482.21	+0.35	+5.21
COL 4	1633	1638.24	+0.32	+5.25

Dial pulse and Flash output (DP/FLO)

This is a combined output which provides control signals for timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{\text{M1}}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

Muting output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling. It is an open drain p-channel output.

DIALLING PROCEDURES (see Figs 7, 8 and 9)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address, (see Fig.6). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated Write Address Counter (WAC). After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected.

All entries are debounced on both the leading and trailing edges for at least time period t_e as shown in Figs 11, 12, 13 and 14.

Each entry is tested for validity before being stored in the redial register.

- In the DTMF mode all non-function keys are valid
- In the $\overline{\text{PD}}$ mode only numeric keys are valid.

Simultaneous to their acceptance and corresponding to the selected mode ($\overline{\text{PD}}$, DTMF or mixed), the entries are transmitted as $\overline{\text{PD}}$ pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling; they are neither stored nor transmitted.

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The circuit is in the conversation mode. If ‘R’ is the first keyboard entry the circuit starts redialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the redialling continues in the main register.

If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing ‘R’ a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling. No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear (‘P’ without successive data entry)
- Memory overflow (more than 23 valid data entries).

Notepad

The redial register can also be used as a notepad. In the conversation mode a number with up to 23 digits can be entered and stored for redialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, redialling will be possible after flash or hook-on and hook-off.

During notepad programming the numbers entered will not be transmitted nor is the mute active, only the confidence tone is generated.

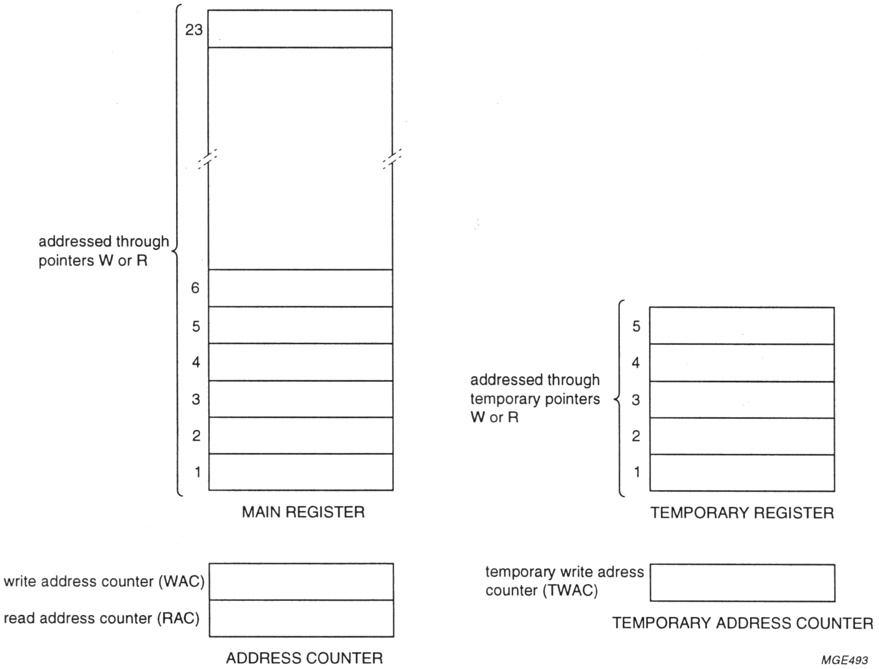
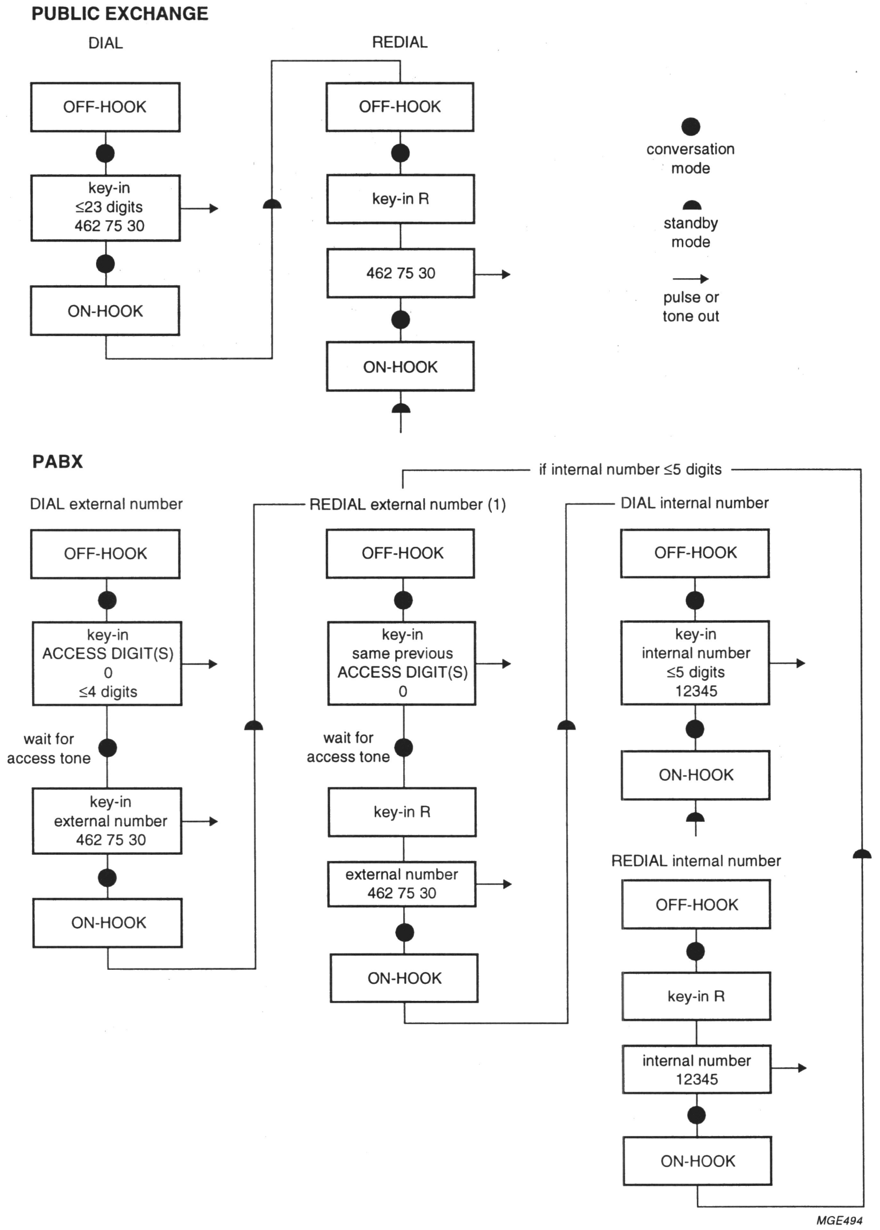

23
addressed through pointers W or R
6
5
4
3
2
1
MAIN REGISTER
write address counter (WAC)
read address counter (RAC)
ADDRESS COUNTER
addressed through temporary pointers W or R
5
4
3
2
1
TEMPORARY REGISTER
temporary write adress counter (TWAC)
TEMPORARY ADDRESS COUNTER
MGE493

Fig.6 Program memory map.


PUBLIC EXCHANGE
DIAL
REDIAL
OFF-HOOK
key-in
≤23 digits
462 75 30
ON-HOOK
OFF-HOOK
key-in R
462 75 30
ON-HOOK
conversation mode
standby mode
pulse or tone out
PABX
DIAL external number
REDIAL external number (1)
DIAL internal number
if internal number ≤5 digits
OFF-HOOK
key-in
ACCESS DIGIT(S)
0
≤4 digits
wait for access tone
key-in
external number
462 75 30
ON-HOOK
OFF-HOOK
key-in
same previous
ACCESS DIGIT(S)
0
wait for access tone
key-in R
external number
462 75 30
ON-HOOK
OFF-HOOK
key-in
internal number
≤5 digits
12345
ON-HOOK
REDIAL internal number
OFF-HOOK
key-in R
internal number
12345
ON-HOOK
MGE494

(1) If [access digit(s) + external number] ≤23 digits.

Fig.7 PD or DTMF dialling mode.

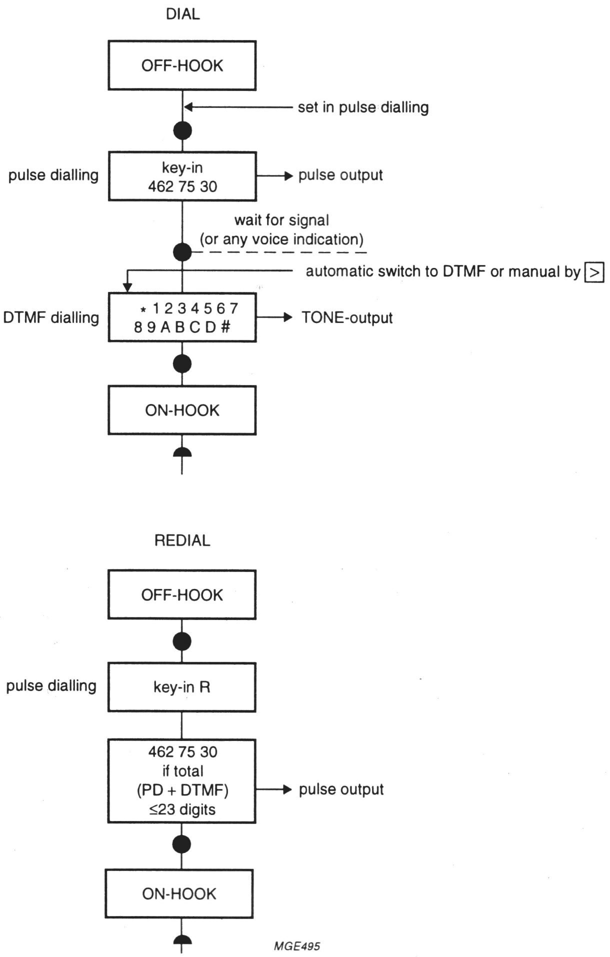

DIAL
OFF-HOOK
set in pulse dialling
pulse dialling
key-in
462 75 30
pulse output
wait for signal
(or any voice indication)
automatic switch to DTMF or manual by >
DTMF dialling
* 1 2 3 4 5 6 7
8 9 A B C D #
TONE-output
ON-HOOK
REDIAL
OFF-HOOK
pulse dialling
key-in R
462 75 30
if total
(PD + DTMF)
≤23 digits
pulse output
ON-HOOK
MGE495

Fig.8 $\overline{\text{PD}}$/DTMF mixed-mode dialling.

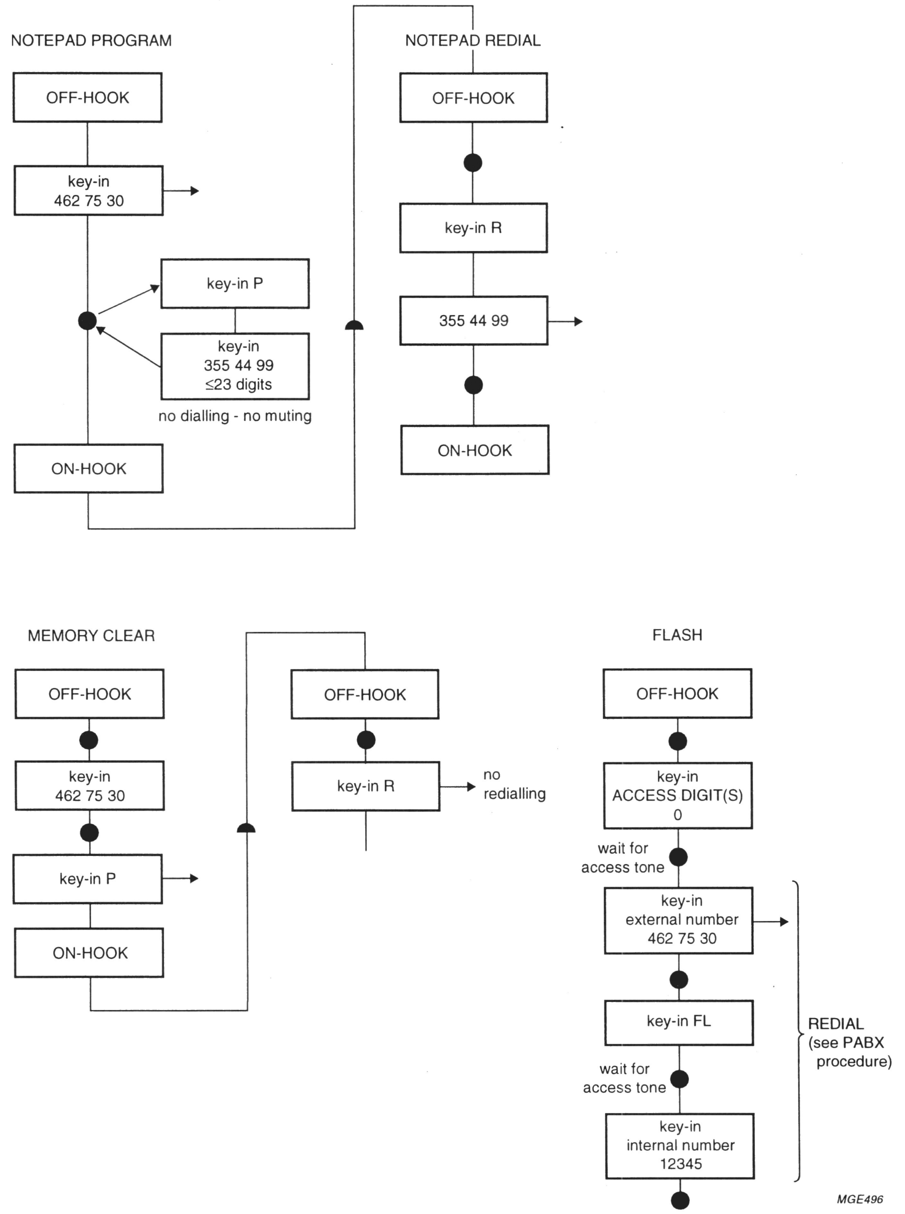

NOTEPAD PROGRAM
OFF-HOOK
key-in
462 75 30
key-in P
key-in
355 44 99
≤23 digits
no dialling - no muting
ON-HOOK
NOTEPAD REDIAL
OFF-HOOK
key-in R
355 44 99
ON-HOOK
MEMORY CLEAR
OFF-HOOK
key-in
462 75 30
key-in P
ON-HOOK
OFF-HOOK
key-in R
no
redialling
FLASH
OFF-HOOK
key-in
ACCESS DIGIT(S)
0
wait for
access tone
key-in
external number
462 75 30
key-in FL
wait for
access tone
key-in
internal number
12345
REDIAL
(see PABX
procedure)
MGE496

Fig.9 Notepad, memory clear, flash; independent of dialling mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+8.0	V
I_{DD}	supply current	–	50	mA
$I_{I,O}$	DC current into any input or output	–	±10	mA
V_I	all input voltages	–0.8	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation	–	300	mW
P_o	power dissipation per output	–	50	mW
T_{stg}	storage temperature range	–65	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz; T_{amb} = –25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.5	–	6.0	V
V_{DDO}	standby supply voltage		1.8	–	6.0	V
I_{DDC}	operating supply current in conversation mode	oscillator ON	–	–	150	μA
I_{DDP}	operating supply current in pulse dialling or flash		–	–	200	μA
I_{DDF}	operating supply current in DTMF dialling	tone ON	–	0.6	0.9	mA
		one OFF	–	–	200	μA
I_{DDO}	standby supply current	V_{DD} = 1.8 V oscillator OFF; note 1	–	2	4	μA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$\lvert I_{IL} \rvert$	input leakage current pin CE		–	–	1	μA
Keyboard inputs						
R_{KON}	keyboard ON resistance		–	–	2	kΩ
R_{KOFF}	keyboard OFF resistance		1	–	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
I_{Osink}	output sink current pins M1, $\overline{\text{M1}}$, DP/FLO, CF and FLD	$V_{OL} = V_{SS} + 0.5$ V	0.7	–	–	mA
	output sink current pin $\overline{\text{PD}}$/DTMF	$V_{OL} = V_{SS} + 0.5$ V; note 2	–	–	1	mA
$I_{Osource}$	output source current pins M1, $\overline{\text{M1}}$, DP/FLO, CF and M2	$V_{OH} = V_{DD} - 0.5$ V	−0.6	–	–	mA
	output source current pin $\overline{\text{PD}}$/DTMF	$V_{OH} = V_{DD} - 0.5$ V; note 2	–	–	−1	mA
	output source current pin FLD	$V_{OH} = V_{DD} - 0.5$ V; note 3	–	−60	–	nA
Timing and frequency						
t_{on}	clock start-up time		–	4	–	ms
t_e	debounce time		–	12	–	ms
t_{rd}	reset delay time		–	160	–	ms
Tone output (see Fig.10)						
$V_{HG(rms)}$	DTMF output voltage levels for HIGH group (RMS value)	$V_{DD} = 2.5$ to 6 V	158	192	205	mV
$V_{LG(rms)}$	DTMF output voltage levels for LOW group (RMS value)	$V_{DD} = 2.5$ to 6 V	125	150	160	mV
Δf	frequency deviation		−0.6	–	+0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	0.1	0.5	kΩ
ΔV_G	pre-emphasis of group		1.85	2.1	2.35	dB
THD	total harmonic distortion	$T_{amb} = 25$ °C, note 4	–	−25	–	dB

Notes

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. $<\lvert 10\text{ mA} \rvert$ dynamic current to set/reset $\overline{\text{PD}}$/DTMF pin (mixed mode).
3. Flash inactive; $V_{OH} = V_{SS}$.
4. Related to the level of the LOW group frequency component (*CEPT CS 203*).

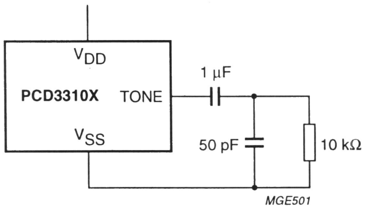
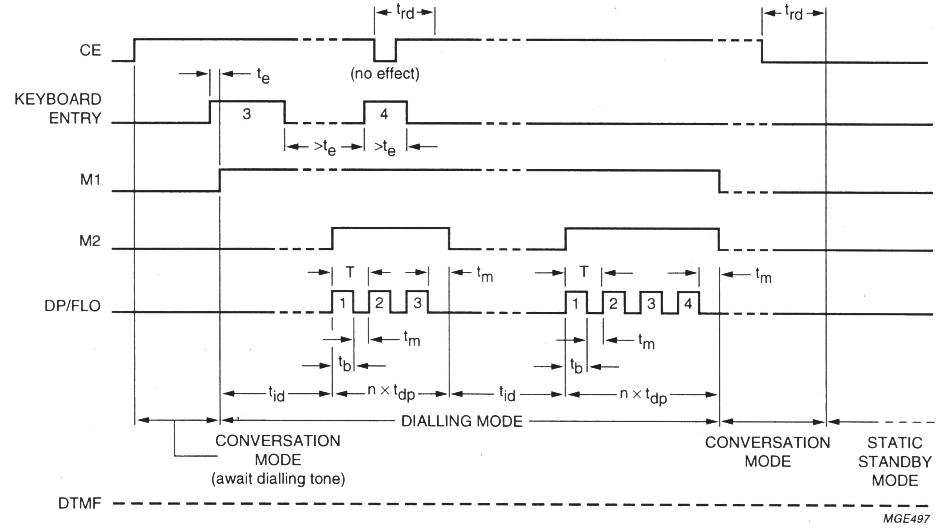


Fig.10 Tone output test circuit.

TIMING CHARACTERISTICS

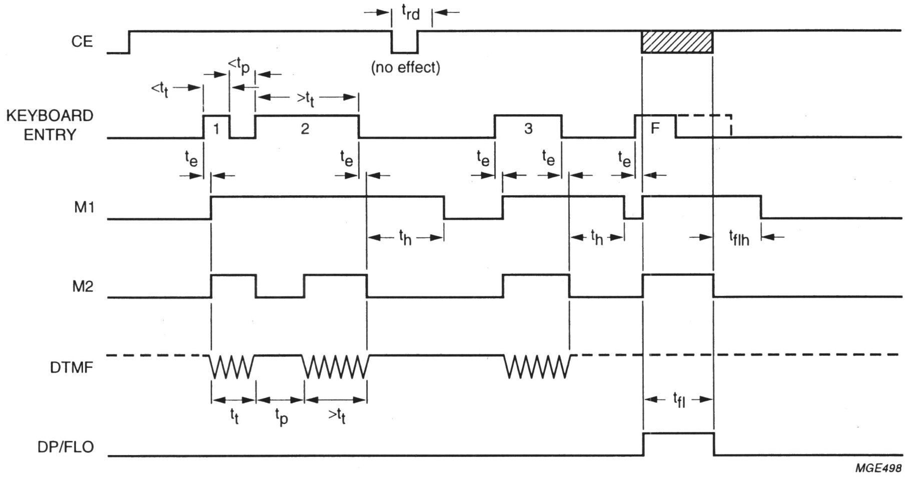
When any key is activated a square wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time (PCD3310 and PCD3310A)					
t_t, t_p	manual dialling	68	–	–	ms
t_t, t_p	redialling	68	70	72	ms
t_{fl}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling (PCD3310)					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms
Pulse dialling (PCD3310A)					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	59	60	61	ms
t_m	make time	39	40	41	ms


CE
KEYBOARD ENTRY
M1
M2
DP/FLO
DTMF
t_{rd}
t_e
(no effect)
3
4
$>t_e$
T
t_m
t_b
1
2
3
4
t_{id}
$n \times t_{dp}$
DIALLING MODE
CONVERSATION MODE (await dialling tone)
CONVERSATION MODE
STATIC STANDBY MODE
MGE497

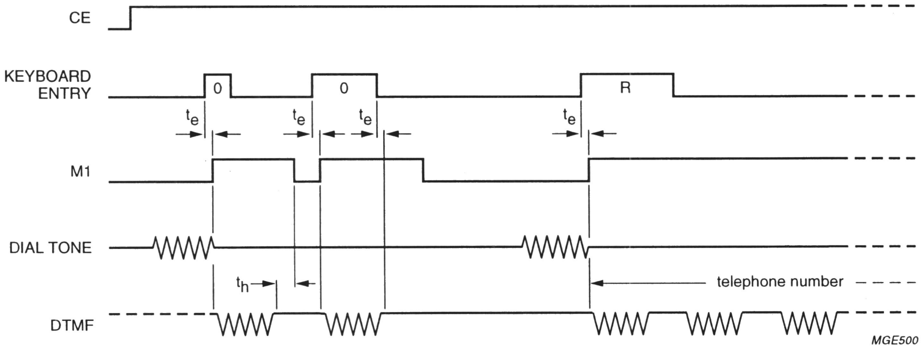
The dashed line signifies floating.

Fig.11 Timing diagram for pulse dialling ($\overline{PD}$/DTMF = V_{SS}).


t_rd
CE
(no effect)
<t_p
<t_t
>t_t
KEYBOARD ENTRY
1
2
3
F
t_e
t_e
t_e
t_e
t_e
M1
t_h
t_h
t_flh
M2
DTMF
t_t
t_p
>t_t
t_fl
DP/FLO
MGE498

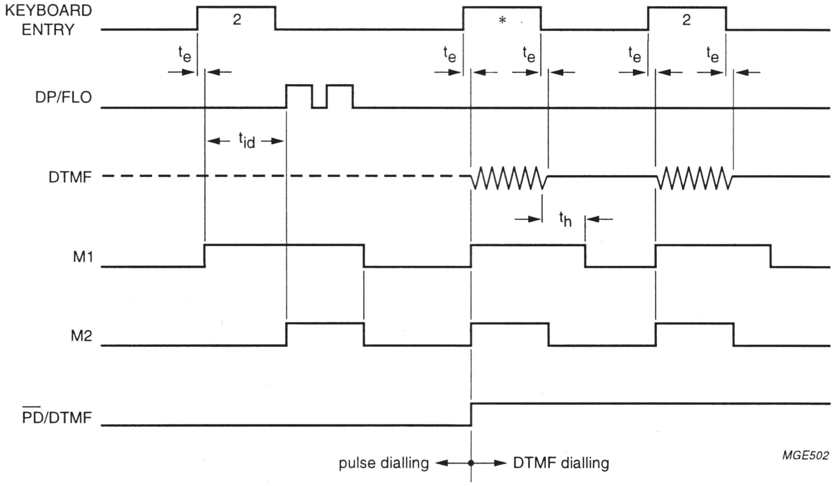
The dashed line signifies floating.

Fig.12 Timing diagram for DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).


CE
KEYBOARD ENTRY
0
0
R
t_e
t_e
t_e
t_e
M1
DIAL TONE
t_h
telephone number
DTMF
MGE500

The dashed line signifies floating.

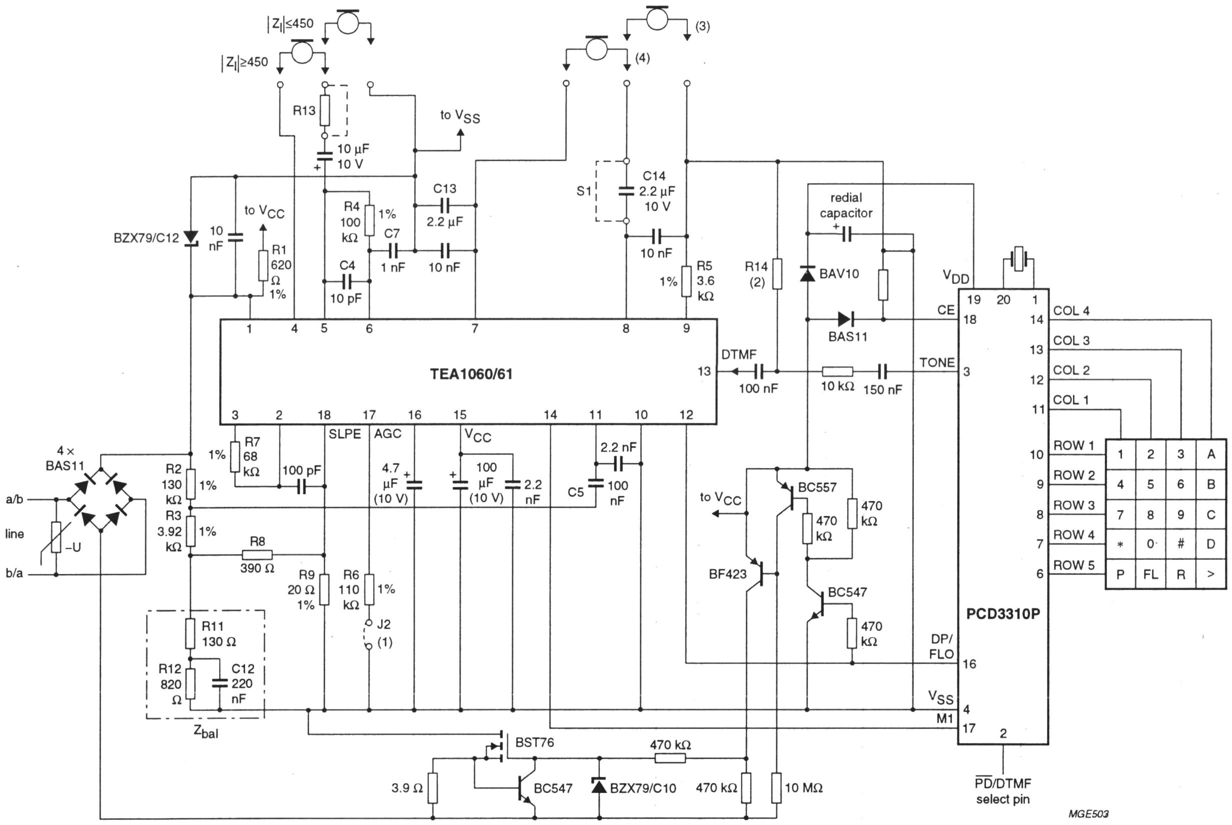
Fig.13 .Timing diagram showing REDIAL where PABX access digits are the first keyboard entries in DTMF dialling mode


KEYBOARD ENTRY
2
*
2
t_e
t_e
t_e
t_e
t_e
DP/FLO
t_{id}
DTMF
t_h
M1
M2
$\overline{PD}$/DTMF
pulse dialling
DTMF dialling
MGE502

The dashed line signifies floating.

Fig.14 .Timing diagram for mixed mode ($\overline{PD}$/DTMF open-circuit)

APPLICATION INFORMATION


|Z_I|≤450
|Z_I|≥450
(3)
(4)
R13
10 µF
10 V
to V_SS
C13
2.2 µF
R4
100
kΩ
1%
C7
1 nF
10 nF
C4
10 pF
to V_CC
10
nF
R1
620
Ω
1%
BZX79/C12
S1
C14
2.2 µF
10 V
10 nF
R5
3.6
kΩ
1%
R14
(2)
redial
capacitor
BAV10
BAS11
V_DD
CE
TONE
DTMF
100 nF
10 kΩ
150 nF
TEA1060/61
SLPE
AGC
V_CC
R7
68
kΩ
1%
100 pF
4.7
µF
(10 V)
100
µF
(10 V)
2.2
nF
2.2 nF
C5
100
nF
4 ×
BAS11
a/b
line
b/a
–U
R2
130
kΩ
1%
R3
3.92
kΩ
1%
R8
390 Ω
R9
20 Ω
1%
R6
110
kΩ
1%
J2
(1)
R11
130 Ω
R12
820
Ω
C12
220
nF
Z_bal
to V_CC
BC557
470
kΩ
470
kΩ
BF423
BC547
470
kΩ
BST76
3.9 Ω
BC547
BZX79/C10
470 kΩ
470 kΩ
10 MΩ
PCD3310P
COL 4
COL 3
COL 2
COL 1
ROW 1
ROW 2
ROW 3
ROW 4
ROW 5
DP/
FLO
V_SS
M1
PD/DTMF
select pin
1 2 3 A
4 5 6 B
7 8 9 C
* 0 # D
P FL R >
MGE503

(1) Automatic line compensation obtained by connecting R6 to V_{SS}.

(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060 and TEA1061.

(3) Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060).

(4) Asymmetrical high-impedance inputs for electret microphones (TEA1061).

Fig.15 Application diagram of the full electronic basic telephone set.

PCD3311C
PCD3312C

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C-bus).

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT T/CS46-03 (= former CS203) recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C-bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (RMS values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	−25	–	dB
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

PCD3311CP: 14-lead DIL; plastic (SOT27).
PCD3311CT: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312CP: 8-lead DIL; plastic (SOT97).
PCD3312CT: 8-lead mini-pack; plastic (SO8L; SOT176C).

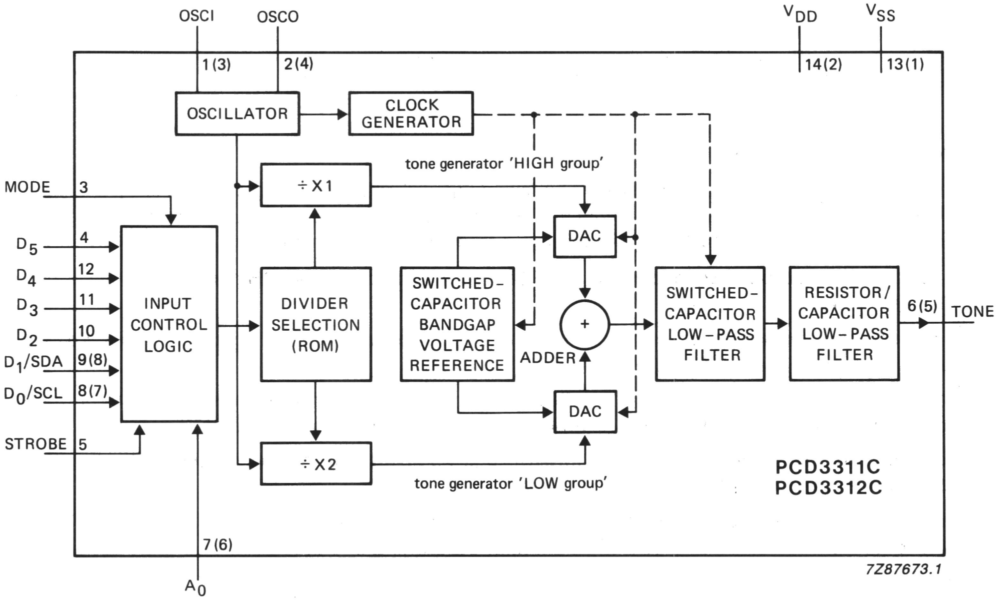

OSCI
OSCO
1 (3)
2 (4)
VDD
VSS
14 (2)
13 (1)
OSCILLATOR
CLOCK GENERATOR
tone generator 'HIGH group'
MODE
3
÷ X1
D5
4
D4
12
D3
11
D2
10
D1/SDA
9 (8)
D0/SCL
8 (7)
STROBE
5
INPUT CONTROL LOGIC
DIVIDER SELECTION (ROM)
SWITCHED-CAPACITOR BANDGAP VOLTAGE REFERENCE
DAC
+
ADDER
DAC
SWITCHED-CAPACITOR LOW-PASS FILTER
RESISTOR/CAPACITOR LOW-PASS FILTER
6 (5)
TONE
÷ X2
tone generator 'LOW group'
PCD3311C
PCD3312C
7 (6)
A0
7Z87673.1

Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312C.

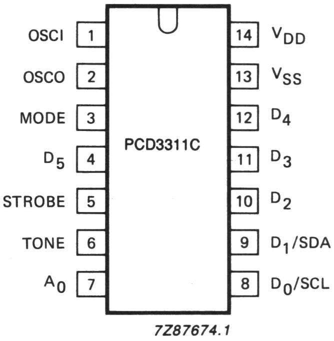

OSCI 1
OSCO 2
MODE 3
D5 4
STROBE 5
TONE 6
A0 7
14 VDD
13 VSS
12 D4
11 D3
10 D2
9 D1/SDA
8 D0/SCL
PCD3311C
7Z87674.1

Fig. 2 Pinning diagram for the PCD3311CP.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
9	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

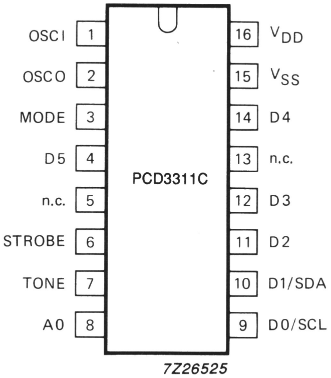

OSCI 1
OSCO 2
MODE 3
D5 4
n.c. 5
STROBE 6
TONE 7
A0 8
16 VDD
15 VSS
14 D4
13 n.c.
12 D3
11 D2
10 D1/SDA
9 D0/SCL
PCD3311C
7Z26525

Fig. 3 Pinning diagram for the PCD3311CT.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D_0/SCL	parallel data input* or serial clock line (I^2C-bus)
10	D_1/SDA	parallel data input* or serial data line (I^2C-bus)
11	D_2	
12	D_3	parallel data inputs*
14	D_4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5; 13	n.c.	not connected

* MODE = HIGH.

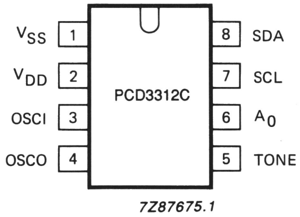

VSS 1
VDD 2
OSCI 3
OSCO 4
8 SDA
7 SCL
6 A0
5 TONE
PCD3312C
7Z87675.1

Fig. 4 Pinning diagram for the PCD3312C.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION (continued)

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

Strobe input (STROBE, only for the PCD3311C)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311C by setting MODE input LOW.

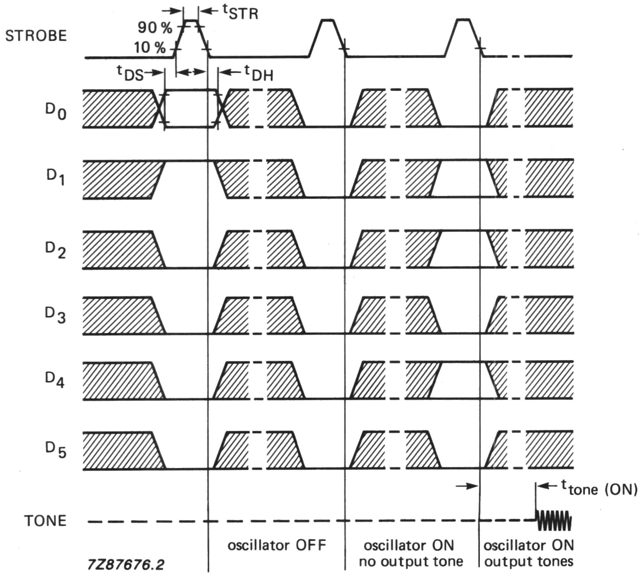


Fig. 5 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311C the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^{2}C-bus specification (see "CHARACTERISTICS OF THE I^{2}C-BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311C or PCD3312C devices are connected to the same I^{2}C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I^{2}C bus data configuration (see Fig. 6)

The PCD3311C and PCD3312C are always slave receivers in the I^{2}C-bus configuration ($R/\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311C as well as for the PCD3312C, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

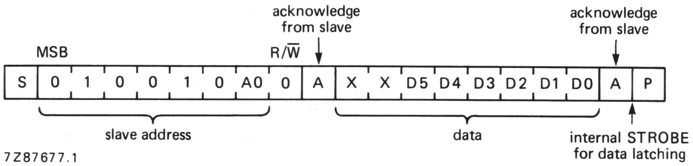


Fig. 6 I^{2}C-bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS46-03 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 2 Input data for control (no output tone; TONE in 3-state)

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation	
										%	Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation		remarks
									%	Hz	
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz **
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

CHARACTERISTICS OF THE I^{2}C-BUS

The I^{2}C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

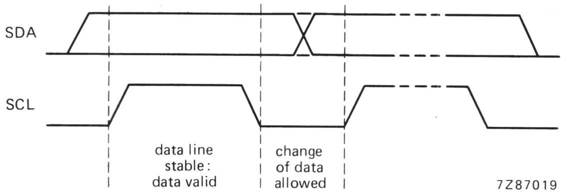


Fig. 7 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

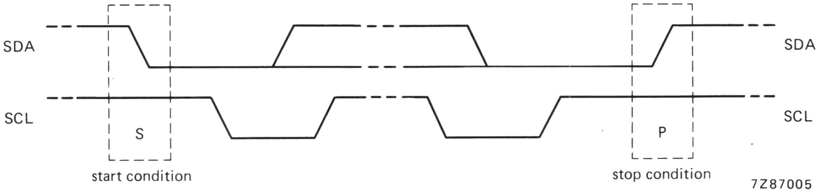


Fig. 8 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

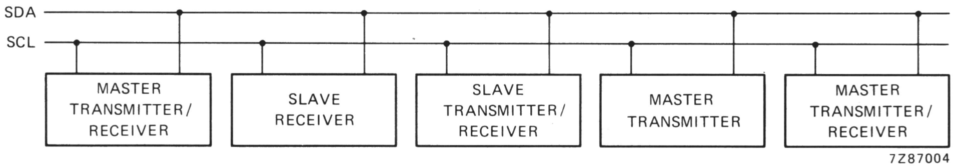

SDA
SCL
MASTER TRANSMITTER/ RECEIVER
SLAVE RECEIVER
SLAVE TRANSMITTER/ RECEIVER
MASTER TRANSMITTER
MASTER TRANSMITTER/ RECEIVER
7Z87004

Fig. 9 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

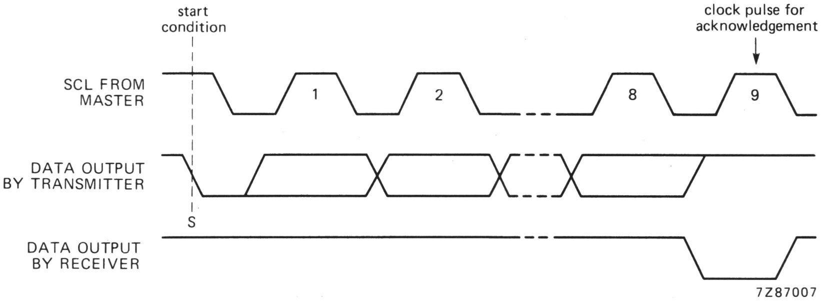

start condition
clock pulse for acknowledgement
SCL FROM MASTER
1
2
8
9
DATA OUTPUT BY TRANSMITTER
S
DATA OUTPUT BY RECEIVER
7Z87007

Fig. 10 Acknowledgement on the I^2C-bus.

CHARACTERISTICS OF THE I²C-BUS (continued)

Timing specifications

Within the I²C-bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 11.

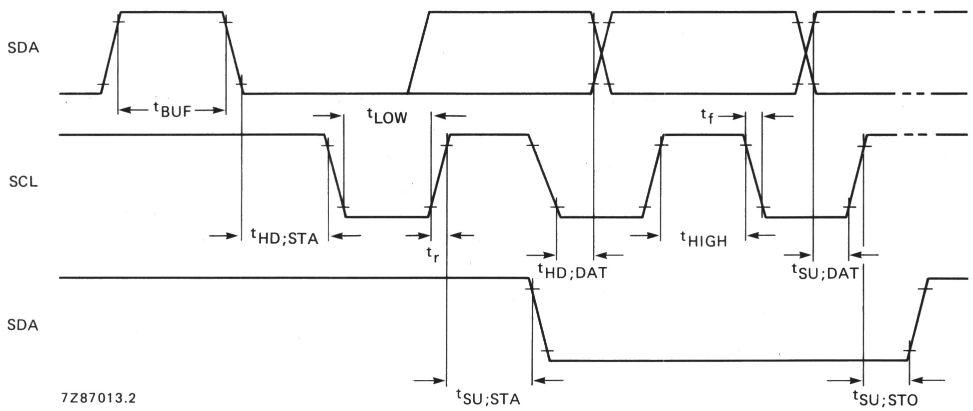


Fig. 11 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 µs	Clock LOW period
$t_{HIGHmin}$	4 µs	Clock HIGH period
$t_{SU;STA}$	$t \geq t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geq 0$ µs	Data hold time
$t_{SU;DAT}$	$t \geq 250$ ns	Data set-up time
t_r	$t \leq 1$ µs	Rise time of both the SDA and SCL line
t_f	$t \leq 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geq t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

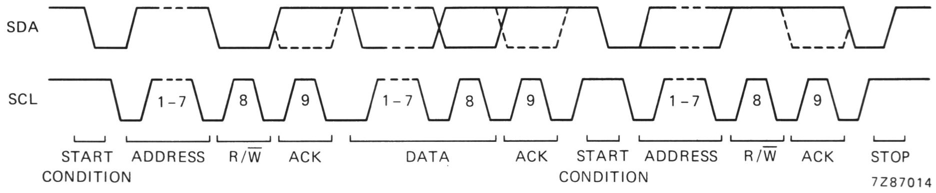

SDA
SCL
1 – 7
8
9
1 – 7
8
9
1 – 7
8
9
START CONDITION
ADDRESS
R/$\overline{W}$
ACK
DATA
ACK
START CONDITION
ADDRESS
R/$\overline{W}$
ACK
STOP
7Z87014

Fig. 12 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 µs
$t_{HIGHmin}$	4 µs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 µs and a minimum HIGH period of 365 µs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 13.

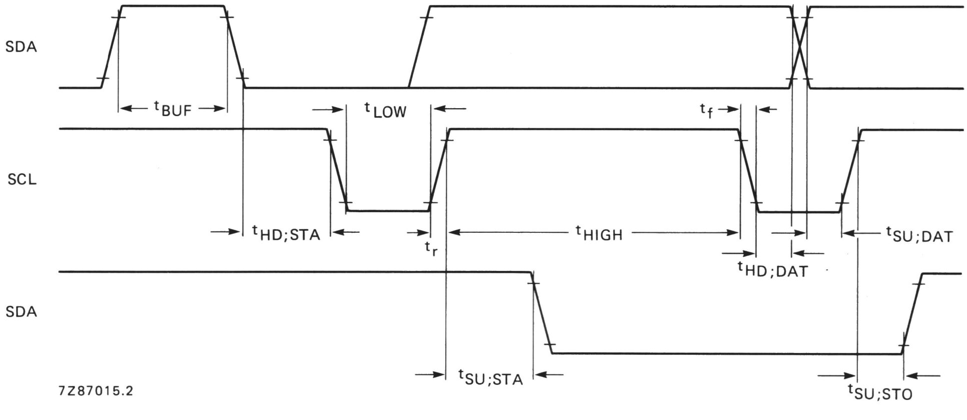

SDA
SCL
SDA
t_{BUF}
t_{LOW}
t_f
$t_{HD;STA}$
t_r
t_{HIGH}
$t_{SU;DAT}$
$t_{HD;DAT}$
$t_{SU;STA}$
$t_{SU;STO}$
7Z87015.2

Fig. 13 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

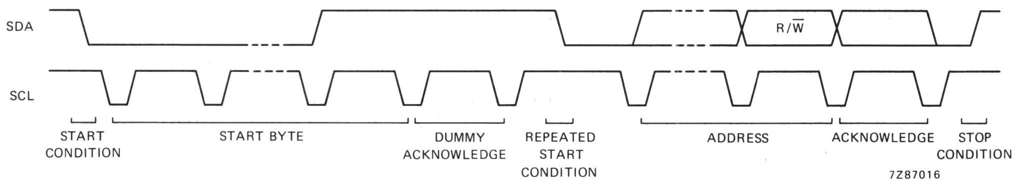

SDA
SCL
R/$\overline{W}$
START CONDITION
START BYTE
DUMMY ACKNOWLEDGE
REPEATED START CONDITION
ADDRESS
ACKNOWLEDGE
STOP CONDITION
7Z87016

Fig. 14 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

---

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	–0,8	+ 8,0	V
Input voltage range (any input)	V_I	–0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}; \pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	–25	+ 70	°C
Storage temperature range	T_{stg}	–65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = –25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,8	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 11)	f_{SCL}	–	–	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 15)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\lvert Z_O \rvert$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS46-03).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

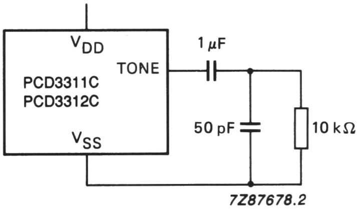

VDD
TONE
PCD3311C
PCD3312C
VSS
1 μF
50 pF
10 kΩ
7Z87678.2

Fig. 15 TONE output test circuit.

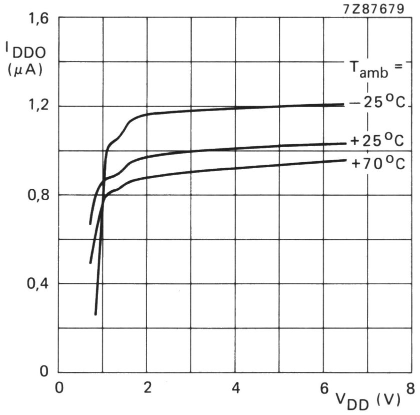


Fig. 16 Standby supply current as a function of supply voltage; oscillator OFF.

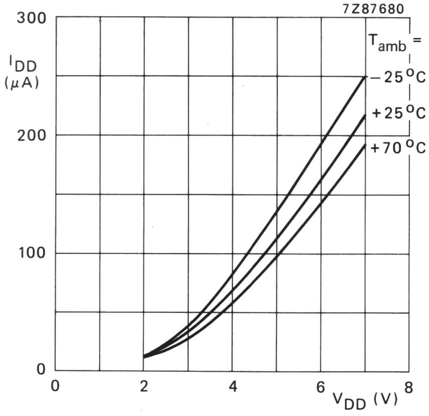


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

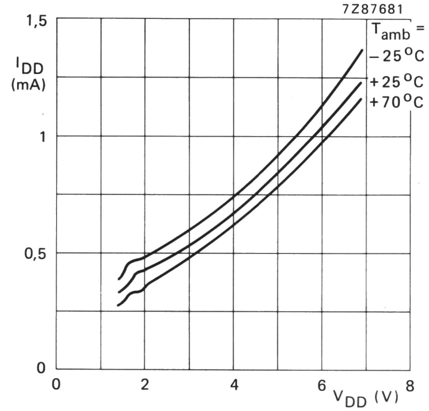


Fig. 18 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

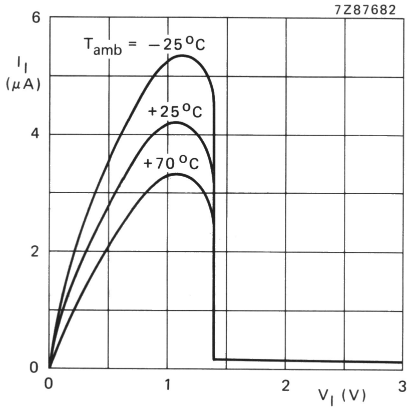


Fig. 19 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

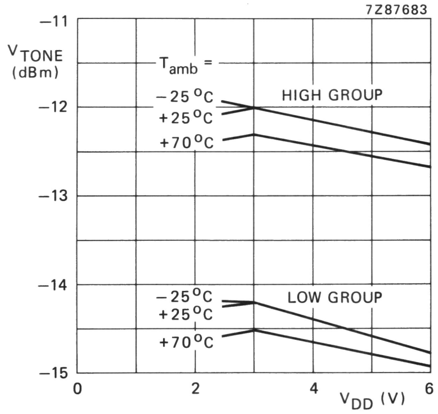


Fig. 20 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

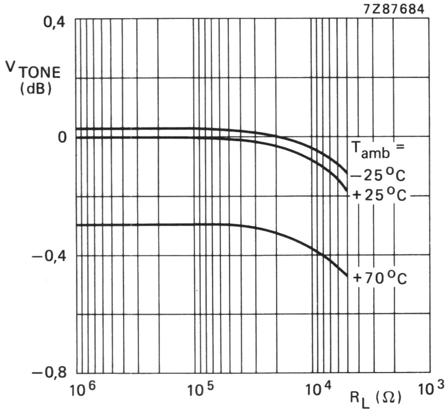


Fig. 21 Dual tone output voltage level as a function of output load resistance.

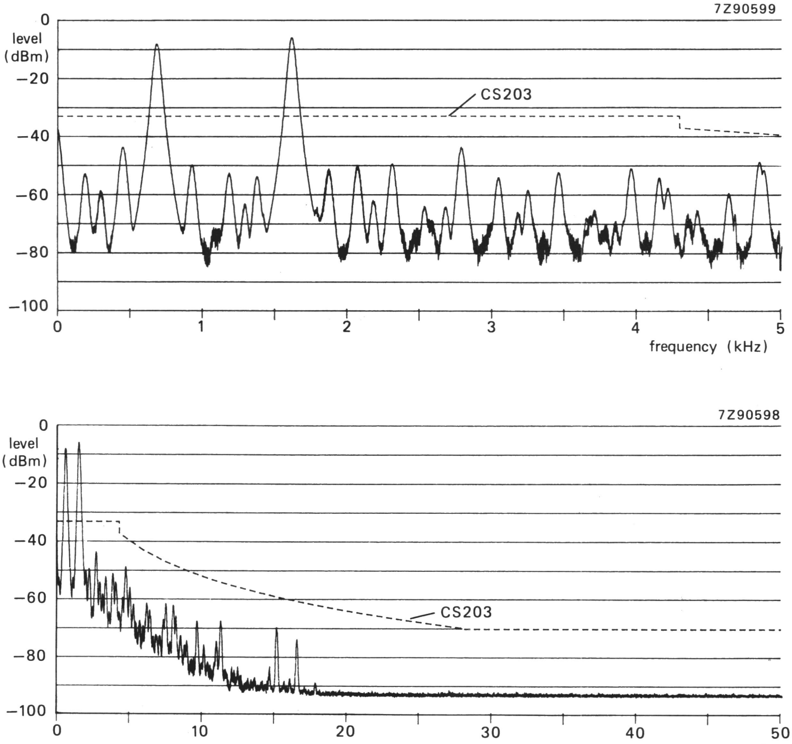


Fig. 22 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

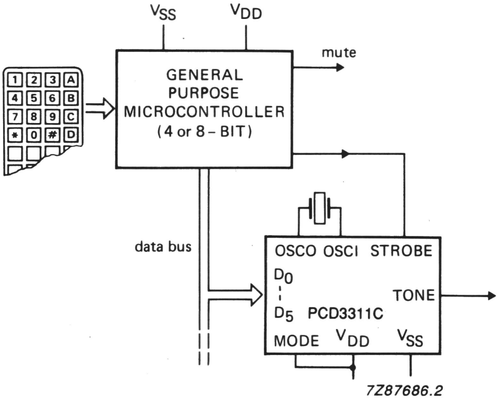

V_SS
V_DD
mute
1 2 3 A
4 5 6 B
7 8 9 C
* 0 # D
GENERAL PURPOSE MICROCONTROLLER (4 or 8 - BIT)
data bus
OSCO OSCI STROBE
D0
D5
PCD3311C
TONE
MODE V_DD V_SS
7Z87686.2

Fig. 23 PCD3311C driven by a microcontroller with parallel data bus.

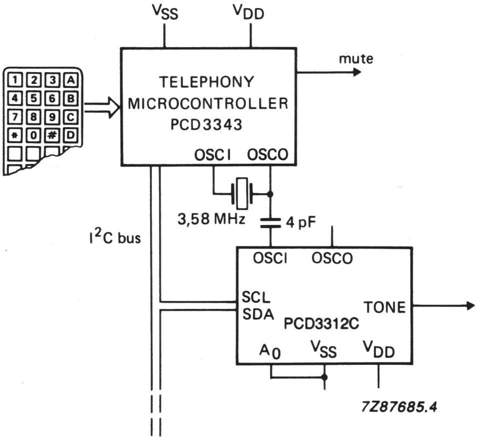

V_SS
V_DD
mute
1 2 3 A
4 5 6 B
7 8 9 C
* 0 # D
TELEPHONY MICROCONTROLLER PCD3343
OSCI OSCO
3,58 MHz
4 pF
I²C bus
OSCI OSCO
SCL
SDA
PCD3312C
TONE
A0 V_SS V_DD
7Z87685.4

Fig. 24 PCD3312C driven by telephony microcontroller PCD3343 with serial I/O (I^2C-bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311C with MODE = V_{SS}.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

Multistandard repertory dialler/ringer with EEPROM

PCD3330-1

FEATURES

Pulse/DTMF dialling

- Pulse dialling
- DTMF dialling
- Mixed mode dialling
- Number of digits per call is infinite (FIFO register)
- Flash or register recall
- Connect a/b to Earth function
- Mute functions
- Disconnect function
- Standard 4 x 4 keyboard for: 0 to 9 and *, #, A, B, C and D
- Function keys for: Flash, Hook, Mute, Tone and Disconnect
- On-hook dialling control
- Country specifications which can be stored in EEPROM are:
  Will * and/or # be transmitted when switching over to DTMF dialling mode
  Mark-to-space ratio (3 : 2 or 2 : 1)
  6 Tone time selections (60/90, 70/70, 80/80, 100/100, 100/140 or 140/140 ms)
  4 Flash time selections (100, 115, 270 or 600 ms)
  Mute output type selection (M1, $\overline{\text{M1}}$, M2 or $\overline{\text{M2}}$)
  DTMF keys or Function keys selection
- On-chip voltage reference for stabilized supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)

Number storage

- Redial Cursor method (maximum 24 digits) stored in internal EEPROM
- Storage for 13 repertory dial numbers (16 digits each) or 10 repertory dial numbers (20 digits each) in internal EEPROM
- Access pause generation and termination: manually or by Atlanta procedure
- Function keys for: LNR, Memory recall, Store, Access Pause and 1 key repertory
- Country specifications which can be stored in EEPROM are:
  Access pause time selection (1.5/1.0, 2.5/1.5, 3.0/3.5 or 6.0/6.0 s)
  10 Number repertory dialler selection (1 or 2 key)
  Two repertory number programming procedures (General or Germany)
  Repertory length (16 or 20 digits)

Ringer

- Ringer input frequency detection
- Function key for: Program Ringer
- Three-tone ringer with 4 different ringer frequencies
- Ringer melody generation with four signal speeds and four output volume steps, keypad controlled
- Country specifications which can be stored in EEPROM are:
  Ringer input frequency detection selection
  Ringer output selection (via DTMF or special RTO output)
  4 possible ringer melodies
  4 possible ringer repetition rates
  4 possible ringer volumes

General

- On-chip oscillator uses low-cost 3.58 MHz (TV colour burst) crystal or PXE resonator
- On-chip power-on reset (typically 2.0 V)
- Supply voltage range 1.8 to 6.0 V (2.5 to 6.0 V in EEPROM erase/write and DTMF and ringer mode)

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3330-1P	28	DIL	plastic	SOT117
PCD3330-1T	28	mini-pack	plastic	SO28; SOT136A

GENERAL DESCRIPTION

The PCD3330-1 is a mixed-mode multistandard repertory dialler/ringer IC frabricated in a low threshold voltage CMOS technology and is a member of the Philips family of telecommunication ICs.

The (maximum 13) repertory numbers, redial and various country specifications are stored in EEPROM so that memory retention is guaranteed for 10 years without using a battery back-up.
Therefore, different models can be created by changing the contents of some EEPROM bytes.

The various country specifications can be fulfilled by changing a few bytes in EEPROM which contain the different telephone timing and dialling procedures.

The two on-chip tone generators are used for Dual Tone Multi-Frequency (DTMF) dialling, and for generating a melody during ringing, which is activated when a correct incoming ringer frequency is detected.

As an output transducer for the ringer, a loudspeaker (ringer out via tone output) or a PXE (ringer out via the special ringer output which generates square wave ringer tones with a peak-to-peak voltage of V_{DD} to V_{SS}) can be used.

The operating supply voltage is 1.8 V (2.5 V in EEPROM erase/write and DTMF and ringer mode) to 6.0 V with a low current consumption in all operating modes: standby, conversation, dialling, programming and ringer.

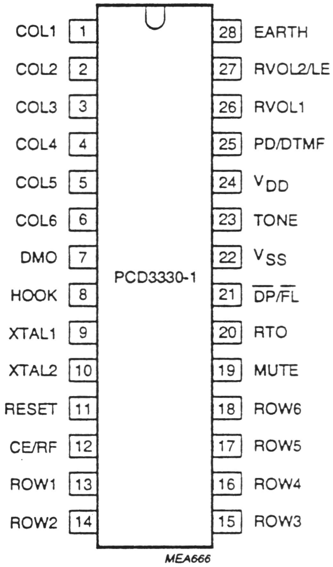

COL1 1
COL2 2
COL3 3
COL4 4
COL5 5
COL6 6
DMO 7
HOOK 8
XTAL1 9
XTAL2 10
RESET 11
CE/RF 12
ROW1 13
ROW2 14
28 EARTH
27 RVOL2/LE
26 RVOL1
25 PD/DTMF
24 V_{DD}
23 TONE
22 V_{SS}
21 $\overline{DP}/\overline{FL}$
20 RTO
19 MUTE
18 ROW6
17 ROW5
16 ROW4
15 ROW3
PCD3330-1
MEA666

Fig.1 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
COL1	1	sense column keyboard input/programming EEPROM
COL2	2	sense column keyboard input/programming EEPROM
COL3	3	sense column keyboard input/programming EEPROM
COL4	4	sense column keyboard input/programming EEPROM
COL5	5	sense column keyboard input
COL6	6	sense column keyboard input
DMO	7	dial mode output
HOOK	8	cradle contact input
XTAL1	9	crystal/PXE oscillator input
XTAL2	10	crystal/PXE oscillator output
RESET	11	reset input
CE/RF	12	chip enable and zero crossing for ringer input
ROW1	13	scanning row keyboard output
ROW2	14	scanning row keyboard output
ROW3	15	scanning row keyboard output
ROW4	16	scanning row keyboard output
ROW5	17	scanning row keyboard output
ROW6	18	scanning row keyboard output
MUTE	19	mute output
RTO	20	ringer melody output
$\overline{DP}/\overline{FL}$	21	dial pulse/flash inverted output
V_{SS}	22	negative supply
TONE	23	DTMF tones or ringer melody output
V_{DD}	24	positive supply
PD/DTMF	25	pulse/DTMF dial selection
RVOL1	26	ringer volume output 1
RVOL2/LSE	27	ringer volume output 2/loudspeaker enable output
EARTH	28	earth output

Multistandard pulse/tone repertory diallers/ringers

PCD3332-x family

FEATURES

- Pulse and DTMF mixed mode dialling
- 13 number repertory dial up to 32 digits
  - 10 direct accessible or 3 direct plus 10 two-touch
- Last number redial up to 32 digits
- Repertory and redial memory integrity check (memory contents check)
- Note pad memory function
- Flash and Earth register recall
- Access pause generation and termination
- On-chip power-on reset
- Function keys for: Program, Memory recall, Flash, LNR, Pause and Tone
- Strap functions (diode options):
  - MLA: Memory Location Access selection
  - RDS: Enable/Disable ringer validation delay (PCD3332-2)
  - DOO: enable/disable transmission * or # (PCD3332-3/S)
  - F/E: register recall Flash or Earth
  - M/S: Mark-to-Space ratio selection (3 : 2 or 2 : 1)
  - APT: Access Pause Timing selection
  - TBT: Tone Burst Time selection
  - FTS: Flash Time Selection
  - P/T: Pulse or Tone (DTMF) mode selection
  - RFS: Ringer Frequency range Selection (19.5 to 57 Hz or 14.4 to 68 Hz)
- Ringer tone generator
- Ringer-input frequency discriminator
- Ringer melody selection via keypad
- Volume control for loudspeaker phones (PCD3332-3)
- On-hook dialling/hands-free mode control (PCD3332-3)
- Pacifier tones.

GENERAL DESCRIPTION

The PCD3332-x family is a mixed-mode multistandard repertory dialler/ringer IC, fabricated in a low threshold voltage CMOS technology and is a member of the Philips Semiconductors family of telecom ICs. Dial parameters of these ICs can be set by diode options to meet the specific requirements for various countries. The on-chip tone generators are used for DTMF dialling and ringer melody generation. A discriminator input enables the tone output only if a correct ringer frequency is applied. The memory contents of a repertory dial location can be up to 32 digits with a maximum of 250 digits.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3332-2P	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3332-2T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3332-3P	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3332-3T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3332-SP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3332-ST	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

PINNING

PCD3332-2

SYMBOL	PIN	DESCRIPTION	I/O TYPE
ROW2	1	row 2 keyboard output	1S(1)
ROW3	2	row 3 keyboard output	1S(1)
ROW4	3	row 4 keyboard output	1S(1)
ROW5	4	row 5 keyboard output	2S(2)
DIODE	5	diode option	1S(1)
MUTE	6	mute output	3R(4)
EARTH	7	earth recall	3R(4)
CSI	8	cradle switch input	–
XTAL1	9	oscillator input	–
XTAL2	10	oscillator output	–
RESET	11	reset input	–
CE/FDI	12	chip enable/frequency discriminator	–
COL6	13	column 6 input	1S(1)
COL5	14	column 5 input	1S(1)
COL4	15	column 4 input	1S(1)
COL3	16	column 3 input	1S(1)
COL2	17	column 2 input	1S(1)
COL1	18	column 1 input	1S(1)
$\overline{DP}/\overline{FL}$	19	dial pulse/flash output	2S(1)
n.c.	20	not connected	3R(4)
VOL2	21	volume 2 output	2R(3)
V_{SS}	22	ground	–
TONE	23	tone generator output	–
V_{DD}	24	positive supply voltage	–
VOL1	25	volume 1 output	2R(3)
DMO/KTE	26	dial mode output	3R(4)
RTE	27	key/ringer tone enable	3R(4)
ROW1	28	row 1 keyboard output	1S(1)

Notes

1. 1S = standard input or output (where S = set to HIGH state).
2. 2S = open-drain output (where S = set to HIGH state).
3. 2R = open-drain output (where R = reset to LOW state).
4. 3R = push-pull output (where R = reset to LOW state).

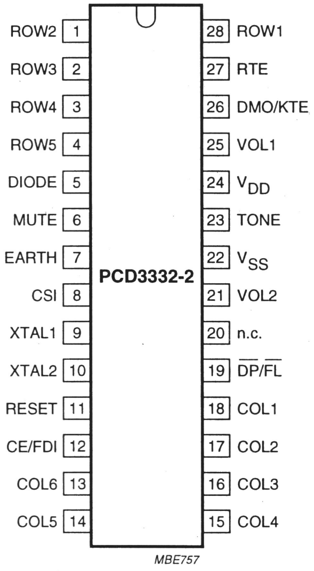

ROW2 1
ROW3 2
ROW4 3
ROW5 4
DIODE 5
MUTE 6
EARTH 7
CSI 8
XTAL1 9
XTAL2 10
RESET 11
CE/FDI 12
COL6 13
COL5 14
28 ROW1
27 RTE
26 DMO/KTE
25 VOL1
24 V_{DD}
23 TONE
22 V_{SS}
21 VOL2
20 n.c.
19 $\overline{DP}/\overline{FL}$
18 COL1
17 COL2
16 COL3
15 COL4
PCD3332-2
MBE757

Fig.1 Pin configuration.

PCD3332-3

SYMBOL	PIN	DESCRIPTION	I/O TYPE
ROW2	1	row 2 keyboard output	1S(1)
ROW3	2	row 3 keyboard output	1S(1)
ROW4	3	row 4 keyboard output	1S(1)
ROW5	4	row 5 keyboard output	2S(2)
DIODE	5	diode option	1S(1)
MUTE	6	mute output	3R(4)
EARTH	7	earth recall	3R(4)
CSI	8	cradle switch input	–
XTAL1	9	oscillator input	–
XTAL2	10	oscillator output	–
RESET	11	reset input	–
CE/FDI	12	chip enable/frequency discriminator	–
COL6	13	column 6 input	1S(1)
COL5	14	column 5 input	1S(1)
COL4	15	column 4 input	1S(1)
COL3	16	column 3 input	1S(1)
COL2	17	column 2 input	1S(1)
COL1	18	column 1 input	1S(1)
$\overline{DP}/\overline{FL}$	19	dial pulse/flash output	2S(1)
LFE	20	low-frequency amplifier enable	3R(4)
VOL2	21	volume 2 output	2R(3)
V_{SS}	22	ground	–
TONE	23	tone generator output	–
V_{DD}	24	positive supply voltage	–
VOL1	25	volume 1 output	2R(3)
DMO/KTE	26	dial mode output	3R(4)
HF/RTE	27	hands-free/ringer tone enable	3R(4)
ROW1	28	row 1 keyboard output	1S(1)

Notes

1. 1S = standard input or output (where S = set to HIGH state).
2. 2S = open-drain output (where S = set to HIGH state).
3. 2R = open-drain output (where R = reset to LOW state).
4. 3R = push-pull output (where R = reset to LOW state).

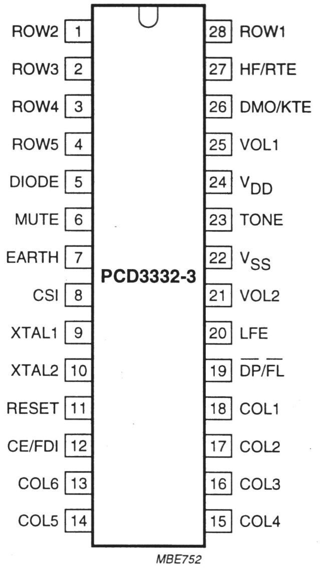

ROW2 1
ROW3 2
ROW4 3
ROW5 4
DIODE 5
MUTE 6
EARTH 7
CSI 8
XTAL1 9
XTAL2 10
RESET 11
CE/FDI 12
COL6 13
COL5 14
PCD3332-3
28 ROW1
27 HF/RTE
26 DMO/KTE
25 VOL1
24 V_DD
23 TONE
22 V_SS
21 VOL2
20 LFE
19 DP/FL
18 COL1
17 COL2
16 COL3
15 COL4
MBE752

Fig.2 Pin configuration.

PCD3332-S

SYMBOL	PIN	DESCRIPTION	I/O TYPE
ROW2	1	row 2 keyboard output	1S(1)
ROW3	2	row 3 keyboard output	1S(1)
ROW4	3	row 4 keyboard output	1S(1)
ROW5	4	row 5 keyboard output	2S(2)
DIODE	5	diode option	1S(1)
MUTE	6	mute output	3R(4)
EARTH	7	earth recall	3R(4)
CSI	8	cradle switch input	–
XTAL1	9	oscillator input	–
XTAL2	10	oscillator output	–
RESET	11	reset input	–
CE/FDI	12	chip enable/frequency discriminator	–
COL6	13	column 6 input	1S(1)
COL5	14	column 5 input	1S(1)
COL4	15	column 4 input	1S(1)
COL3	16	column 3 input	1S(1)
COL2	17	column 2 input	1S(1)
COL1	18	column 1 input	1S(1)
$\overline{\text{DP}}/\overline{\text{FL}}$	19	dial pulse/flash output	1S(1)
n.c.	20	not connected	3R(4)
VOL2	21	volume 2 output	2R(3)
V_{SS}	22	ground	–
TONE	23	tone generator output	–
V_{DD}	24	positive supply voltage	–
VOL1	25	volume 1 output	2R(3)
DMO/KTE	26	dial mode output	3R(4)
RTE	27	key/ringer tone enable	3R(4)
ROW1	28	row 1 keyboard output	1S(1)

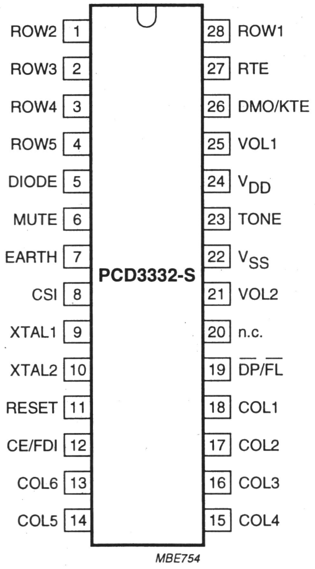

ROW2 1
ROW3 2
ROW4 3
ROW5 4
DIODE 5
MUTE 6
EARTH 7
CSI 8
XTAL1 9
XTAL2 10
RESET 11
CE/FDI 12
COL6 13
COL5 14
28 ROW1
27 RTE
26 DMO/KTE
25 VOL1
24 V_{DD}
23 TONE
22 V_{SS}
21 VOL2
20 n.c.
19 $\overline{\text{DP}}/\overline{\text{FL}}$
18 COL1
17 COL2
16 COL3
15 COL4
PCD3332-S
MBE754

Fig.3 Pin configuration.

Notes

1. 1S = standard input or output (where S = set to HIGH state).
2. 2S = open-drain output (where S = set to HIGH state).
3. 2R = open-drain output (where R = reset to LOW state).
4. 3R = push-pull output (where R = reset to LOW state).

FUNCTIONAL DESCRIPTION

Pin description

SUPPLY TERMINALS (V_{DD} AND V_{SS})

The power supply must be maintained for data storage. The RAM retention voltage (standby supply voltage) is 1 V, which is enough to retain the contents of the RAM. To ensure that the contents of the RAM is secure in the event of a power failure, a capacitor may be connected across the supply terminals. The capacitor must have a suitable value to maintain the RAM retention voltage for a certain period of time. The minimum operating voltage of these devices is 2.5 V. The internal power-on reset is enabled for a voltage below this minimum operating voltage.

OSCILLATOR INPUT/OUTPUT (XTAL1 AND XTAL2)

The time base for the PCD3332 is a crystal-controlled on-chip oscillator, which incorporates a 3.58 MHz crystal or ceramic resonator connected between XTAL1 and XTAL2. It should be noted that when using a ceramic resonator, the minimum supply voltage increases. The oscillator starts when V_{DD} reaches its operating voltage level and CE = HIGH [2.5 V (min.)].

CHIP ENABLE AND FREQUENCY DISCRIMINATOR INPUT (CE/FDI)

This active HIGH input is used to:

1. Activate and initialize the PCD3332.
2. Detect line power breaks.
3. Enter the ringer mode.
4. Enter the off-hook mode.

To keep the PCD3332 in the off-hook mode, CE must remain HIGH. The CE pin is also used for ringer frequency detection. If the ringer AC voltage is applied to this pin the frequency is measured and, if accepted, the output TONE will generate a 3-tone ringer burst.

To generate a correct ringer tone, the frequency must be between:

1. 19.5 and 57 Hz; frequencies below 18 Hz and higher than 64 Hz are omitted.
2. 14.5 and 68 Hz; frequencies below 14 Hz and higher than 76 Hz are omitted.

Ringer response timing and detection is illustrated in Fig.15.

CRADLE SWITCH INPUT (CSI)

Table 1 Different modes of the PCD3332

INPUT CSI	INPUT CE/FDI	PCD3332 STATUS
LOW	LOW	stop or power-down mode
HIGH	LOW	idle mode
LOW	HIGH	ringer mode
HIGH	HIGH	conversation or off-hook mode

RESET INPUT (RESET)

Pin RESET is an input to the internal reset circuit. When the reset input is activated (HIGH), an internal PCD3332 hardware reset is generated. All inputs/outputs are set to their default state, also referred to as a cold start or power-on-reset, which is also generated If V_{DD} drops below 2.5 V. The power-on reset is generated by the on-chip power-on-reset circuit, thereby ensuring a proper initiation after a power failure. Activating the PCD3332 by activating CE/FDI is often referred to as a warm start which is the normal situation, since the power back-up capacitor connected across the supply terminals must be valued such that the V_{DD} will remain above 2.5 V. The reset pin can be connected to V_{SS}, preferable via a 100 kΩ to 1 MΩ resistor, which will save leakage current. A capacitor connected to V_{DD} can be used to extend the reset time, should a longer reset time be desirable.

PULSE DIAL AND FLASH OUTPUT ($\overline{DP}/\overline{FL}$)

A calibrated pulse (recall register) is output when the Flash key is depressed.

The calibrated time for which the output $\overline{DP}/\overline{FL}$ is active depends on the diode option selected. During the conversation mode, output $\overline{DP}/\overline{FL}$ is HIGH. The timing sequence for pulse dialling is illustrated in Figs 5 and 7. Output $\overline{DP}/\overline{FL}$ starts with a sequence of pulses corresponding with the digit for transmission followed by an interdigit pause. After CE is set LOW, $\overline{DP}/\overline{FL}$ stays LOW. Thus $\overline{DP}/\overline{FL}$ is HIGH during a line-make and LOW during a line-break.

MUTE OUTPUT (MUTE)

During the dialling sequence this push-pull output is activated. In the pulse dialling mode, MUTE goes HIGH prior to the dialling action and goes LOW after the last t_{idp} (interdigit pause), the timing relationship is illustrated in Figs.11 to 14. In DTMF dialling, MUTE goes HIGH prior to the dialling action and goes LOW after an additional $t_{hold\ over}$ (hold over time, see Figs.13 and 14).

This output is also activated if the set enters the programming mode, to avoid transmitting the keys entered.

DTMF OUTPUT (TONE)

The timing sequence for DTMF dialling is illustrated in Figs.13 and 14. The tones generated by this TONE are filtered by an on-chip switched capacitor filter, and active RC low-pass filter. Therefore, the total harmonic distortion fulfils the CEPT CS203 recommendations. An on-chip reference voltage provides output tone levels independent of supply voltages and temperatures. Spread among the individual parts is extremely low.

The DC level of the TONE output measures $\frac{1}{2}V_{DD}$ and the impedance is 100 Ω (typ.). Table 2 shows the frequency tolerances.

The TONE output is also used to generate the ringer melody, key entry acception beep, error or warning beeps and confirmation beeps. These beeps are generated in programming mode as a response to the users action. The ringer is designed to generate 3-melodies that may be selected using the keyboard. Table 3 shows the implemented ringer melodies.

Table 2 DTMF frequency tolerances

ROW/COL	STANDARD FREQUENCY (Hz)	OUTPUT FREQUENCY (Hz)	DEVIATION (%)	DEVIATION (Hz)
Row 1	697	697.90	+0.13	+0.90
Row 2	770	770.46	+0.06	+0.46
Row 3	852	852.45	−0.18	−1.55
Row 4	941	943.23	+0.24	+2.23
Col 1	1209	1206.45	−0.21	−2.55
Col 2	1336	1341.66	+0.42	+5.66
Col 3	1477	1482.21	+0.35	+5.21

Table 3 Ringer melodies

KEY DEPRESSED	TONE 1 (Hz)	TONE 2 (Hz)	TONE 3 (Hz)	TONE ON TIME (ms)	TONE OFF TIME (ms)
1	826	925	1037	30	30
2	1037	1161	1297	30	30
3	1297	1455	1621	30	30

Table 4 Beep frequencies

BEEP FUNCTION	TONE 1 (Hz)	TONE 2 (Hz)	TONE 3 (Hz)	TONE ON TIME (ms)	TONE OFF TIME (ms)
Key accept	2358	–	–	40	–
Error	2358	2358	2358	134	35
Confirmation	806	899	1010	134	67

REGISTER RECALL (EARTH)

If the diode option of the PCD3332 is set to the Earth, then dialling the EARTH either out of Repertory/LNR or by pressing the FLASH key will activate the push-pull output EARTH for a calibrated time. Figures 12 and 14 illustrate the EARTH timing relationship with other signals.
The calibrated EARTH time is followed by an interdigit time t_{idp}. A second dialling of EARTH can only be performed after the interdigit time has elapsed.

If the Flash key was the first key depressed directly after going off-hook, followed by a second depressing of the Flash key while the EARTH is still in progress, then the second depression will be ignored.

RINGER TONE ENABLE (RTE: PCD3332-2/S)

The PCD3332-2 generates tones for the ringer output stage and key tones when depressing a function key at the keypad. Output RTE will go HIGH and stay HIGH for the duration of the tone generated at output TONE.

HANDS-FREE/RINGER TONE ENABLE (HF/RTE: PCD3332-3)

The PCD3332-3 generates tones for the ringer output stage and key tones when depressing a function key at the keypad. Output RTE will go HIGH and stay HIGH for the duration of the tone generated at output TONE.

During the conversation mode, the hands-free output (HF) is used for enabling the hands-free mode. Depressing the HOOK key will change the operation mode as follows:

- Change from on-hook (stop mode) to hands-free mode
- Toggles the listening-in mode
- Change from handset to hands-free.

VOLUME CONTROL OUTPUTS (VOL1 AND VOL2)

PCD3332-2

The PCD3332-2 has the facility to control the ringer output signal, as well as the loudspeaker volume, by depressing the keys ∗/VOL− or #/ VOL+ during the ringer mode.

If the maximum volume level is reached, depressing #/VOL+ key will not change the volume setting. If the minimum volume level is reached, depressing ∗/VOL− key will not change the volume setting. Selection between ringer volume or conversation mode volume, is performed in the hardware using the RTE output. In the ringer mode the output RTE is HIGH.

Table 5 shows the volume outputs setting, as well as the default setting in case of a power failure or if the power is supplied for the first time.

PCD3332-3

The PCD3332-3 has the facility to control the ringer output signal and the loudspeaker signal during listening-in or hands-free operation. Depressing the keys VOL− or VOL+ during the ringer mode will change the ringer volume setting. Depressing the keys VOL− or VOL+ during the conversation mode will change the loudspeaker volume setting.

If the maximum volume level is reached, depressing the VOL+ key will not change the volume setting. If the minimum volume level is reached, depressing the VOL− key will not change the volume setting. Selection between ringer volume or conversation mode volume, is performed in the hardware using the HF/RTE output. In the ringer mode the output HF/RTE is HIGH.

Table 5 shows the volume outputs setting, as well as the default setting in case of a power failure or if the power is supplied for the first time.

PCD3332-S

The PCD3332-S has the facility to control the ringer output signal by depressing the keys VOL− or VOL+ during the ringer mode.

If the maximum volume level is reached, depressing the VOL+ key will not change the volume setting. If the minimum volume level is reached, depressing the VOL− key will not change the volume setting. Selection between ringer volume or conversation mode volume, is performed in the hardware using the RTE output. In the ringer mode the output RTE is HIGH.

Table 5 shows the volume outputs setting, as well as the default setting in case of a power failure or if the power is supplied for the first time.

RINGER VOLUME SETTINGS

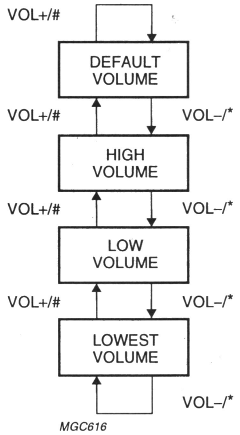


Fig.4 FSM for volume control (PCD3332-2).

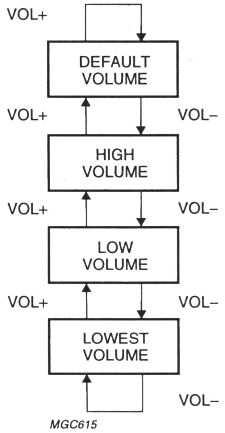


Fig.5 FSM for volume control (PCD3332-3/S).

Table 5 State assignment

STATE	VOL2	VOL1
Default volume setting	HIGH	HIGH
High volume setting	HIGH	LOW
Low volume setting	LOW	HIGH
Lowest volume setting	LOW	LOW

DIAL MODE OUTPUT /KEY-TONE ENABLE (DMO/KTE)

In the PULSE dialling mode the DMO/KTE output is activated (HIGH), at dialling the Make/Brake pulse dial sequences. Figures 11 and 12 illustrate the signal timing relationship.

In the programming mode, the DMO/KTE output is activated at the same time the key beeps are generated at output TONE and may be used to enable the key tone to the earpiece amplifier.

KEYBOARD INPUTS/OUTPUTS

A single contact keyboard with a maximum of 6 columns and 5 rows can be connected to the PCD3332-2.
The keyboard scanning is started if a key depression is detected. The rows are scanned while the columns are used as sense inputs.

To overcome key bouncing, a debounce on/off time of approximately 14 to 20 ms is implemented.

Only one single key depression is validated and accepted at any one time. Once a key is accepted the keyboard scanning is continued until no further keys are depressed. This means that if a key is accepted but still depressed while a second key is entered, the second key depression is ignored. Also, if two or more keys are depressed within the debounce time while no key is yet accepted, all keys are ignored.

Keyboard detection is also performed in the ringer mode to enable the ringer volume setting and ringer melody selection.

In the on-hook mode or power-down mode of the PCD3332-2 and PCD3332-S, the keyboard I/Os are set to HIGH except ROW 5 which is set to LOW.

In the on-hook mode or power-down mode of the PCD3332-3, the keyboard I/Os are set to HIGH except ROW 5 which is set to LOW. In this instance, depression of the HOOK button can be detected by the external hardware circuitry and converted to an active HIGH signal which is passed to $\overline{CE}$ in order to 'wake-up' the PCD3332-3.

When the HOOK key has been accepted the PCD3332-3 enters the hands-free mode.

ROW 5 was used to detect the HOOK key, this function is deleted.

ROW 5 is an open-drain input, this configuration is used to avoid current flowing in the on-hook mode or power-down mode. A pull-up resistor should be connected to ROW 5.

Keyboards

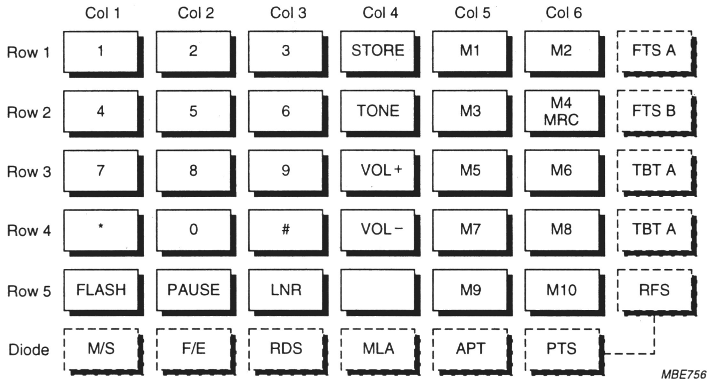

Col 1
Col 2
Col 3
Col 4
Col 5
Col 6
Row 1
1
2
3
STORE
M1
M2
FTS A
Row 2
4
5
6
TONE
M3
M4
MRC
FTS B
Row 3
7
8
9
VOL +
M5
M6
TBT A
Row 4
*
0
#
VOL −
M7
M8
TBT A
Row 5
FLASH
PAUSE
LNR
M9
M10
RFS
Diode
M/S
F/E
RDS
MLA
APT
PTS
MBE756

Fig.6 Keyboard layout (PCD3332-2).

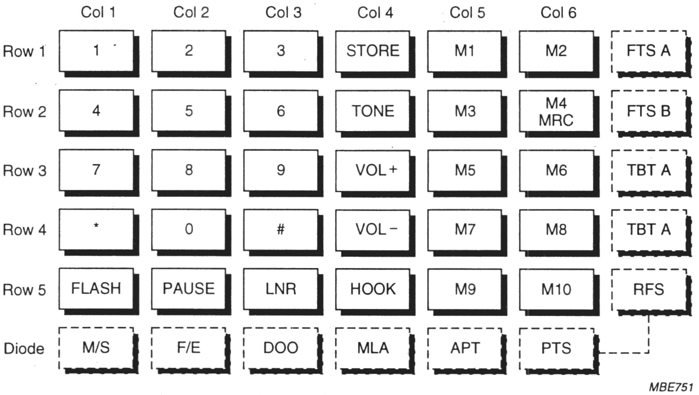

Col 1
Col 2
Col 3
Col 4
Col 5
Col 6
Row 1
1
2
3
STORE
M1
M2
FTS A
Row 2
4
5
6
TONE
M3
M4 MRC
FTS B
Row 3
7
8
9
VOL+
M5
M6
TBT A
Row 4
*
0
#
VOL−
M7
M8
TBT A
Row 5
FLASH
PAUSE
LNR
HOOK
M9
M10
RFS
Diode
M/S
F/E
DOO
MLA
APT
PTS
MBE751

Fig.7 Keyboard layout (PCD3332-3).

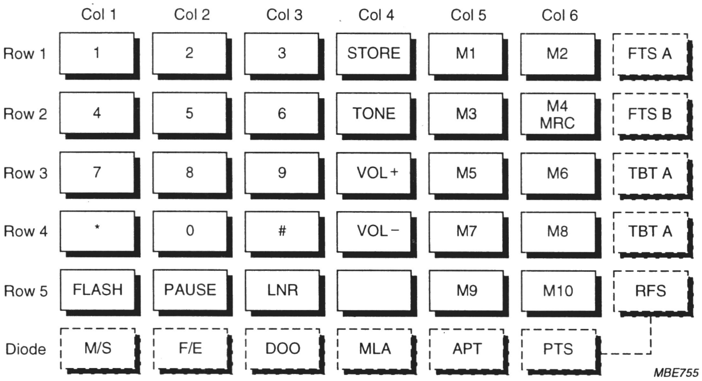

Col 1
Col 2
Col 3
Col 4
Col 5
Col 6
Row 1
1
2
3
STORE
M1
M2
FTS A
Row 2
4
5
6
TONE
M3
M4 MRC
FTS B
Row 3
7
8
9
VOL+
M5
M6
TBT A
Row 4
*
0
#
VOL−
M7
M8
TBT A
Row 5
FLASH
PAUSE
LNR
M9
M10
RFS
Diode
M/S
F/E
DOO
MLA
APT
PTS
MBE755

Fig.8 Keyboard layout (PCD3332-S).

KEYBOARD FUNCTION KEYS

LNR

If the first key operated after CE = HIGH (off-hook) is button LNR the PCD3332 will transmit the last number dialled before CE was LOW (on-hook).

PAUSE

Pressing the PAUSE key will insert an access pause during manual dialling and/or during programming. During manual dialling the pause time is not dialled, but is stored in the redial memory. This means that with manual dialling the user actually waits for the dial tone before dialling is continued. Repertory and LNR dialling however, will dial out the access pause. If the pause key is depressed while an access pause is being dialled, the access pause in progress is terminated and dialling will continue at the next non-access pause digit. The access pause duration is option selectable.

TONE (mixed mode dialling)

If the pulse dial mode is selected by the diode option, then pressing the 'TONE', '∗' or '#' keys will change the dial mode to DTMF. Pressing the Flash key or going on-hook will restore the pulse dial mode.

RECALL (Flash or Earth)

Depressing the FLASH key will activate output $\overline{DP}/\overline{FL}$ or output EARTH for the calibrated time, depending on which function Flash or Earth is selected.

STORE

Pressing the STORE key will start/stop the programming mode. To inhibit transmitting the key entries while in programming mode, the output and MUTE is activated.

MRC

In order to access one of the memory locations, the MRC button must be depressed followed by one of the numerical keys 0 to 9. To enable the MRC button, diode option MLA must be on.

VOL− and VOL+

In these modes (hands-free and listening-in), where the loudspeaker is on, the VOL buttons control the loudspeaker volume (PCD3332-3 only). In the ringer mode, the VOL buttons control the ringer volume.

At power-on reset a default volume is preset for both the loudspeaker and the ringer volume.

DIODE OPTIONS

Table 6 Tone Burst Time diode configuration

TBT A DIODE	TBT B DIODE	SELECTED TIMING (ms)
Not connected	not connected	70/70
Not connected	connected	100/100
Connected	not connected	85/85
Connected	connected	70/140

Table 7 Flash time select diode configuration

FTS A DIODE	FTS B DIODE	SELECTED TIMING (ms)
Not connected	not connected	95
Not connected	connected	270
Connected	not connected	115
Connected	connected	600

Table 8 Flash/Earth diode configuration (PCD3332-2/S)

F/E DIODE	SELECTED MODE
Not connected	Flash
Connected	Earth (400 ms)

Table 9 Flash/Earth diode configuration (PCD3332-3)

F/E DIODE	SELECTED MODE
Not connected	Flash
Connected	Earth

Table 10 Mark/space diode configuration

M/S DIODE	SELECTED MAKE/BRAKE RATIO (ms)
Not connected	33/66 (1 : 2)
Connected	40/60 (2 : 3)

Table 11 Pulse/tone diode configuration

P/T DIODE	SELECTED DIAL MODE
Not connected	DTMF
Connected	Pulse

Table 12 Access Pause Time diode configuration

APT DIODE	SELECTED TIMING (s)
Not connected	2
Connected	4

Table 13 Ringer tones control

RFS DIODE	RINGER FREQUENCY SELECTION (Hz)
Not connected	19.5 to 54
Connected	14.5 to 68

Table 14 Memory Location Access diode configuration

MLA DIODE	KEY FUNCTION
Not connected	M4/MRC button is MRC
Connected	M4/MRC button is M4

Table 15 DTMF output option diode configuration (PCD3332-2)

RDS DIODE	OUTPUT SELECTION
Not connected	no delay
Connected	ringer validation delay, 100 ms

Table 16 DTMF output option diode configuration (PCD3332-3/S)

DOO DIODE	OUTPUT SELECTION
Not connected	no transmission of ∗/#
Connected	transmission of ∗/#

Ringer Delay Selection (RDS: PCD3332-2)

If the diode is connected, then the actual ringer frequency validation is started after a delay of 100 ms. This is only performed at the start of each ringer burst signal.

DOO DTMF output selection (PCD3332-3/S)

If the diode is connected, then the ∗ and # DTMF signals will be dialled out during pulse-to-tone switching. If the diode is not connected ∗ and # will not be dialled out during pulse-to-tone switching.

Ringer Tones Control (RTC: PCD3332-2/S)

The ringer melody can be changed by depressing buttons 1, 2 and 3. To disable this, apply a diode at RFS location.

Ringer Frequency Selection (RFS)

This diode is used to select between two frequency ranges, 19.5 to 54 Hz or 14.5 to 68 Hz.

Memory Location Access (MLA)

To be able to build various telephone models by using the PCD3332, a possibility has been created to define different keypad layouts. e.g. a 13 number repertory dial consist of 10 numbers recalled via MRC + 0 to 9, and 3 direct access numbers M1, M2 and M3. A 10 number direct accessible dialler can be created by applying the buttons M1 to M10 while a diode is connected at the MLA location.

Mark-to-Space ratio (M/S)

Changes the make-break ratio from 60:40 ms (3:2) to 66:33 ms (2:1).

Access Pause Time (APT)

To adapt the access pause timing to local requirements, 2 different times for DTMF and the corresponding times for pulse dialling are built-in.

Tone Burst Time (TBT)

During automatic transmission of a number in the DTMF mode the tone-on time and the pause time between two digits can be selected by option TBT A and TBT B. During manual dialling this option selects the minimum tone-on and pause time while the maximum time is determined by the time a button is depressed.

Pulse/Tone mode Selection (PTS)

The telephone set can be initially set to the PULSE or DTMF mode by switching on and off the diode in the matrix.

The first entry of buttons ∗ and # in the pulse dial mode will change the dial mode as well.

Flash or Earth register recall (F/E)

Dependent on this option, the output $\overline{DP}/\overline{FL}$ or output EARTH will be activated after a flash button operation.

Flash Time Select (FTS: PCD3332-2/S)

Pressing the flash button (when FLASH mode is selected) will generate a time calibrated pulse at output $\overline{DP}/\overline{FL}$ for 100, 115, 270 or 600 ms.

Flash Time Select (FTS: PCD3332-3)

Pressing the flash button will generate a time calibrated pulse at output $\overline{DP}/\overline{FL}$ or EARTH depending on the F/E setting.

Low Frequency amplifier Enable (LFE: PCD3332-3)

Output LFE can be used to enable the TEA108X or TEA109X listening-in or hands-free IC. The HOOK key functions as a toggle to control the hands-free mode (LFE = LOW) or listening-in mode (LFE = HIGH). while in the off-hook condition the button can be pressed and kept down to replace the handset while saving the LFE and DPN/FLN selection.

HOOK MODES

Figure 9 illustrates the different HOOK modes and how those modes are entered (PCD3332-3).

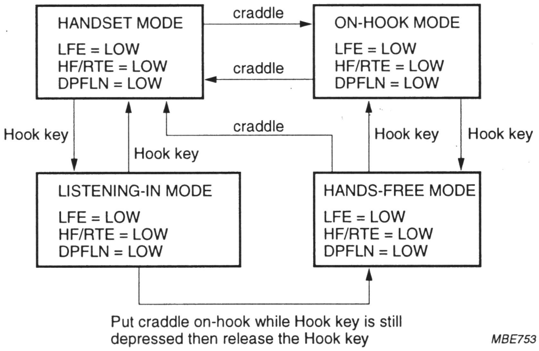

HANDSET MODE
LFE = LOW
HF/RTE = LOW
DPFLN = LOW
craddle
craddle
ON-HOOK MODE
LFE = LOW
HF/RTE = LOW
DPFLN = LOW
Hook key
Hook key
craddle
Hook key
Hook key
LISTENING-IN MODE
LFE = LOW
HF/RTE = LOW
DPFLN = LOW
HANDS-FREE MODE
LFE = LOW
HF/RTE = LOW
DPFLN = LOW
Put craddle on-hook while Hook key is still depressed then release the Hook key
MBE753

Fig.9 Schematic diagram of the HOOK modes.

OPERATING PROCEDURES

Operating modes

The PCD3332-2/S has 4 operating modes:

1. On-hook mode or ringer mode.
2. Off-hook mode or conversation mode.
3. Programming mode or store mode.
4. Dial mode.

The PCD3332-3 has 4 operating modes:

1. On-hook mode or ringer mode.
2. Conversation mode which is divided into hands-free mode and listening-in mode.
3. Programming mode or store mode.
4. Dial mode.

ON-HOOK MODE OR RINGER MODE

When the chip enable input CE/FDI is LOW the PCD3332 is disabled. In the standby mode, the only current drawn is for memory retention of the redial digits. During the standby mode all keyboard pins are HIGH.

DIAL MODE

Lifting the cradle (handset) or pressing the hook key will put the set in the conversation mode, an accepted key entry is processed and may initiate the following:

- Dialling the digits entered
- Redialling the previously entered digits
- Dialling out a repertory memory
- Enter programming mode.

RESET DELAY TIME

All modes, except for the ringer mode, are terminated by a line break (CE is deactivated), or by going on-hook. If this condition is detected, the reset delay time is initiated. The set will not enter the on-hook state unless the reset delay has expired. In the event of a line break, the set will remain in the actual operation mode if the line-brake is ended while the reset delay is still in progress (see Fig.10).

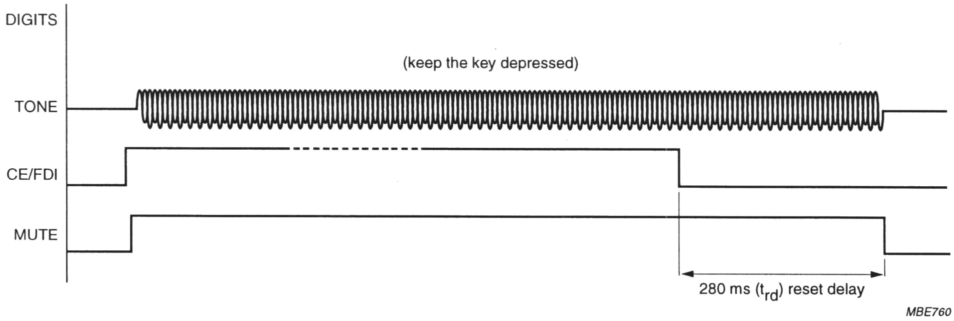
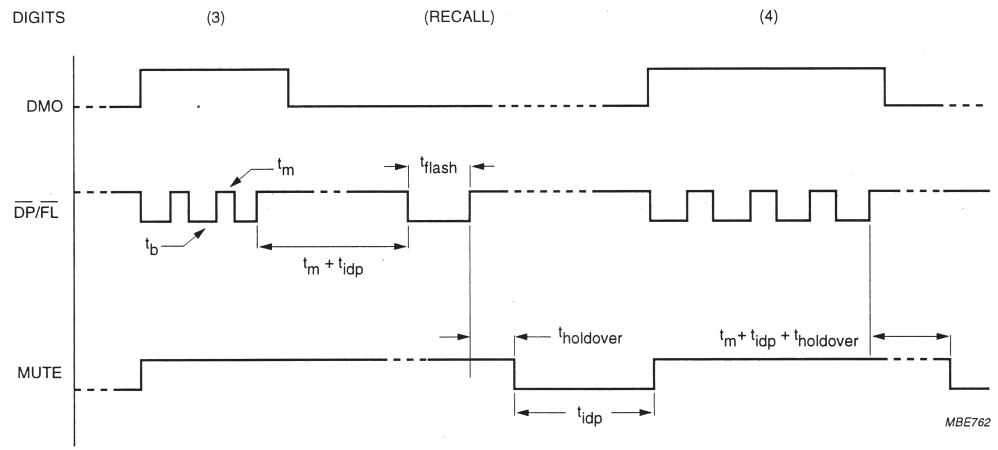


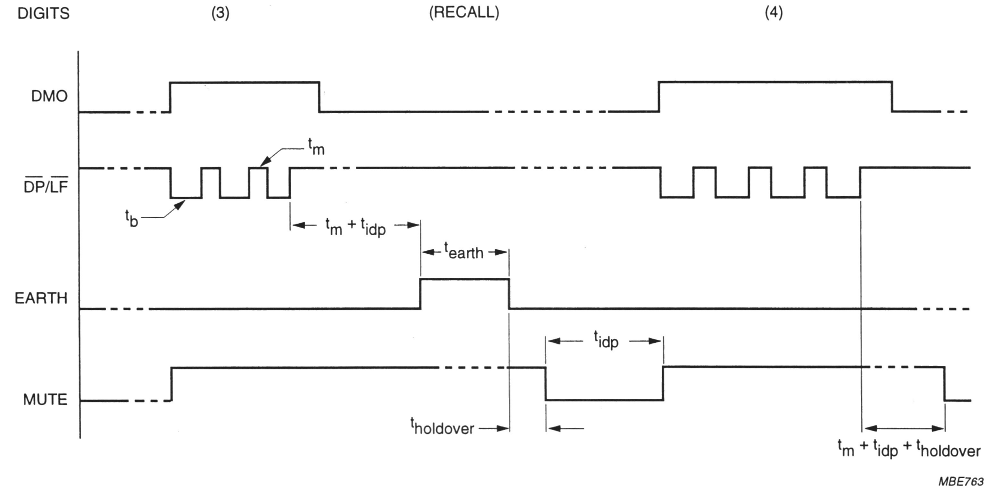
Fig.10 Reset delay timing relationship.

Pulse dialling (PTS = ON)


DIGITS
(3)
(RECALL)
(4)
DMO
DP/FL
MUTE
t_m
t_flash
t_b
t_m + t_idp
t_holdover
t_m+ t_idp + t_holdover
t_idp
MBE762

$t_{holdover}$ = 80 ms; t = 840 ms.
t_b = break time; t_m = make time; t_{idp} = interdigit pause time.

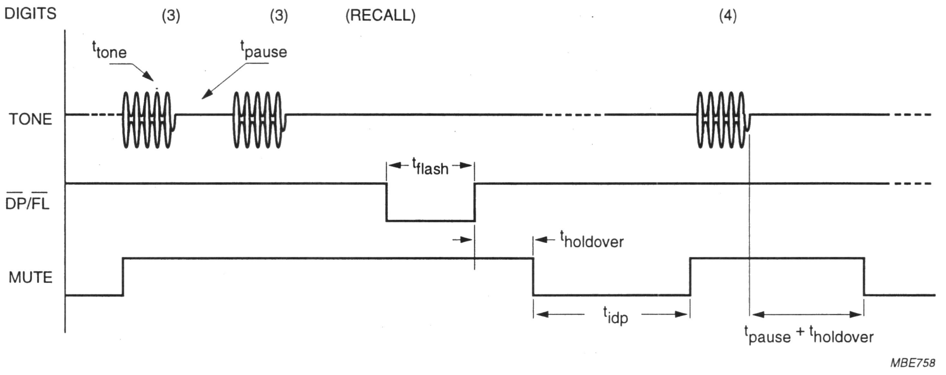
Fig.11 $\overline{\text{DP}}/\overline{\text{FL}}$, DMO and MUTE timing relationship.


DIGITS
(3)
(RECALL)
(4)
DMO
DP/LF
EARTH
MUTE
t_m
t_b
t_m + t_idp
t_earth
t_idp
t_holdover
t_m + t_idp + t_holdover
MBE763

$t_{holdover}$ = 80 ms; t_{idp} = 840 ms.
t_b = break time; t_m = make time; t_{idp} = interdigit pause time.

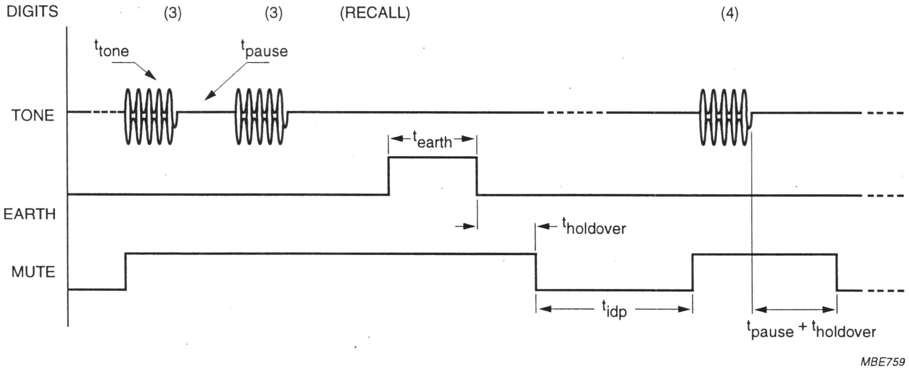
Fig.12 $\overline{\text{DP}}/\overline{\text{FL}}$, DMO, MUTE and EARTH timing relationship.

DTMF dialling (PTS = OFF)


DIGITS
(3)
(3)
(RECALL)
(4)
t_{tone}
t_{pause}
TONE
$\overline{DP}/\overline{FL}$
t_{flash}
MUTE
$t_{holdover}$
t_{idp}
$t_{pause} + t_{holdover}$
MBE758

$t_{holdover}$ = 80 ms; $_{idp}$ = 840 ms.
t_{idp} = interdigit pause time.

Fig.13 $\overline{DP}/\overline{FL}$, MUTE and TONE timing relationship.


DIGITS
(3)
(3)
(RECALL)
(4)
t_{tone}
t_{pause}
TONE
t_{earth}
EARTH
$t_{holdover}$
MUTE
t_{idp}
$t_{pause} + t_{holdover}$
MBE759

$t_{holdover}$ = 80 ms; $t_{idp\ (flash-idp)}$ = 840 ms.
t_{idp} = interdigit pause time.

Fig.14 TONE, MUTE and EARTH timing relationship.

Manual dialling

During the digit entry, the circuit starts immediately with transmission of the digit(s). The minimum transmission time is unaffected by the speed of entry. Transmission continues as long as further data input has to be processed. Up to 32 digits can be stored in the redial register.

After the main register overflows, a 10 digits First-In First-Out register (FIFO) takes over as buffer. After transmitting the first digit of the FIFO register this position is automatically cleared to provide space for storing new data. In this way, the total number of digits which can be transmitted is unlimited, provided the key-in rate is not excessive.

If the key-in rate causes both the redial register and FIFO register to overflow, the PCD3332-2 will return to the conversation mode and no keyboard entries will be accepted. For the PCD3332-3/S no keyboard entries will be accepted before CE = LOW and HIGH again (on-hook/off-hook).

Last number redial

If the first key entered is the LNR key, the stored LNR number is dialled out-section. LNR can hold a maximum of 32 digits. LNR is inhibited If more than 32 digits are entered, normal dialling however is continued.

LNR functional examples:

⇓ = Go on-hook

⇑ = Go off-hook

Table 17 LNR capacity

INPUT	OUTPUT
⇑, [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], [1], [2], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2
⇑. [LNR], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2
⇑, [LNR], [0], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, 0
⇑, [LNR], ⇓	nothing dialled

Table 18 LNR after programming

INPUT	OUTPUT
⇑, [1], [2], [3], [4], [5], ⇓	DTMF: 1, 2, 3, 4, 5
⇑, [LNR], ⇓	DTMF: 1, 2, 3, 4, 5
⇓, ⇑, [STORE] [5], [4], [3], [2], [1], [STORE], [M1], ⇓	beep for each entry (confirmation beep)
⇑, [LNR], ⇓	nothing dialled

Table 19 LNR sliding cursor

INPUT (M1 = 1, 2, 3, 4 or 5)	OUTPUT
⇑, [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
⇑, [1], [2], [3], [LNR], ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
⇑, [STORE] [5], [4], [3], [2], [1], [STORE], [M1] ⇓	DTMF: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
⇑, [M1], Wait for end of dial, [M1], ⇓	DTMF: 1, 2, 3, 4, 5, 1, 2, 3, 4, 5
⇑[1], [2], [3], [LNR], ⇓	DTMF: 1, 2, 3, 4, 5, 1, 2, 3, 4, 5
⇑[2], [3], [LNR], ⇓	DTMF: 2, 3
⇑[2], [3], [LNR], ⇓	DTMF: 2, 3

Table 20 LNR if ∗, #, Tone, and recall is entered in DTMF mode

INPUT	OUTPUT
⇑ [1], [2], [∗], [3], [4], [Recall], [6], [7], ⇓	DTMF: 1, 2, ∗, 3, 4, Flash, 6, 7
⇑, [LNR], ⇓	DTMF: Flash, 6, 7
⇑ [Recall], Wait 0.5 sec, [Recall], Wait 0.5 sec, [Recall], [1], [2], [3], ⇓	Flash, Flash, Flash, 1, 2, 3
⇑ [LNR], ⇓	Flash, 1, 2, 3
⇑ [1], [2], [3], [Recall], [3], [2], [1], ⇓	1, 2, 3, Flash, 3, 2, 1
⇑ [LNR], ⇓	Flash, 3, 2, 1
⇑ [1], [2], [3], [Recall], [∗], [3], [2], [1], ⇓	1, 2, 3, Flash, ∗, 3, 2, 1
⇑ [LNR], ⇓	∗, 3, 2, 1
⇑ [∗], [1], [2], [3], [Recall], [3], [2], [1], ⇓	∗, 1, 2, 3, Flash, 3, 2, 1
⇑ [LNR], ⇓	Flash, 3, 2, 1
⇑ [∗], [1], [2], [3], [Recall], [∗], [3], [2], [1], ⇓	∗, 1, 2, 3, Flash, 3, 2, 1
⇑ [LNR], ⇓	Flash, 3, 2, 1

Table 21 LNR if ∗, #, Tone, and recall is entered in PULSE mode

INPUT	OUTPUT
⇑ [1], [2], [∗], [3], [4], [Recall], [6], [7], ⇓	PULSE: 1, 2, DTMF: 3, 4, Earth, PULSE: 6, 7
⇑ [LNR], ⇓	PULSE: 1, 2,
⇑ [Recall], Wait 0.5 sec, [Recall], Wait 0.5 sec, [Recall], [1], [2], [3], ⇓	PULSE: Earth, Earth, Earth, 1, 2, 3
⇑ [LNR], ⇓	PULSE: Earth, 1, 2, 3
⇑ [1], [2], [3], [Recall], [3], [2], [1], ⇓	PULSE: 1, 2, 3, Earth, 3, 2, 1
⇑ [LNR], ⇓	PULSE: Earth, 3, 2, 1
⇑ [1], [2], [3], [Recall], [∗], [3], [2], [1], ⇓	PULSE: 1, 2, 3, Earth, DTMF: 3, 2, 1
⇑ [LNR], ⇓	PULSE: 1, 2, 3
⇑ [∗], [1], [2], [3], [Recall], [3], [2], [1], ⇓	DTMF: 1, 2, 3, Earth, PULSE: 3, 2, 1
⇑ [LNR], ⇓	PULSE: Earth, 3, 2, 1
⇑ [∗], [1], [2], [3], [Recall], [∗], [3], [2], [1], ⇓	DTMF: 1, 2, 3, Earth, 3, 2, 1
⇑ [LNR], ⇓	DTMF: 1, 2, 3

Access pause dialling and termination

Access pauses entered during manual dialling are not dialled out, but are stored in LNR. At LNR dialling or dialling of a repertory, the access pauses are dialled out. If at LNR or repertory dial, an access pause is being dialled out, then depressing the AP key will terminate the access pause in progress and dialling will continue at the first non-access pause digit.

Flash/Earth recall

Depending on the option selected (see Table 7), depressing the Flash key will generate a calibrated Flash time at output DPFLN (see Table 6), or a calibrated earth time of 400 ms on the EARTH output 8.

The Flash/Earth will also refer the set to dial mode selected by the diode option.

Data dialling in the pulse dialling mode (PCD3332-3/S)

If the PCD3332-3/S is initially set to the pulse dial mode (PTS = ON), depressing the TONE, ∗ or # button will continue dialling in the DTMF mode. Flash/Earth recall will restore the pulse dialling mode.

PROGRAMMING MODE

The PCD3332 has an on-chip CMOS RAM which can store up to 10 numbers of 32 digits with a total of 250 digits (floating memory). If the memory overflows, a warning beep is generated. If the controller is initially set to the pulse dial mode, digits can be stored in the pulse dial and/or in the DTMF mode by depressing button ∗ or # or using the 'change mode' procedure during the store procedure. This function is best illustrated in Table 22

Memory overflow

A total of 250 digits can be stored. After a repertory number tries to be stored, which will bring the total amount of digits over the 250, the TONE output will generate the memory overflow beeps and the store procedure is cancelled.

Notepad function

In the speech mode, a number can be entered on the keyboard. This number may be dialled out at the next off-hook situation or may be entered in memory. This function effectively mimics a notepad for a number passed during a telephone conversation.

Repertory and chain dialling

Repertory numbers can be dialled out before or after manual dialling, or last number redial or by entering the memory locations in successive order. However, during transmission of LNR or a repertory number, a next repertory is not accepted. This means that a repertory number can only be entered if the previous repertory dial or LNR is ended.

Depending on the MLA diode configuration (see Table 14) the procedure is as follows:

- Direct repertory access: M1 to M10
- Two-key repertory access: MRC 0 to MRC 9.

RINGER MODE (PCD3332-2)

The PCD3332-2 has a built-in frequency discriminator circuit, with CE/FDI being used as the discriminator input. If the ringer frequency supplied is accepted, a ringer melody is generated.

Depending on the diode option selected, 1 out of 3 ringer melodies may be selected. Also, when the ringer melody sounds, the ringer volume is adjustable in 4 steps using the ∗/VOL– #/VOL+ keys.

RINGER MODE (PCD3332-3/S)

The PCD3332-3/S has a built-in frequency discriminator circuit, with CE/FDI being used as the discriminator input. If the ringer frequency supplied is accepted, a ringer melody is generated.

Depending on the diode option selected, 1 out of 3 ringer melodies may be selected. Also, when the ringer melody sounds, the ringer volume is adjustable in 4 steps using the VOL– and VOL+ keys.

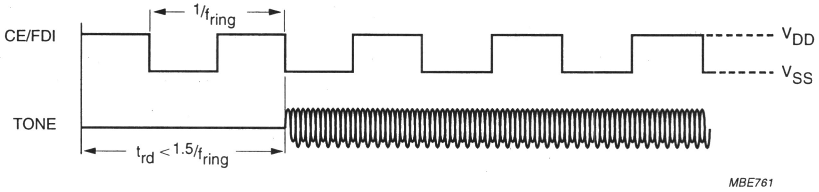

CE/FDI
TONE
1/f_ring
t_rd < 1.5/f_ring
V_DD
V_SS
MBE761

Fig.15 Ringer response timing and detection.

Table 22 Key sequence at programming mode

KEY SEQUENCE	REMARKS
Programming a repertory location	
[STORE] data [STORE] [M1](1)	
[STORE] data [M1](1)	
[STORE] data [STORE] [0](2)	
[STORE] data [STORE] [MRC] [0](2), and [STORE] data [STORE] [M1](3)	MLA diode connected
[STORE] data [MRC] [0](2), and [STORE] data [M1](3)	MLA diode connected
Copy LNR to a repertory location	
[STORE] [LNR] [STORE] [M1](1)	
[STORE] [LNR] [M1](1)	
[STORE] [LNR] [STORE] [0](2)	
[STORE] [LNR] [STORE] [MRC] [0](2), and [STORE] [LNR] [STORE] [M1](3)	MLA diode connected
[STORE] [LNR] [MRC] [0](2), and [STORE] [LNR] [M1](3)	MLA diode connected
Clearing a repertory location	
[STORE] [M1](1)	
[STORE] [STORE] [0](2)	
[STORE] [STORE] [MRC] [0](2), and [STORE] [STORE] [M1](3)	MLA diode connected
[STORE] [MRC] [0](2), and [STORE] [M1](3)	MLA diode connected
[STORE] data [MRC] [0](2), and [STORE] data [M1](3)	MLA diode connected
Notepad programming	
[STORE] data [STORE] [LNR]	
[STORE] data [LNR]	
Clear Notepad	
[STORE] [STORE] [LNR]	
[STORE] [LNR]	

Notes

1. Select [M1] to [M10].
2. Select [0] to [9].
3. Select [M1] to [M3].

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_I	input voltage	0.5	V_{DD} + 0.5	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3.57954 MHz; R_s = 50 Ω (max.); T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	operating supply voltage		2.5	–	6.0	V
$I_{DD(cm)}$	supply current conversation mode	CE = 1	–	100	–	µA
$I_{DD(dm)}$	supply current dialling mode	CE = 1	–	300	–	µA
$V_{DD(stb)}$	standby supply voltage	CE = 0	1.0	–	6.0	V
$I_{DD(stb)}$	standby supply current	CE = 0	–	1.0	2.5	µA
Reset I/O						
V_{sw}	reset voltage switching level	$V_{DD} < V_{sw}$	–	–	2.5	V
I_{sink}	reset sink current	$V_{DD} < V_{sw}$	–	7	–	µA
Inputs						
V_{IL}	LOW level input voltage (any pin)		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage (any pin)		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current (pin CE)	$V_i = V_{SS}$ to V_{DD}	–	–	–100	nA
		CE = 1	–	–	1	µA
Keyboard contact resistance						
R_{on}	keyboard ON		–	–	1	kΩ
R_{off}	keyboard OFF		100	–	–	kΩ
Outputs						
$I_{O(sink)}$	output sink current	V_{OH} = 0.4 V	–	1.5	–	mA
$I_{OH(s)}$	HIGH level output source current	V_{OH} = 2.6 V (push-pull)	–	–1.5	–	mA
$I_{OH(sl)}$	HIGH level output source leakage current	V_{OH} = 0 to V_{DD} (open-drain)	–	–	–1	µA

8-bit microcontroller with DTMF generator PCD3344A; PCD3349A

CONTENTS

1 FEATURES

2 GENERAL DESCRIPTION

3 ORDERING INFORMATION

4 BLOCK DIAGRAM

5 PINNING INFORMATION

5.1 Pinning
5.2 Pin description

6 FREQUENCY GENERATOR

6.1 Frequency generator derivative registers
6.2 Frequency registers
6.3 DTMF frequencies
6.4 Modem frequencies
6.5 Musical scale frequencies

7 TIMING

8 RESET

9 STOP MODE

10 IDLE MODE

11 INSTRUCTION SET

12 SUMMARY OF MASK OPTIONS

13 LIMITING VALUES

14 HANDLING

15 DC CHARACTERISTICS

16 AC CHARACTERISTICS

17 PACKAGE OUTLINES

18 SOLDERING

18.1 Introduction
18.2 DIP
18.3 SO

19 DEFINITIONS

20 LIFE SUPPORT APPLICATIONS

8-bit microcontroller with DTMF generator PCD3344A; PCD3349A

1 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- ROM:
  - 2 kbytes (PCD3344A)
  - 4 kbytes (PCD3349A)
- 224 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 2 single-level vectored interrupts:
  - external
  - Timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent TONE output
- Filtering for low output distortion (CEPT compatible)
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF TONE output from 2.5 V)
- Low standby voltage of 1 V
- Low Stop mode current of 1 µA (typ.)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3344A and the PCD3349A provide 2 kbytes and 4 kbytes respectively of Program Memory, 224 bytes of RAM and 20 I/O lines.

The PCD3344A and PCD3349A are microcontrollers which have been designed primarily for telecom applications. They include an on-chip dual tone multifrequency (DTMF) generator.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family. This data sheet details the specific properties of the PCD3351A, PCD3352A and PCD3353A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the:

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3344AP; PCD3349AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3344AT; PCD3349AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

4 BLOCK DIAGRAM

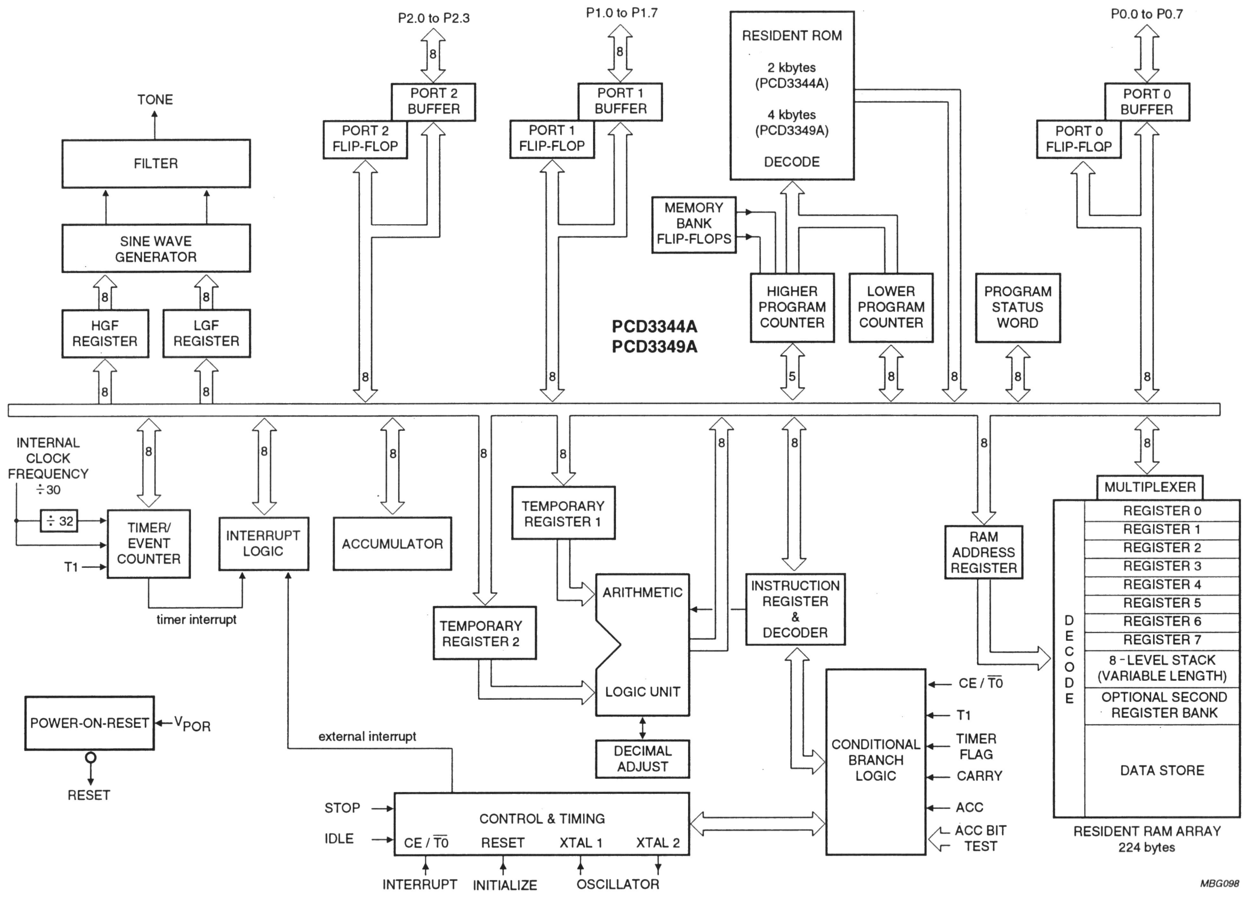

TONE
FILTER
SINE WAVE GENERATOR
8
8
HGF REGISTER
LGF REGISTER
8
8
P2.0 to P2.3
8
PORT 2 BUFFER
PORT 2 FLIP-FLOP
8
P1.0 to P1.7
8
PORT 1 BUFFER
PORT 1 FLIP-FLOP
8
RESIDENT ROM
2 kbytes
(PCD3344A)
4 kbytes
(PCD3349A)
DECODE
MEMORY BANK FLIP-FLOPS
HIGHER PROGRAM COUNTER
5
LOWER PROGRAM COUNTER
8
8
PROGRAM STATUS WORD
8
P0.0 to P0.7
PORT 0 BUFFER
PORT 0 FLIP-FLOP
8
PCD3344A
PCD3349A
INTERNAL CLOCK FREQUENCY ÷30
÷ 32
T1
TIMER/ EVENT COUNTER
8
timer interrupt
INTERRUPT LOGIC
8
ACCUMULATOR
8
8
TEMPORARY REGISTER 2
8
TEMPORARY REGISTER 1
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
8
INSTRUCTION REGISTER & DECODER
8
8
RAM ADDRESS REGISTER
8
MULTIPLEXER
DECODE
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 - LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
RESIDENT RAM ARRAY 224 bytes
CONDITIONAL BRANCH LOGIC
CE / $\overline{T0}$
T1
TIMER FLAG
CARRY
ACC
ACC BIT TEST
POWER-ON-RESET
V_{POR}
RESET
external interrupt
STOP
IDLE
CONTROL & TIMING
CE / $\overline{T0}$
RESET
XTAL 1
XTAL 2
INTERRUPT
INITIALIZE
OSCILLATOR
MBG098

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

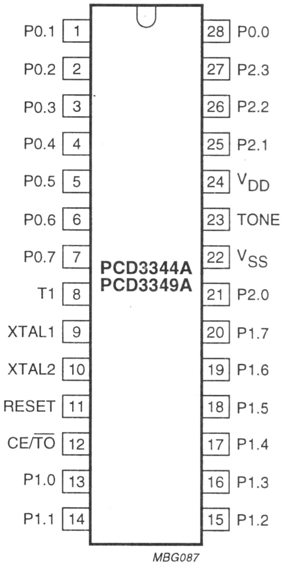

P0.1 1
P0.2 2
P0.3 3
P0.4 4
P0.5 5
P0.6 6
P0.7 7
T1 8
XTAL1 9
XTAL2 10
RESET 11
CE/$\overline{\text{T0}}$ 12
P1.0 13
P1.1 14
28 P0.0
27 P2.3
26 P2.2
25 P2.1
24 V_{DD}
23 TONE
22 V_{SS}
21 P2.0
20 P1.7
19 P1.6
18 P1.5
17 P1.4
16 P1.3
15 P1.2
PCD3344A
PCD3349A
MBG087

Fig.2 Pin configuration (SOT117-1 and SOT136-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines
T1	8	Test 1 or count input of 8-bit timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{\text{T0}}$	12	Chip Enable or Test 0
P1.0 to P1.7	13 to 20	Port 1: 8 quasi-bidirectional I/O lines
P2.0 to P2.3	21, 25, 26, 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.3). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

6.1 Frequency generator derivative registers

Table 2 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers. The addresses 03H to FFH are not used.

Table 2 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
01H	HGF(1)	H7	H6	H5	H4	H3	H2	H1	H0
02H	LGF(2)	L7	L6	L5	L4	L3	L2	L1	L0

Notes

1. HGF = High Group Frequency; access type W.
2. LGF = Low Group Frequency; access type W.

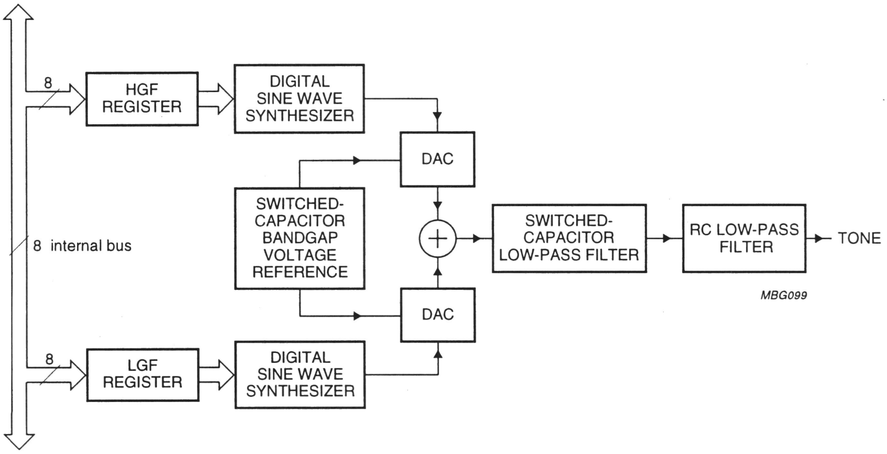

8
HGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER
DAC
SWITCHED-CAPACITOR BANDGAP VOLTAGE REFERENCE
8 internal bus
SWITCHED-CAPACITOR LOW-PASS FILTER
RC LOW-PASS FILTER
TONE
MBG099
DAC
8
LGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER

Fig.3 Block diagram of the frequency generator section.

6.2 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures TONE output levels independent of supply voltage and temperature. The amplitude of the Low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value ‘x’ held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.3 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 3.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 4.

Table 3 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 4 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.4 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 5 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low group frequency generation.

Table 5 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980(1)	978.82	−0.12	−1.18
82	1180(1)	1179.03	−0.08	−0.97
8F	1070(2)	1073.33	0.31	3.33
79	1270(2)	1265.30	−0.37	−4.70
80	1200(3)	1197.17	−0.24	−2.83
45	2200(3)	2192.01	−0.36	−7.99
76	1300(4)	1296.94	−0.24	−3.06
48	2100(4)	2103.14	0.15	3.14
5C	1650(1)	1655.66	0.34	5.66
52	1850(1)	1852.77	0.15	2.77
4B	2025(2)	2021.20	−0.19	−3.80
44	2225(2)	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.5 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 6). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low group frequency generation.

Table 6 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD(1)	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 TIMING

Although the PCD3344A and PCD3349A operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

8 RESET

In addition to the conditions given in the PCD33XXA family data sheet, all derivative registers are cleared in the RESET state.

9 STOP MODE

Since the oscillator is switched off, the frequency generator receives no clock. It is suggested to clear both the HGF and LGF registers before entering Stop mode. This will cut-off the biasing of the internal amplifiers, considerably reducing current requirements.

10 IDLE MODE

In the Idle mode, the frequency generator remains operative.

11 INSTRUCTION SET RESTRICTIONS

Since no serial I/O interface is provided, the serial I/O (Input/Output) instructions are not available. 'Mov Dx, A' is the only applicable derivative instruction because the derivative registers are write-only.

ROM space being restricted to 2 kbytes (PCD3344A) and 4 kbytes (PCD3349A) respectively, SEL MB1 (for PCD3344A) and SEL MB2/3 (for both PCD3344A and PCD3349A) would define non-existing Program Memory banks and should therefore be avoided.

RAM space being restricted to 224 bytes, care should be taken to avoid accesses to non-existing RAM locations.

12 SUMMARY OF MASK OPTIONS

Table 7 Port mask options

PORT NAME	PORT OUTPUT DRIVE(1)			PORT STATE AFTER RESET	
	OPTION 1	OPTION 2	OPTION 3	SET	RESET
Port 0 (P0.0 to P0.7)	X	X	X	X	X
Port 1 (P1.0 to P1.7)	X	X	X	X	X
Port 2 (P2.0 to P2.3)	X	X	X	X	X

Notes

1. Port output drives:
   a) Option 1: standard I/Ot.
   b) Option 2: open-drain I/O.
   c) Option 3: push-pull output. see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).

Table 8 Mask options

FEATURE	DESCRIPTION
ROM Code: program/data	Any mix of instructions and data up to ROM size of 2 kbytes (PCD3344A) and 4 kbytes (PCD3349A).
Power-on-reset voltage level: V_{POR}	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see note 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

15 DC CHARACTERISTICS

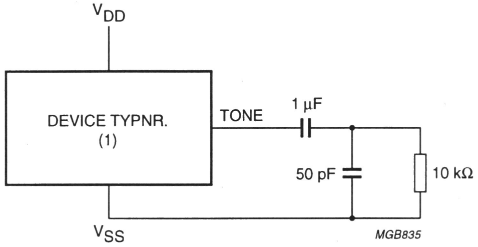
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 5 to 9)						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.9	1.8	mA
		V_{DD} = 3 V	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	2.5	6.0	mA
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V; value HGF = LGF =0	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 3	–	1.0	2.5	μA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 3	–	–	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	μA
Port outputs (see Figs 10 to 12)						
I_{OL}	LOW level port sink current	$V_{DD} = 3$ V; $V_O = 0.4$ V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	$V_O = 2.7$ V; $V_{DD} = 3$ V	–10	–20	–	μA
		$V_O = 0$ V; $V_{DD} = 3$ V	–	–100	–300	μA
I_{OH}	HIGH level port push-pull source current	$V_{DD} = 3$ V; $V_O = 2.6$ V	–0.7	–4	–	mA
TONE output (see Fig.4; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	$T_{amb} = 25$ °C; note 5	–	25	–	dB
Power-on-reset						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 6	–0.5	0	+0.5	V

Notes

1. TONE output requires $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
3. Crystal connected between XTAL1 and XTAL2; pins T1 and $CE/\overline{T0}$ at V_{SS}; value HGF = LGF = 0.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low group frequency (LGF) component (CEPT).
6. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.



(1) Device typenr.: PCD3344A or PCD3349A

Fig.4 TONE output test circuit.

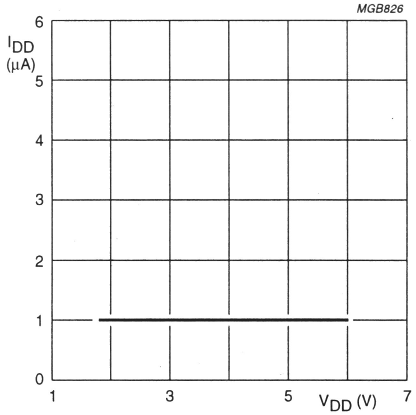
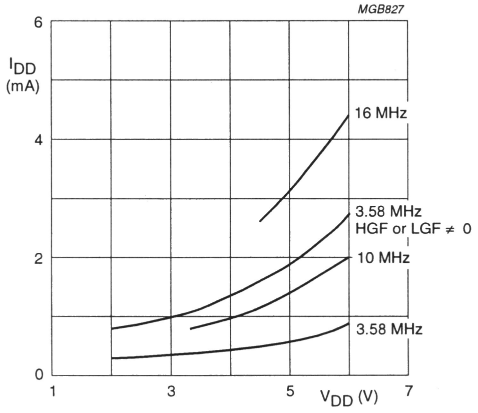
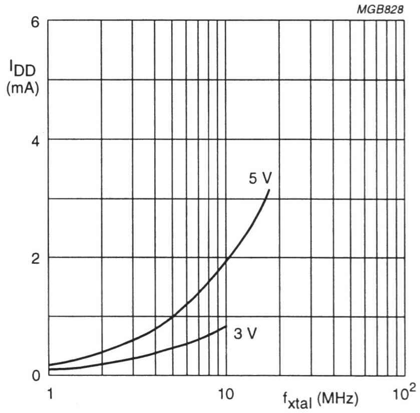


Fig.5 Typical supply current (I$_{DD}$) in Stop mode as a function of supply voltage (V$_{DD}$).



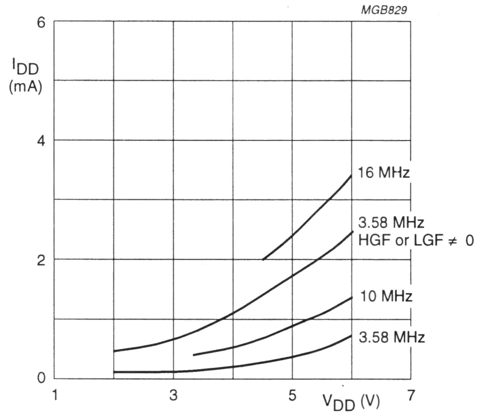
Measured with crystal between XTAL1 and XTAL2.

Fig.6 Typical operating supply current (I$_{DD}$) as a function of supply voltage (V$_{DD}$).



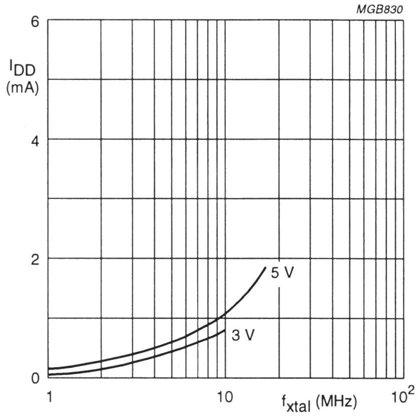
Measured with function generator on XTAL1.

Fig.7 Typical operating supply current (I$_{DD}$) as a function of clock frequency (f$_{xtal}$).



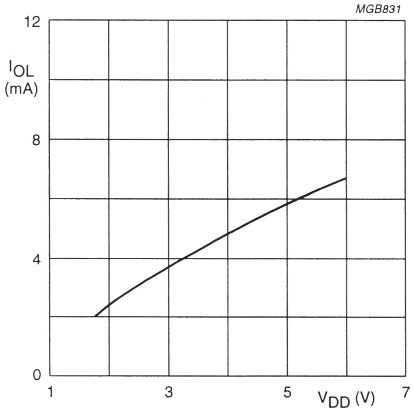
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.9 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



$V_O = 0.4$ V.

Fig.10 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

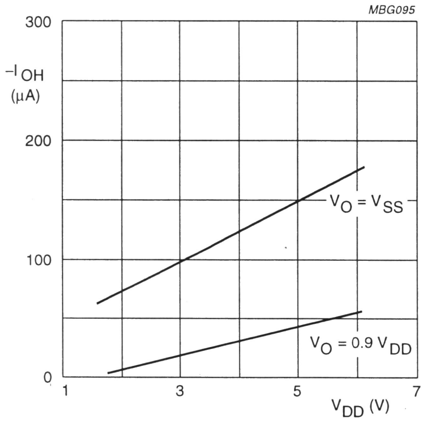
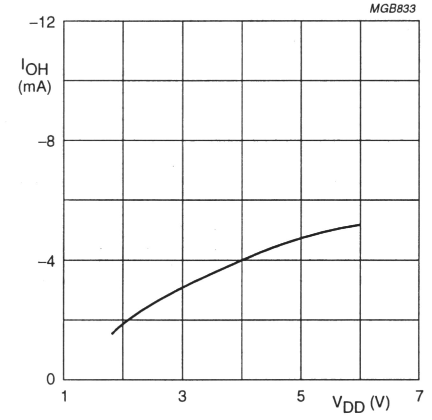


Fig.11 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.12 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

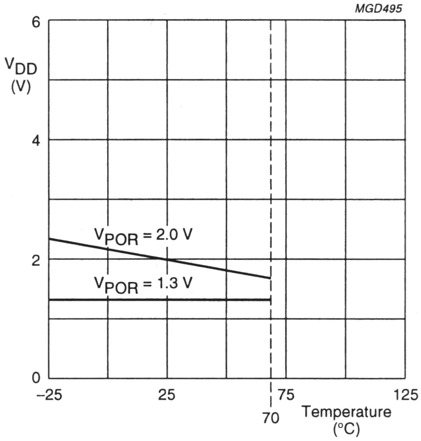


Fig.13 Typical Power-on-reset level (V_{POR}) as function of temperature.

16 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.14	1	–	16	MHz
Oscillator (see Fig.15)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance		0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance		3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

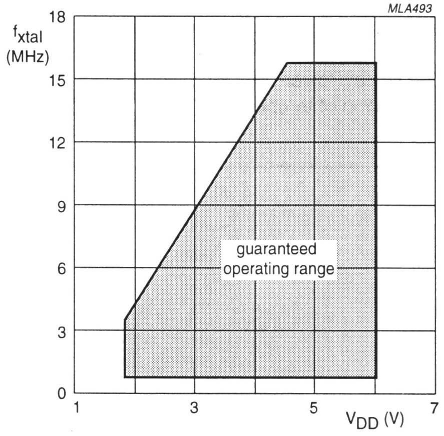


Fig.14 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

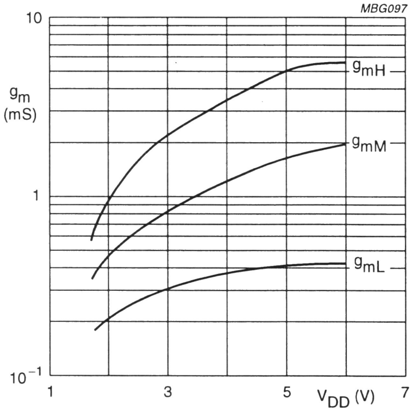


Fig.15 Typical transconductance as a function of supply voltage (V_{DD}).

8-bit microcontroller with DTMF generator, 256 bytes EEPROM and real-time clock

PCD3350A

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FREQUENCY GENERATOR
6.1 Frequency generator derivative registers
6.2 Melody output (P1.7/MDY)
6.3 DTMF clock divider and output (DP1.7/DCO)
6.4 Frequency registers
6.5 DTMF frequencies
6.6 Modem frequencies
6.7 Musical scale frequencies
7 EEPROM AND TIMER 2 ORGANIZATION
7.1 EEPROM registers
7.2 EEPROM latches
7.3 EEPROM flags
7.4 EEPROM macros
7.5 EEPROM access
7.6 Timer 2
8 REAL-TIME CLOCK
8.1 Oscillator
8.2 Divider chain
8.3 Frequency adjustment
8.4 Real-time clock derivative registers
9 DERIVATIVE INTERRUPTS
10 TIMING
11 RESET
12 IDLE MODE
13 STOP MODE
14 SUMMARY OF I/O PORTS AND MASK OPTIONS
15 SUMMARY OF DERIVATIVE REGISTERS
16 LIMITING VALUES
17 HANDLING
18 DC CHARACTERISTICS
19 AC CHARACTERISTICS
20 PACKAGE OUTLINES
21 SOLDERING
21.1 Introduction
21.2 Reflow soldering
21.3 Wave soldering
21.4 Repairing soldered joints
22 DEFINITIONS
23 LIFE SUPPORT APPLICATIONS

8-bit microcontroller with DTMF generator, 256 bytes EEPROM and real-time clock

PCD3350A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; all in a 44-lead quad flat package
- 8 kbytes ROM
- 256 bytes RAM
- 256 bytes Electrically Erasable Programmable Read Only Memory (EEPROM)
- 32 kHz crystal oscillator for Real-Time Clock (RTC)
- EEPROM programmable RTC
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 34 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU clock frequency: 1 to 16 MHz (3.58 MHz or 10.74 MHz for DTMF)
- Operating temperature: –25 to 70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3350A is a microcontroller oriented towards telephony applications. It includes 8 kbytes ROM, 256 bytes RAM, 34 I/O lines, and an on-chip dual tone multifrequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation.

The PCD3350A also incorporates 256 bytes of EEPROM, permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers. Finally, the PCD3350A includes a low power 32 kHz crystal oscillator with an EEPROM programmable Real-Time Clock (RTC) working in standby mode.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family. This data sheet details the specific properties of the PCD3350A. The shared characteristics of the PCD33xxA family of microcontrollers are described in the:

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3350AH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

4 BLOCK DIAGRAM

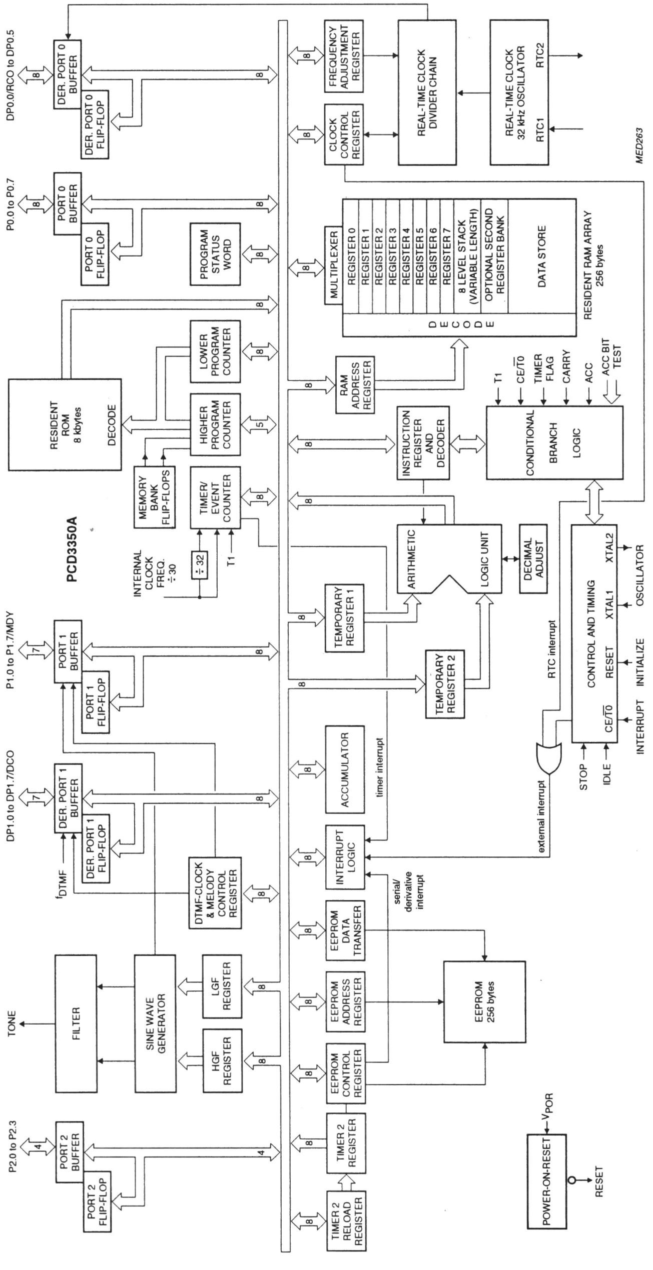

DP0.0/RC0 to DP0.5
DER. PORT 0 BUFFER
DER. PORT 0 FLIP-FLOP
P0.0 to P0.7
PORT 0 BUFFER
PORT 0 FLIP-FLOP
PROGRAM STATUS WORD
LOWER PROGRAM COUNTER
HIGHER PROGRAM COUNTER
RESIDENT ROM 8 kbytes
DECODE
MEMORY BANK FLIP-FLOPS
TIMER/ EVENT COUNTER
PCD3350A
INTERNAL CLOCK FREQ. ÷ 30
÷ 32
T1
P1.0 to P1.7/MDY
PORT 1 BUFFER
PORT 1 FLIP-FLOP
DP1.0 to DP1.7/DCO
DER. PORT 1 BUFFER
DER. PORT 1 FLIP-FLOP
f_{DTMF}
DTMF-CLOCK & MELODY CONTROL REGISTER
TONE
FILTER
SINE WAVE GENERATOR
LGF REGISTER
HGF REGISTER
P2.0 to P2.3
PORT 2 BUFFER
PORT 2 FLIP-FLOP
FREQUENCY ADJUSTMENT REGISTER
CLOCK CONTROL REGISTER
REAL-TIME CLOCK DIVIDER CHAIN
REAL-TIME CLOCK 32 kHz OSCILLATOR
RTC1
RTC2
MED263
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
RESIDENT RAM ARRAY 256 bytes
DECODE
RAM ADDRESS REGISTER
INSTRUCTION REGISTER AND DECODER
CONDITIONAL BRANCH LOGIC
T1
CE/$\overline{T0}$
TIMER FLAG
CARRY
ACC
ACC BIT TEST
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
TEMPORARY REGISTER 1
TEMPORARY REGISTER 2
CONTROL AND TIMING
XTAL2
XTAL1
RESET
CE/$\overline{T0}$
OSCILLATOR
INITIALIZE
INTERRUPT
RTC interrupt
STOP
IDLE
external interrupt
ACCUMULATOR
timer interrupt
INTERRUPT LOGIC
serial/ derivative interrupt
EEPROM DATA TRANSFER
EEPROM ADDRESS REGISTER
EEPROM CONTROL REGISTER
EEPROM 256 bytes
TIMER 2 REGISTER
TIMER 2 RELOAD REGISTER
POWER-ON-RESET
V_{POR}
RESET
8
7
5
4

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

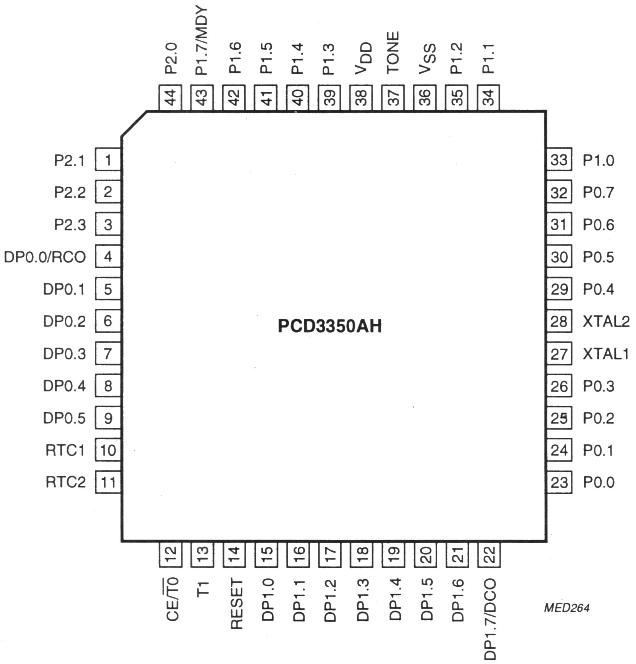

P2.0
P1.7/MDY
P1.6
P1.5
P1.4
P1.3
V_{DD}
TONE
V_{SS}
P1.2
P1.1
44
43
42
41
40
39
38
37
36
35
34
P2.1 1
P2.2 2
P2.3 3
DP0.0/RCO 4
DP0.1 5
DP0.2 6
DP0.3 7
DP0.4 8
DP0.5 9
RTC1 10
RTC2 11
PCD3350AH
33 P1.0
32 P0.7
31 P0.6
30 P0.5
29 P0.4
28 XTAL2
27 XTAL1
26 P0.3
25 P0.2
24 P0.1
23 P0.0
12
13
14
15
16
17
18
19
20
21
22
CE/$\overline{T0}$
T1
RESET
DP1.0
DP1.1
DP1.2
DP1.3
DP1.4
DP1.5
DP1.6
DP1.7/DCO
MED264

Fig.2 Pin configuration (SOT205-1).

5.2 Pin description

Table 1 SOT205-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
P2.0 to P2.3	44, 1 to 3	Port 2: 4 quasi-bidirectional I/O lines
DP0.0/RCO	4	Derivative Port 0: quasi-bidirectional I/O line or RTC output
DP0.1 to DP0.5	5 to 9	Derivative Port 0: 5 quasi-bidirectional I/O lines
RTC1	10	RTC 32 kHz oscillator input
RTC2	11	RTC 32 kHz oscillator output
CE/$\overline{\mathrm{T0}}$	12	Chip Enable or Test 0
T1	13	Test 1/count input of 8-bit Timer/event counter 1
RESET	14	reset input
DP1.0 to DP1.6	15 to 21	Derivative Port 1: 7 quasi bidirectional I/O lines
DP1.7/DCO	22	Derivative Port 1: quasi bidirectional I/O line or DTMF clock output
P0.0 to P0.7	23 to 26, 29 to 32	Port 0: 8 quasi-bidirectional I/O lines
XTAL1	27	crystal oscillator/external clock input
XTAL2	28	crystal oscillator output
P1.0 to P1.6	33 to 35, 39 to 42	Port 1: 7 quasi-bidirectional I/O lines
V_{SS}	36	ground
TONE	37	DTMF output
V_{DD}	38	positive supply voltage
P1.7/MDY	43	Port 1: quasi-bidirectional I/O line or melody output

6 FREQUENCY GENERATOR

A versatile frequency generator section with built-in programmable clock divider is provided (see Fig.3). The clock divider allows the DTMF section to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = \frac{1}{3} \times f_{xtal}$) depending on the state of the divider control bit DIV3 (see Table 4). The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available. Their frequencies are provided either in purely sinusoidal form on the TONE output or as a square wave on the port line P1.7/MDY. The latter is typically for ringer applications in telephone sets. In case no tones are generated the TONE output is in tri-state mode.

6.1 Frequency generator derivative registers

6.1.1 HIGH AND LOW GROUP FREQUENCY REGISTERS

Table 2 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers HGF (High Group Frequency) and LGF (Low Group Frequency); access type W.

Table 2 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
11H	HGF	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 CLOCK AND MELODY CONTROL REGISTER (MDYCON)

Table 3 Clock and Melody Control Register (address 13H; access type R/W)

7	6	5	4	3	2	1	0
0	0	0	0	0	EDCO	DIV3	EMO

Table 4 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These bits are set to a logic 0.
2	EDCO	Enable DTMF clock output. If bit EDCO = 0, then DP1.7/DCO is a general purpose derivative port line. If bit EDCO = 1, then DP1.7/DCO is the DTMF clock output. EDCO = 1 does not inhibit the port instructions for DP1.7/DCO. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of DP1.7/DCO must remain set to avoid conflicts between DTMF clock and port outputs.
1	DIV3	Enable DTMF clock divider. If bit DIV3 = 0, then the DTMF clock $f_{DTMF} = f_{xtal}$. If bit DIV3 = 1, then $f_{DTMF} = \frac{1}{3} \times f_{xtal}$.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the HIGH state.

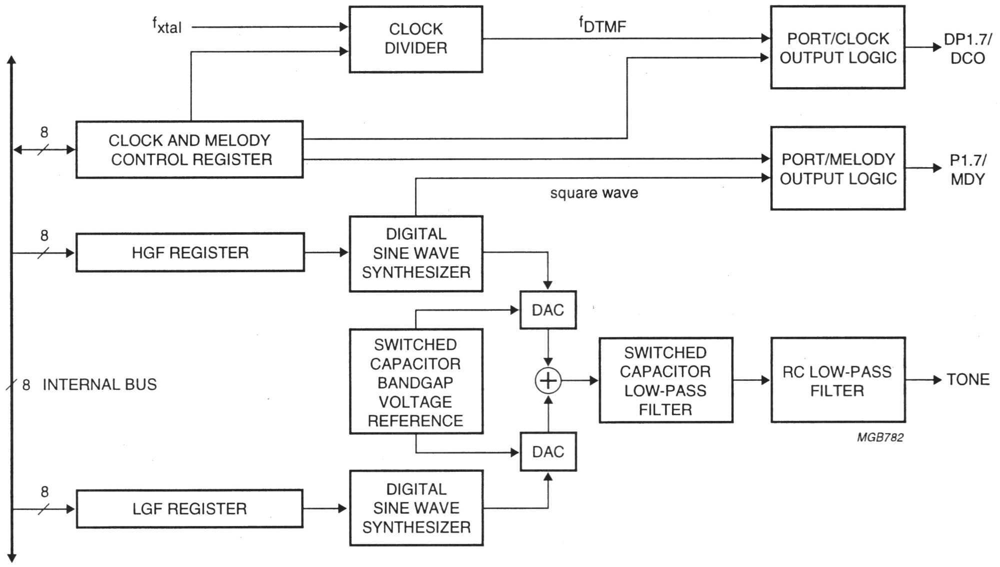

f_{xtal}
CLOCK DIVIDER
f_{DTMF}
PORT/CLOCK OUTPUT LOGIC
DP1.7/ DCO
8
CLOCK AND MELODY CONTROL REGISTER
PORT/MELODY OUTPUT LOGIC
P1.7/ MDY
square wave
8
HGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER
DAC
SWITCHED CAPACITOR BANDGAP VOLTAGE REFERENCE
8 INTERNAL BUS
SWITCHED CAPACITOR LOW-PASS FILTER
RC LOW-PASS FILTER
TONE
MGB782
DAC
8
LGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER

Fig.3 Block diagram of the frequency generator, melody output (P1.7/MDY) and DTMF clock output (DP1.7/DCO).

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 2). However, even higher frequency notes may be produced since the limitation $60 \leq x \leq 255$ is relaxed to $2 \leq x \leq 255$ in this application; x = decimal value of the HGF register contents. Due to the low-pass filters, the simultaneous signal on the TONE output is not useful for $x < 60$.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set high before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 14, Table 27.

6.3 DTMF clock divider and output (DP1.7/DCO)

The DTMF clock divider allows the DTMF part to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = ^1/_3 \times f_{xtal}$) depending on the state of the divider control bit DIV3 in register MDYCON.

For low power applications, a 3.58 MHz quartz crystal or PXE resonator can be chosen together with the divide-by-one function of the clock divider.

For applications a 10.74 MHz quartz crystal or PXE resonator may be chosen together with the divide-by-three function of the clock divider. This triples the program speed of the microcontroller, thereby keeping the assumed DTMF frequency of 3.58 MHz.

Since a 3.58 MHz clock is needed for peripheral telephony circuits such as the analog voice scrambler/descrambler PCD4440, a switchable DTMF clock output is provided depending on the state of the enable clock output bit EDCO in register MDYCON.

If EDCO = 1 and DIV3 = 1 in the MDYCON register: a square wave with the frequency $f_{DTMF} = ^1/_3 \times f_{xtal}$ is output on the derivative port line DP1.7/DCO. If EDCO = 1 and DIV3 = 0: a square wave with the frequency $f_{DTMF} = f_{xtal}$ is output on the derivative port line DP1.7/DCO.

The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 14, Table 27.

6.4 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the Low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value ‘x’ held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23(x+2)]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.5 DTMF frequencies

Assuming a oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 5.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 6.

Table 5 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 6 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.6 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 7 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low group frequency generation.

Table 7 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980(1)	978.82	−0.12	−1.18
82	1180(1)	1179.03	−0.08	−0.97
8F	1070(2)	1073.33	0.31	3.33
79	1270(2)	1265.30	−0.37	−4.70
80	1200(3)	1197.17	−0.24	−2.83
45	2200(3)	2192.01	−0.36	−7.99
76	1300(4)	1296.94	−0.24	−3.06
48	2100(4)	2103.14	0.15	3.14
5C	1650(1)	1655.66	0.34	5.66
52	1850(1)	1852.77	0.15	2.77
4B	2025(2)	2021.20	−0.19	−3.80
44	2225(2)	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.7 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 8). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low group frequency generation.

Table 8 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD(1)	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3350A has 256 bytes of Electrically Erasable Programmable Read Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCD3350A.

First, the EEPROM array is structured into 64 four-byte pages (see Fig.4) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes.

Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

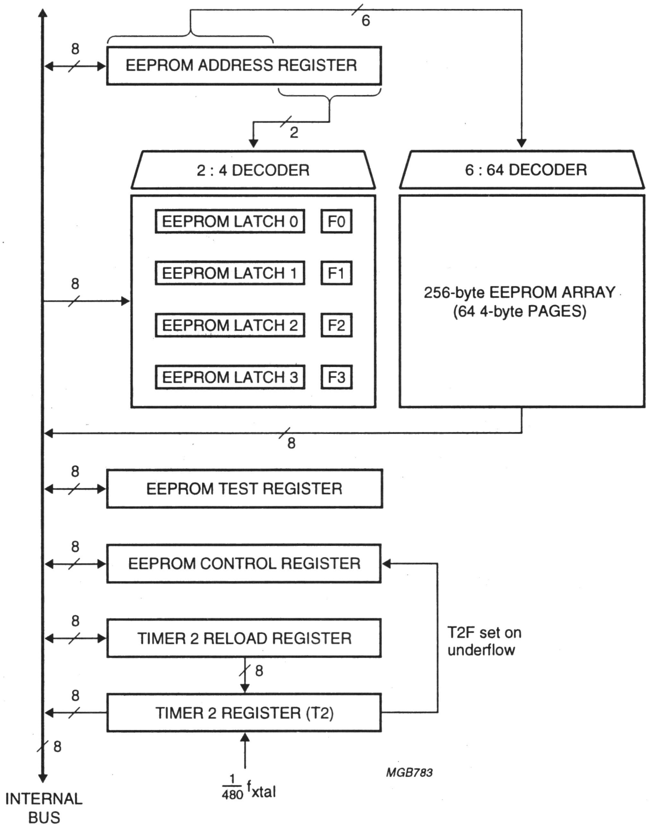

6
8
EEPROM ADDRESS REGISTER
2
2 : 4 DECODER
6 : 64 DECODER
EEPROM LATCH 0
F0
EEPROM LATCH 1
F1
EEPROM LATCH 2
F2
EEPROM LATCH 3
F3
8
256-byte EEPROM ARRAY (64 4-byte PAGES)
8
8
EEPROM TEST REGISTER
8
EEPROM CONTROL REGISTER
8
TIMER 2 RELOAD REGISTER
T2F set on underflow
8
8
TIMER 2 REGISTER (T2)
8
INTERNAL BUS
$\frac{1}{480}$ fxtal
MGB783

Fig.4 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. The register access type is R/W.

Table 9 EEPROM Control Register (address 04H)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 10 Description of EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 11.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 11 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed. The register access type is R/W.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 12 EEPROM Address Register (address 01H)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 13 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (see Table 11) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 14 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 15 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.4) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test Register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.4) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.4) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 22). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 9.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 12), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.4) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.4) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches. ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect.

Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 16).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 11) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 17.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 16 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 17 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 18 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 19.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of ‘write page’.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 19 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	‘write page’ control word
MOV EPCR, A	start ‘write page’ cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 20 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 21 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $\frac{1}{480} \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $\frac{1}{480} \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 22 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 22 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE(1) (HEX)
1	0A
2	14
3.58	25
6	3E
10.74	6F
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times \frac{1}{480} \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer 2 Register T2 (see Table 29) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 REAL-TIME CLOCK

The Real Time Clock (RTC) consists of a 32 kHz crystal oscillator, a 32 kHz to 1 second or 1 minute divider chain, an 8-bit Frequency Adjustment Register and the Clock Control Register. The complete RTC section works independent of the microcontroller status, even in Idle and Stop mode.

8.1 Oscillator

The internal 32 kHz oscillator needs an external quartz crystal with a frequency of 32768.00 Hz (a positive deviation up to +259 ppm is allowed) and an external feedback resistor between pins RTC1 and RTC2; 4.7 MΩ is recommended. It is controlled by the RUN-bit in the Clock Control Register.

8.2 Divider chain

The divider chain operates with the 32 kHz oscillator output and divides this signal down to two clocks with a period of 1 second or 1 minute. Depending on bit ITS in the Clock Control Register, the falling edge of the seconds or minutes clock is used to set the Clock Interrupt Flag (CIF) in the Clock Control Register.

Since the clock interrupt is used to let the microcontroller leave the Stop mode, it is ORed to the external interrupt ($\mathrm{CE}/\overline{\mathrm{T0}}$) and has the same functionality, e.g. it must be enabled in the Clock Control Register (bit ECI) and by execution of the instruction 'EN I'. The clock interrupt will then be treated as an external interrupt.

Additionally, the divider chain generates a 16 kHz clock (RCO) that can be routed through derivative port line DP0.0/RCO, controlled by bit ERCO in the Clock Control Register.

8.3 Frequency adjustment

The frequency adjustment is used to extend the interrupt time by defining the number of 16 kHz clocks in the Frequency Adjustment Register that will be counted twice within the first second period after a minute interrupt.

If the second interrupt is used (ITS = 1), every 60th interval may be up to 15.3 ms longer than the others as a result of the frequency adjustment. The adjusted Minute Interrupt Time (MIT) shows now a maximum deviation of 0.5 ppm.

8.4 Real-time clock derivative registers

8.4.1 CLOCK CONTROL REGISTER (CLCR)

The register access type is R/W and the value at reset is 00H.

Table 23 Clock Control Register (address 20H)

7	6	5	4	3	2	1	0
0	TST2	TST1	ERCO	RUN	ITS	CIF	ECI

Table 24 Description of CLCR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6	TST2	Test 2 input. This is a testing bit; has to be fixed at a logic 0 by user software.
5	TST1	Test 1 input. This is a testing bit; has to be fixed at a logic 0 by user software.
4	ERCO	Enable 16 kHz clock output. If ERCO = 0, then the DP0.0/RCO is a derivative port line. If ERCO = 1, then DP0.0./RCO is a 16 kHz clock output. ERCO = 1 does not inhibit the port instructions for DP0.0/RCO. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of DP0.0/RCO must remain set to avoid conflicts between 16 kHz clock and port outputs.
3	RUN	Clock run or stop bit. If RUN = 0, then the oscillator is stopped and the clock is reset. If RUN = 1, then the oscillator and the clock are running.
2	ITS	Interrupt Time Select. If ITS = 1, then the interrupt time is one second. If ITS = 0, then the interrupt time is one minute.
1	CIF	Clock Interrupt Flag. Set by hardware, if RTC divider chain overflows (every second or minute depending on ITS) or by program. Reset by program.
0	ECI	Enable Clock Interrupt. If ECI = 0, then CIF event cannot request interrupt. If ECI = 1, then CIF event requests interrupt.

8.4.2 FREQUENCY ADJUSTMENT REGISTER (FAR)

The frequency adjustment value of the RTC is defined by the 8-bit Frequency Adjustment Register. The register access type is R/W. The value of FAR at reset is 00H.

The significance of the individual bits of FAR can be illustrated by the following equation:

$$\text{Minute Interrupt Time (MIT)} = \left(60 \times 2^{\frac{14}{f_{RCO}}}\right) + \frac{FAR}{2^{14}}$$

where f_{RCO} = RTC frequency and ‘FAR’ is the decimal contents of the Frequency Adjustment Register.

Table 26 shows the recommended correction factor FAR for all allowed RTC frequencies f_{RCO}.

Table 25 Frequency Adjustment Register (address 21H)

7	6	5	4	3	2	1	0
FAR7	FAR6	FAR5	FAR4	FAR3	FAR2	FAR1	FAR0

Table 26 FAR as a result of f_{RCO}

f_{RCO}	FAR (HEX)
16384.000	00
16384.018	01
16384.033	02
16384.051	03
16384.066	04
16384.084	05
16384.100	06
16384.117	07
16384.135	08
16384.150	09
16384.168	0A
16384.184	0B
16384.201	0C
16384.217	0D
16384.234	0E
16384.250	0F
16384.268	10
16384.283	11
16384.301	12
16384.316	13
16384.334	14
16384.350	15
16384.367	16
16384.385	17
16384.400	18
16384.418	19
16384.434	1A
16384.451	1B
16384.467	1C
16384.484	1D
16384.500	1E
16384.518	1F
16384.533	20
16384.551	21
16384.566	22
16384.584	23
16384.600	24
16384.617	25
16384.635	26
16384.650	27
16384.668	28
16384.684	29
16384.701	2A
16384.717	2B
16384.734	2C
16384.750	2D
16384.768	2E
16384.783	2F
16384.801	30
16384.816	31
16384.834	32
16384.850	33
16384.867	34
16384.885	35
16384.900	36
16384.918	37
16384.934	38
16384.951	39
16384.967	3A
16384.984	3B
16385.000	3C
16385.018	3D
16385.033	3E
16385.051	3F
16385.066	40
16385.084	41
16385.100	42
16385.117	43
16385.135	44
16385.150	45
16385.168	46
16385.184	47
16385.201	48
16385.217	49
16385.234	4A
16385.250	4B
16385.268	4C
16385.283	4D
16385.301	4E
16385.316	4F
16385.334	50
16385.350	51
16385.367	52
16385.385	53
16385.400	54
16385.418	55
16385.434	56
16385.451	57
16385.467	58
16385.484	59
16385.500	5A
16385.518	5B

f_{RCO}	FAR (HEX)
16385.533	5C
16385.551	5D
16385.566	5E
16385.584	5F
16385.600	60
16385.617	61
16385.635	62
16385.650	63
16385.668	64
16385.684	65
16385.701	66
16385.717	67
16385.734	68
16385.750	69
16385.768	6A
16385.783	6B
16385.801	6C
16385.816	6D
16385.834	6E
16385.850	6F
16385.867	70
16385.885	71
16385.900	72
16385.918	73
16385.934	74
16385.951	75
16385.967	76
16385.984	77

f_{RCO}	FAR (HEX)
16386.000	78
16386.018	79
16386.033	7A
16386.051	7B
16386.066	7C
16386.084	7D
16386.100	7E
16386.117	7F
16386.135	80
16386.150	81
16386.168	82
16386.184	83
16386.201	84
16386.217	85
16386.234	86
16386.250	87
16386.268	88
16386.283	89
16386.301	8A
16386.316	8B
16386.334	8C
16386.350	8D
16386.367	8E
16386.385	8F
16386.400	90
16386.418	91
16386.434	92
16386.451	93

f_{RCO}	FAR (HEX)
16386.467	94
16386.484	95
16386.500	96
16386.518	97
16386.533	98
16386.551	99
16386.566	9A
16386.584	9B
16386.600	9C
16386.617	9D
16386.635	9E
16386.650	9F
16386.668	A0
16386.684	A1
16386.701	A2
16386.717	A3
16386.734	A4
16386.750	A5
16386.768	A6
16386.783	A7
16386.801	A8
16386.816	A9
16386.834	AA
16386.850	AB
16386.867	AC
16386.885	AD
16386.900	AE
16386.918	AF

f_{RCO}	FAR (HEX)
16386.934	B0
16386.951	B1
16386.967	B2
16386.984	B3
16387.000	B4
16387.018	B5
16387.033	B6
16387.051	B7
16387.066	B8
16387.084	B9
16387.100	BA
16387.117	BB
16387.135	BC
16387.150	BD
16387.168	BE
16387.184	BF
16387.201	C0
16387.217	C1
16387.234	C2
16387.250	C3
16387.268	C4
16387.283	C5
16387.301	C6
16387.316	C7
16387.334	C8
16387.350	C9
16387.367	CA
16387.385	CB
16387.400	CC
16387.418	CD
16387.434	CE
16387.451	CF
16387.467	D0
16387.484	D1
16387.500	D2
16387.518	D3
16387.533	D4
16387.551	D5
16387.566	D6
16387.584	D7
16387.600	D8
16387.617	D9
16387.635	DA
16387.650	DB
16387.668	DC
16387.684	DD
16387.701	DE
16387.717	DF
16387.734	E0
16387.750	E1
16387.768	E2
16387.783	E3
16387.801	E4
16387.816	E5
16387.834	E6
16387.850	E7
16387.867	E8
16387.885	E9
16387.900	EA
16387.918	EB
16387.934	EC
16387.951	ED
16387.967	EE
16387.984	EF
16388.002	F0
16388.018	F1
16388.035	F2
16388.051	F3
16388.068	F4
16388.084	F5
16388.102	F6
16388.117	F7
16388.135	F8
16388.152	F9
16388.168	FA
16388.186	FB
16388.201	FC
16388.219	FD
16388.234	FE
16384.000	FF

9 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 9 and 10).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

Although the clock interrupt is part of a derivative function it is linked to the external interrupt. A clock interrupt request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The enable clock interrupt bit in the derivative clock control register is set.

10 TIMING

Although the PCD3350A operates over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz or 10.74 MHz will usually be chosen to take full advantage of the frequency generator (DTMF) section.

11 RESET

In addition to the conditions given in the *“PCD33xxA Family”* data sheet, all derivative registers are cleared in the reset state.

12 IDLE MODE

In Idle mode all derivative functions remain operative, i.e.:

- DTMF generator
- DTMF clock divider and output
- 32 kHz crystal oscillator and RTC
- EEPROM and Timer 2 sections.

13 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

The 32 kHz crystal oscillator and the RTC section remain operative during Stop mode (depending only on bit RUN in the Clock Control Register). In addition to the description in the *“PCD33xxA Family”* data sheet, Stop mode may be left by a clock interrupt event (see Section 9).

14 SUMMARY OF I/O PORTS AND MASK OPTIONS

All standard quasi-bidirectional I/O ports are available; see *"PCD33XXA Family"* data sheet.

- Port 0: 8 parallel port lines P0.0 to P0.7
- Port 1: 8 parallel port lines P1.0 to P1.7
- Port 2: 4 parallel port lines P2.0 to P2.3.

In addition to the standard ports, 2 derivative I/O ports are available:

- Derivative Port 0: 6 parallel port lines DP0.0 to DP0.5 (register DP0I)
- Derivative Port 1: 8 parallel port lines DP1.0 to DP1.7 (register DP1I).

See Table 29 for the addresses of DP0I and DP1I.

Table 27 Port mask options

PORT NAME	PORT OUTPUT DRIVE(1)			PORT STATE AFTER RESET	
	OPTION 1	OPTION 2	OPTION 3	SET (H)	RESET (L)
P0.0 to P0.7	X	X	X	X	X
P1.0 to P1.6	X	X	X	X	X
P1.7/MDY(2)	X	X	X	X	X
P2.0 to P2.3	X	X	X	X	X
DP0.0 to DP0.5	X	X	X	X	X
DP1.0 to DP1.6	X	X	X	X	X
DP1.7/DCO(3)	X	X	X	X	X

Notes

1. Port Output Drive (see *"PCD33xxA Family"* data sheet):
    a) Option 1: standard I/O.
    b) Option 2: open-drain I/O.
    c) Option 3: push-pull output
2. If Option 1 or 3 is chosen, the melody output becomes a push-pull output; if Option 2 is chosen, the melody output becomes an open-drain output.
3. If Option 1 or 3 is chosen, the DTMF clock output becomes a push-pull output; if Option 2 is chosen, the DTMF clock output becomes an open-drain output.

Table 28 Mask options

FEATURE	DESCRIPTION
ROM Code: program/data	Any mix of instructions and data up to ROM size of 8 kbytes.
Power-on-reset voltage level: V_{POR}	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

15 SUMMARY OF DERIVATIVE REGISTERS

Table 29 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Clock and Melody Control Register (MDYCON)	0	0	0	0	0	DCO	DIV3	EMO	R/W
14 to 1F	not used									
20	Clock Control Register (CLCR)	0	TST2	TST1	ERCO	RUN	ITS	CIF	ECI	R/W
21	Frequency Adjustment Register (FAR)	FAR7	FAR6	FAR5	FAR4	FAR3	FAR2	FAR1	FAR0	R/W
22 to 2F	not used									
30	Derivative Port 0 lines (DP0I)	0	0	D0.5	D0.4	D0.3	D0.2	D0.1	D0.0	R
31	Derivative Port 1 lines (DP1I)	D1.7	D1.6	D1.5	D1.4	D1.3	D1.2	D1.1	D1.0	R
32	Derivative Port 0 flip-flop (DP0FF)	0	0	F0.5	F0.4	F0.3	F0.2	F0.1	F0.0	R/W
33	Derivative Port 1 flip-flop (DP1FF)	F1.7	F1.6	F1.5	F1.4	F1.3	F1.2	F1.1	F1.0	R/W
34 to FF	not used									

16 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+7.0	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	–50	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

17 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

18 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); f_{RTC} = 32768 Hz (+200 ppm, –0); unless otherwise specified.

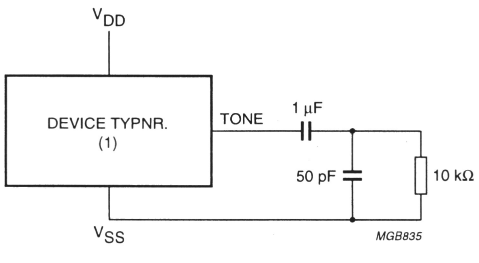
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 6, 7 and 10)						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V; value HGF = LGF = 0	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF ≠ LGF ≠ 0; DIV3 = 1	–	2.7	6.2	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.7	4.2	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	3.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V; value HGF = LGF =0	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF ≠ LGF ≠ 0; DIV3 = 1	–	2.3	5.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.3	3.5	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	2.4	–	mA
$I_{DD(ST)}$	supply current Stop mode; notes 2 and 3	V_{DD} = 1.8 V; T_{amb} = 25 °C; RTC not running	–	1.0	5.5	μA
		V_{DD} = 1.8 V; T_{amb} = –25 to 70 °C; RTC not running	–	–	10	μA
		V_{DD} = 1.8 V; T_{amb} = 25 °C; RTC running	–	2.0	6.0	μA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	μA
Port outputs (see Figs 11, 12 and 13)						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	–10	–30	–	μA
		V_{DD} = 3 V; V_O = 0 V	–	–140	–300	μA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–3.5	–	mA
Real-time clock 32 kHz oscillator						
g_m	transconductance	$V_{i(p-p)}$ < 50 mV; see Fig.17	2	10	50	μS
$\partial f/f$	frequency adjustment		–0.6	–	+0.6	ppm
C_I	input capacitance (pin 10)		–	10	–	pF
C_O	output capacitance (pin 11)		–	10	–	pF
TONE output (see Fig.5; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	–25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
n_{cyc}	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention		10	–	–	years
Power-on-reset						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 8	–0.5	0	+0.5	V

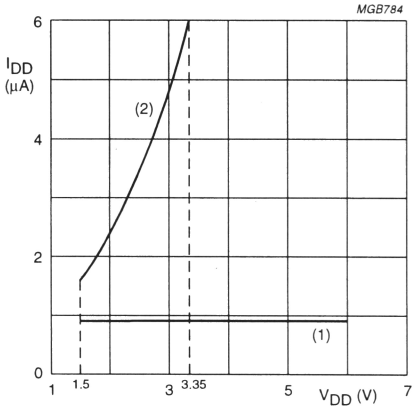
Notes

1. TONE output; EEPROM erase and write require $V_{DD} \geq 2.5$ V:
   a) TONE output requires $f_{xtal} < 4$ MHz in case DIV3 = 0.
   b) TONE output requires $f_{xtal} < 12$ MHz in case DIV3 = 1.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open:
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; open-drain outputs connected to V_{SS}; all other outputs open.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is typically logic 1.
7. Verified on sampling basis.
8. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.



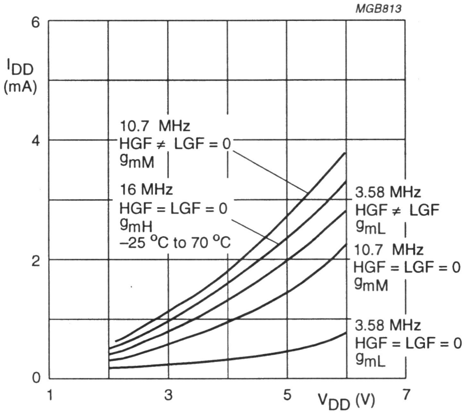
(1) Device typenr.: PCD3350A

Fig.5 Tone output test circuit.



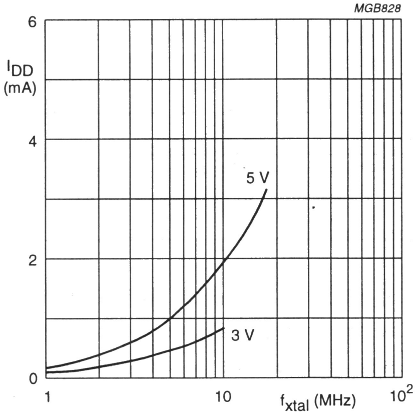
(1) RTC stopped; –25 to 70 °C.
(2) RTC running; –25 to 70 °C.

Fig.6 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



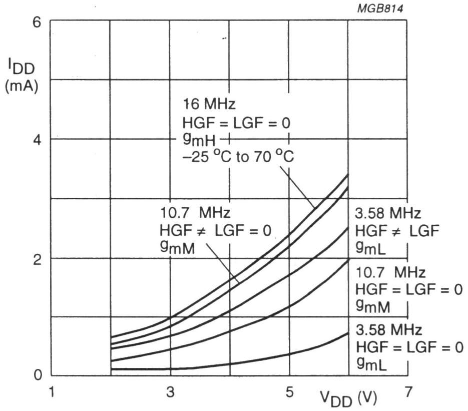
Measured with crystal between XTAL1 and XTAL2.

Fig.7 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



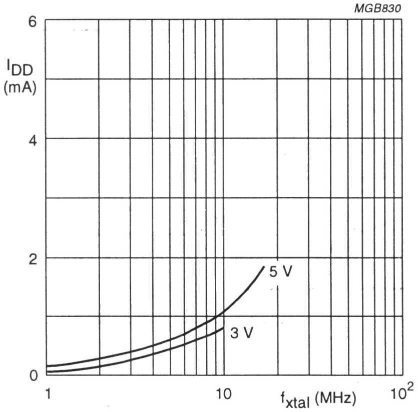
Measured with function generator on XTAL1.

Fig.8 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



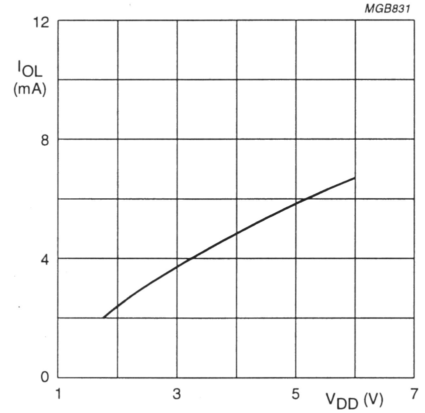
Measured with crystal between XTAL1 and XTAL2.

Fig.9 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.10 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



$V_O = 0.4$ V.

Fig.11 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

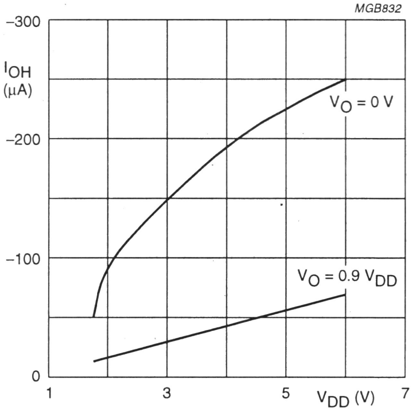
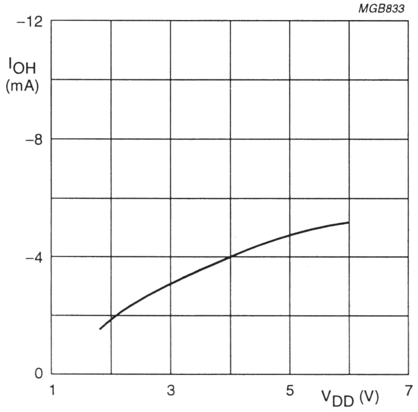


Fig.12 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.13 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

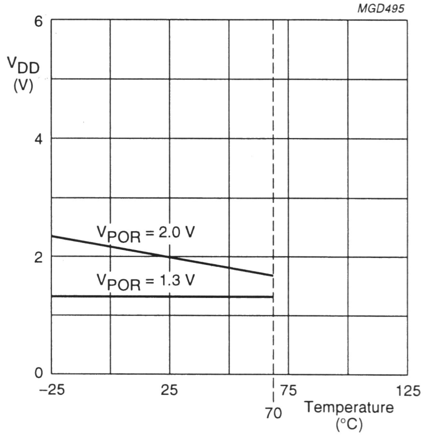


Fig.14 Typical Power-on-reset level (V_{POR}) as function of temperature.

19 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.15	1	–	16	MHz
Oscillator (see Fig. 16)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance		0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance		3	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

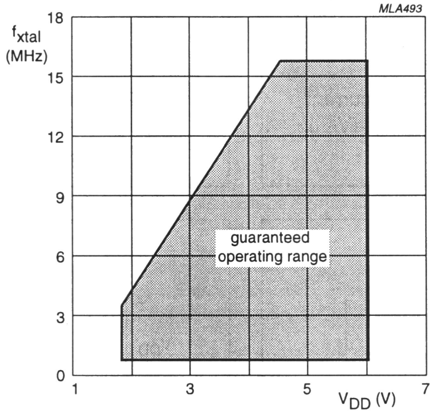


Fig.15 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

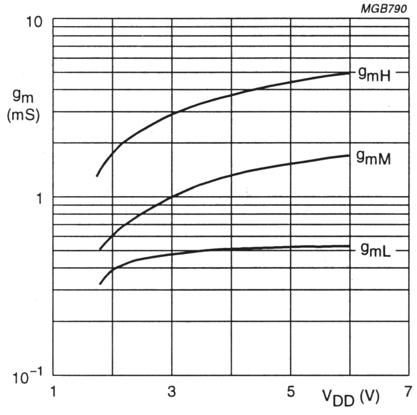


Fig.16 Typical oscillator transconductance as a function of supply voltage (V_{DD}).

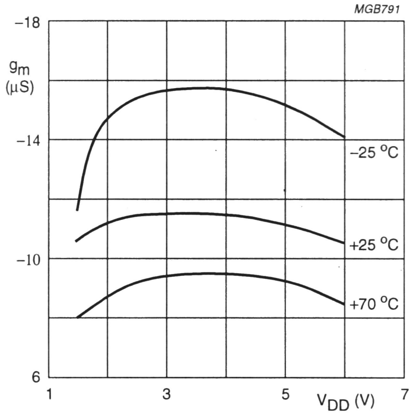


Fig.17 Typical RTC oscillator transconductance as a function of supply voltage (V_{DD}).

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FREQUENCY GENERATOR
6.1 Frequency generator derivative registers
6.2 Melody output (P1.7/MDY)
6.3 Frequency registers
6.4 DTMF frequencies
6.5 Modem frequencies
6.6 Musical scale frequencies
7 EEPROM AND TIMER 2 ORGANIZATION
7.1 EEPROM registers
7.2 EEPROM latches
7.3 EEPROM flags
7.4 EEPROM macros
7.5 EEPROM access
7.6 Timer 2
8 DERIVATIVE INTERRUPTS
9 TIMING
10 RESET
11 IDLE MODE
12 STOP MODE
13 INSTRUCTION SET RESTRICTIONS
14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATIONS
15 SUMMARY OF DERIVATIVE REGISTERS
16 LIMITING VALUES
17 HANDLING
18 DC CHARACTERISTICS
19 AC CHARACTERISTICS
20 PACKAGE OUTLINES
21 SOLDERING
21.1 Reflow soldering
21.2 Wave soldering
21.3 DIP
21.4 Repairing soldered joints
22 DEFINITIONS
23 LIFE SUPPORT APPLICATIONS

8-bit microcontrollers with DTMF generator and 128 bytes EEPROM

PCA3351C; 52C; 53C
PCD3351A; 52A; 53A; 55A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; all in one (28-lead or 32-lead) package
- ROM:
  - 2 kbytes (PCA3351C and PCD3351A)
  - 4 kbytes (PCA3352C and PCD3352A)
  - 6 kbytes (PCA3353C and PCD3353A)
  - 8 kbytes (PCD3355A)
- RAM:
  - 64 bytes (PCA3351C and PCD3351A)
  - 128 bytes (PCA3352C, PCA3353C, PCD3352A, PCD3353A and PCD3355A)
- 128 bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- 3 single-level vectored interrupts:
  - external
  - Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Logic supply from 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating temperature: –25 to 70 °C or 0 to 50 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The type numbers:

- 'PCA3351C; 52C; 53C' denotes the types PCA3351C, PCA3352C and PCA3353C, here after referred to as 'PCA335xC'.
- 'PCD3351A; 52A; 53A; 55A' denotes the types PCD3351A, PCD3352A, PCD3353A, PCD3355A, here after referred to as 'PCD335xA'.

The PCA335xC and PCD335xA are microcontrollers oriented towards telephony applications. They include an on-chip dual tone multifrequency (DTMF) generator. In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation.

The PCA335xC and PCD335xA also incorporate 128 bytes of EEPROM, permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The PCA335xC and PCD335xA can be emulated with the OTP microcontroller PCD3755x; see Chapter 14, Table 25.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family. This data sheet details the specific properties of the PCA335xC and PCD335xA. The shared characteristics of the PCD33xxA family of microcontrollers are described in the:

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

Differences between PCA335xC and PCD335xA are shown in Table 1.

Table 1 Differences: PCA3354C and PCD3354A

TYPE	V_{POR}	TEMP. RANGE
PCA335xC	fixed at 2.0 V ±0.3 V	0 to 50 °C
PCD335xA	(1.2 to 3.6 V) ±0.5 V(1)	–25 to 70 °C

Note

1. See Chapter 14, Table 26.

3 ORDERING INFORMATION

TYPE NUMBER(1)	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA335xCP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD335xAP			
PCA335xCT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD335xAT			
PCA335xCH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD335xAH			

Note

1. The types:
   a) PCA335xC denotes: PCA3351C, PCA3352C or PCA3353C.
   b) PCD335xA denotes: PCD3351A, PCD3352A, PCD3353A or PCD3355A.

4 BLOCK DIAGRAM

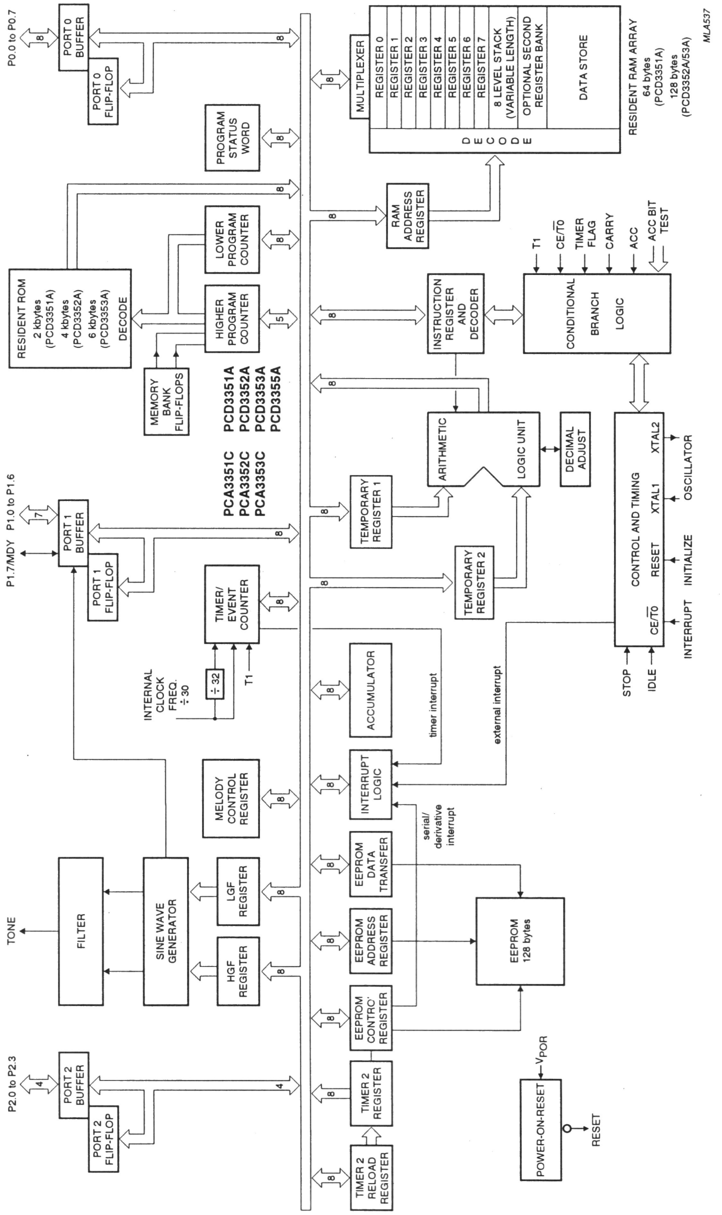
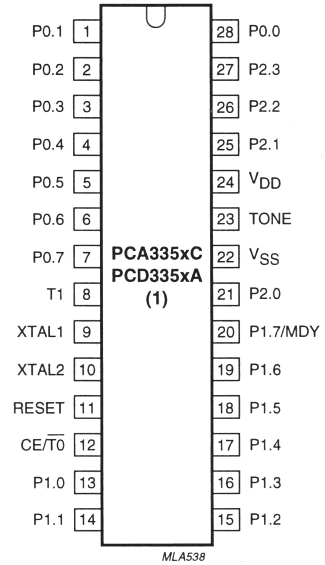

P0.0 to P0.7
8
PORT 0 BUFFER
PORT 0 FLIP-FLOP
PROGRAM STATUS WORD
RESIDENT ROM
2 kbytes (PCD3351A)
4 kbytes (PCD3352A)
6 kbytes (PCD3353A)
DECODE
LOWER PROGRAM COUNTER
HIGHER PROGRAM COUNTER
5
MEMORY BANK FLIP-FLOPS
PCD3351A
PCD3352A
PCD3353A
PCD3355A
PCA3351C
PCA3352C
PCA3353C
P1.7/MDY
P1.0 to P1.6
7
PORT 1 BUFFER
PORT 1 FLIP-FLOP
TIMER/ EVENT COUNTER
INTERNAL CLOCK FREQ. ÷ 30
÷ 32
T1
MELODY CONTROL REGISTER
TONE
FILTER
SINE WAVE GENERATOR
LGF REGISTER
HGF REGISTER
P2.0 to P2.3
4
PORT 2 BUFFER
PORT 2 FLIP-FLOP
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
DECODE
RESIDENT RAM ARRAY
64 bytes (PCD3351A)
128 bytes (PCD3352A/53A)
MLA537
RAM ADDRESS REGISTER
T1
CE/$\overline{T0}$
TIMER FLAG
CARRY
ACC
ACC BIT TEST
INSTRUCTION REGISTER AND DECODER
CONDITIONAL BRANCH LOGIC
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
TEMPORARY REGISTER 1
TEMPORARY REGISTER 2
CONTROL AND TIMING
XTAL2
XTAL1
OSCILLATOR
RESET
INITIALIZE
CE/$\overline{T0}$
INTERRUPT
STOP
IDLE
ACCUMULATOR
timer interrupt
external interrupt
INTERRUPT LOGIC
serial/ derivative interrupt
EEPROM DATA TRANSFER
EEPROM ADDRESS REGISTER
EEPROM 128 bytes
EEPROM CONTROL REGISTER
TIMER 2 REGISTER
TIMER 2 RELOAD REGISTER
POWER-ON-RESET
V_{POR}
RESET
8

Fig.1 Block diagram.

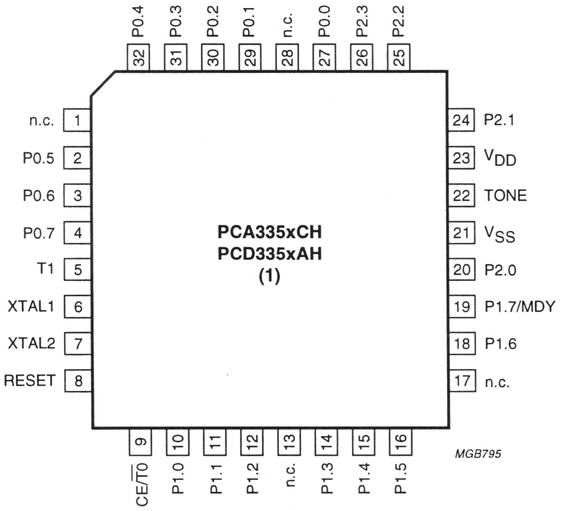
5 PINNING INFORMATION

5.1 Pinning


P0.1 1
P0.2 2
P0.3 3
P0.4 4
P0.5 5
P0.6 6
P0.7 7
T1 8
XTAL1 9
XTAL2 10
RESET 11
CE/$\overline{T0}$ 12
P1.0 13
P1.1 14
28 P0.0
27 P2.3
26 P2.2
25 P2.1
24 V$_{DD}$
23 TONE
22 V$_{SS}$
21 P2.0
20 P1.7/MDY
19 P1.6
18 P1.5
17 P1.4
16 P1.3
15 P1.2
PCA335xC
PCD335xA
(1)
MLA538

(1) **PCA335xC denotes**: PCA3351C, PCA3352C or PCA3353C
PCD335xA denotes: PCD3351A, PCD3352A, PCD3353A or PCD3355A.

Fig.2 Pin configuration (SOT117-1 and SOT136-1).


P0.4 32
P0.3 31
P0.2 30
P0.1 29
n.c. 28
P0.0 27
P2.3 26
P2.2 25
n.c. 1
P0.5 2
P0.6 3
P0.7 4
T1 5
XTAL1 6
XTAL2 7
RESET 8
24 P2.1
23 V$_{DD}$
22 TONE
21 V$_{SS}$
20 P2.0
19 P1.7/MDY
18 P1.6
17 n.c.
9 CE/$\overline{T0}$
10 P1.0
11 P1.1
12 P1.2
13 n.c.
14 P1.3
15 P1.4
16 P1.5
PCA335xCH
PCD335xAH
(1)
MGB795

(1) **PCA335xCH denotes**: PCA3351CH, PCA3352CH or PCA3353CH
PCD335xAH denotes: PCD3351AH, PCD3352AH, PCD3353AH or PCD3355AH.

Fig.3 Pin configuration (SOT358-1).

5.2 Pin description

Table 2 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines
T1	8	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{\text{T0}}$	12	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	20	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	21, 25 to 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

Table 3 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
T1	5	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	crystal oscillator or external clock input
XTAL2	7	crystal oscillator output
RESET	8	reset input
CE/$\overline{\text{T0}}$	9	Chip Enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	19	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	20, 24 to 26	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	21	ground
TONE	22	DTMF output
V_{DD}	23	positive supply voltage
P0.0 to P0.7	27, 29 to 32, 2 to 4	Port 0: 8 quasi-bidirectional I/O lines
n.c.	1, 13, 17, 28	not connected

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the port line P1.7/MDY.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

When no tones are generated the TONE output is in tri-state mode.

6.1 Frequency generator derivative registers

6.1.1 HIGH AND LOW GROUP FREQUENCY REGISTERS

Table 4 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers HGF (High Group Frequency) and LGF (Low Group Frequency); access type W.

Table 4 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
11H	HGF	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 MELODY CONTROL REGISTER (MDYCON)

The Melody Control Register is a R/W register.

Table 5 Melody Control Register (address 13H)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EMO

Table 6 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the HIGH state.

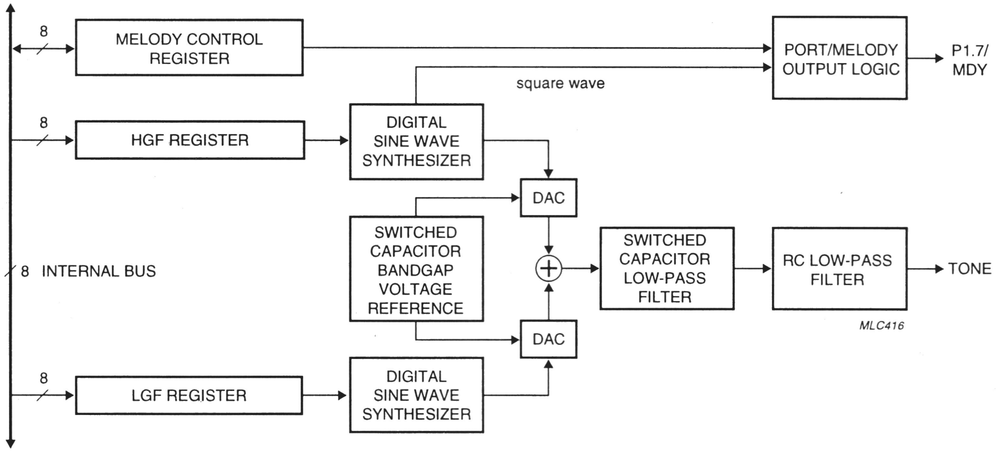

8
MELODY CONTROL REGISTER
PORT/MELODY OUTPUT LOGIC
P1.7/ MDY
square wave
8
HGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER
DAC
SWITCHED CAPACITOR BANDGAP VOLTAGE REFERENCE
8 INTERNAL BUS
SWITCHED CAPACITOR LOW-PASS FILTER
RC LOW-PASS FILTER
TONE
MLC416
DAC
8
LGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER

Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 4). However, even higher frequency notes may be produced since the limitation $60 \le x \le 255$ is relaxed to $2 \le x \le 255$ in this application; x = decimal value of the HGF register contents. Due to the low-pass filters, the simultaneous signal on the TONE output is not useful for $x < 60$.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 14, Table 26.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value ‘x’ held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]};\text{ where } 60 \le x \le 255.$$

The frequency limitation given by $x \ge 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 7.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 8.

Table 7 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 8 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 9 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low group frequency generation.

Table 9 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 10). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low group frequency generation

Table 10 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD335xA and PCA335xC have 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without he need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCD335xA and PCA335xC.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

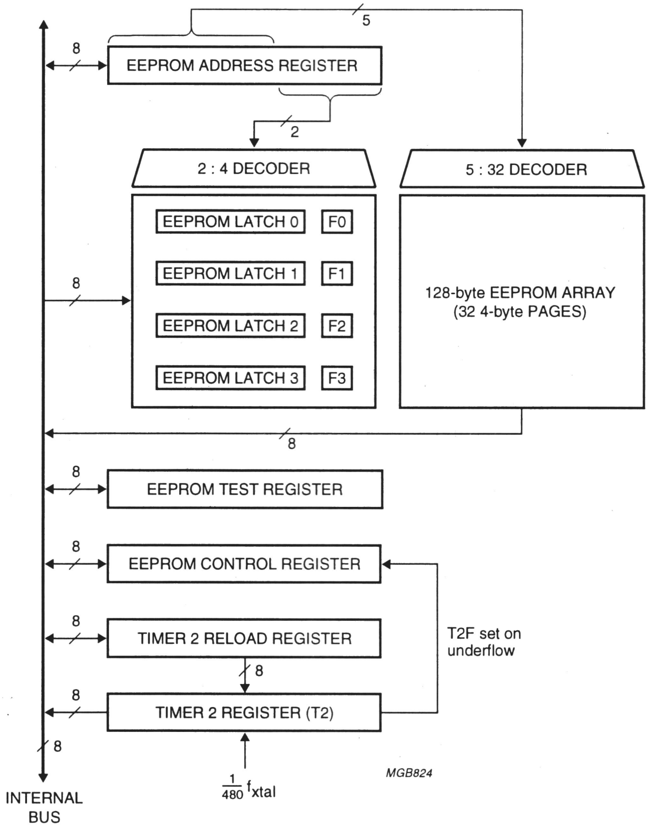

5
8
EEPROM ADDRESS REGISTER
2
2 : 4 DECODER
5 : 32 DECODER
EEPROM LATCH 0
F0
EEPROM LATCH 1
F1
EEPROM LATCH 2
F2
EEPROM LATCH 3
F3
8
128-byte EEPROM ARRAY
(32 4-byte PAGES)
8
8
EEPROM TEST REGISTER
8
EEPROM CONTROL REGISTER
8
TIMER 2 RELOAD REGISTER
T2F set on underflow
8
8
TIMER 2 REGISTER (T2)
8
INTERNAL BUS
1/480 fxtal
MGB824

Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. The register access type is R/W.

Table 11 EEPROM Control Register (address 04H)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 12 Description of the EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 13.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 13 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed. The register access type is R/W.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 14 EEPROM Address Register (address 01H)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 15 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 13) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 16 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 17 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 24). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 11.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 14), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 18).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 13) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 19.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 18 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 19 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 20 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 21.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 21 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 22 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 23 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $\frac{1}{480} \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $\frac{1}{480} \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 24 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 24 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE(1) (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times \frac{1}{480} \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 27) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 12).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

9 TIMING

Although the PCD335xA and PCA335xC operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33XXA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode.

After exit from Stop mode by a HIGH level on CE/$\overline{\text{T0}}$, Timer 2 proceeds from the held state.

13 INSTRUCTION SET RESTRICTIONS

- For PCD3351A and PCA3351C only:
  - ROM space being restricted to 2 kbytes, the 'SEL MB1/2/3' instructions would define non-existing program memory banks and should therefore be avoided.
  - RAM space being restricted to 64 bytes, care should be taken to avoid accesses to non-existing RAM locations.
- For PCD3352A and PCA3352C only:
  - ROM space being restricted to 4 kbytes, the 'SEL MB2/3' instructions would define non-existing program memory banks and should therefore be avoided.
- For PCD3353A and PCA3353Conly:
  - ROM space being restricted to 6 kbytes, the 'SEL MB3' instructions would define non-existing program memory banks and should therefore be avoided.
- For the PCD3352A, PCD3353A, PCD3355A, PCA3352C and PCA3353C, RAM space is restricted to 128 bytes, thus care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATIONS

- The PCA335xC microcontrollers support one port and Power-on-reset configuration which keeps the compatibility to the OTP PCD3755E.
- The PCD335xA microcontrollers support two port and Power-on-reset configurations which can be chosen: one is compatible to the OTP PCD3755A, the other is compatible to the OTP PCD3755E.

Table 25 Available mask configurations

TYPE	CONFIGURATION AS:	
	PCD3755A	PCD3755E
PCA3351C	–	X
PCA3352C	–	X
PCA3353C	–	X
PCD3351A	X	X
PCD3352A	X	X
PCD3353A	X	X
PCD3355A	X	X

Table 26 Port and Power-on-Reset configurations
See note 1 and 2.

COVERED BY OTP	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3755A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R[(3)]	2S	2S	2S	2S	1.3 V
PCD3755E	1S	1S	1S	1S	1S	1S	1S	1S	2S	2S	2S	2S	2S	2S	1S	1S[(3)]	2S	1R	1R	1R	2.0 V

Notes

1. Port output drive: 1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* datasheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The melody output drive type is push-pull.

15 SUMMARY OF DERIVATIVE REGISTERS

Table 27 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody Control Register (MDYCON)	0	0	0	0	0	0	0	EMO	R/W
14 to FF	not used									

16 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+7.0	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	–50	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

17 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

18 DC CHARACTERISTICS

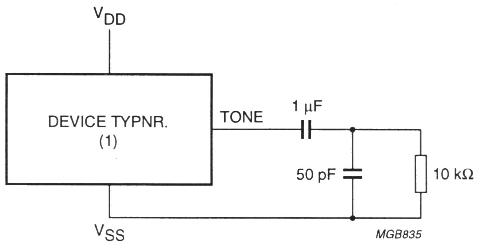
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA335xC) or −25 to +70 °C (PCD335xA); all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 7 to 11)						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 3	–	1.0	5.5	μA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 3	–	–	10	μA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	1	μA
Port outputs (see Figs 12 to 14)						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	−10	−30	–	μA
		V_{DD} = 3 V; V_O = 0 V	–	−140	−300	μA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	−0.7	−3.5	–	mA
Tone output (see Fig.6; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		−0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	**note** 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset						
V_{POR}	Power-on-reset level					
	PCD335xA	configuration as PCD3755A	0.8	1.3	1.8	V
	PCD335xA	configuration as PCD3755E	1.5	2.0	2.5	V
	PCA335xC	configuration as PCD3755E	1.7(8)	2.0	2.3	V

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: 25 C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/T0 at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{\text{T0}}$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.
8. Each device is tested on the condition: $V_{DD(min)} < V_{POR}$; to ensure a correct start-up, even for slow rising supply voltages.



(1) Device typenr.: PCA3351C, PCA3352C, PCA3353C, PCD3351A, PCD3352A, PCD3353A or PCD3355A

Fig.6 TONE output test circuit.

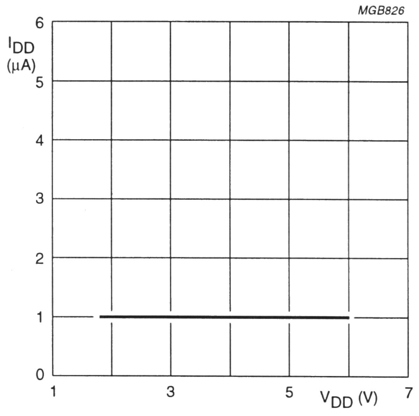
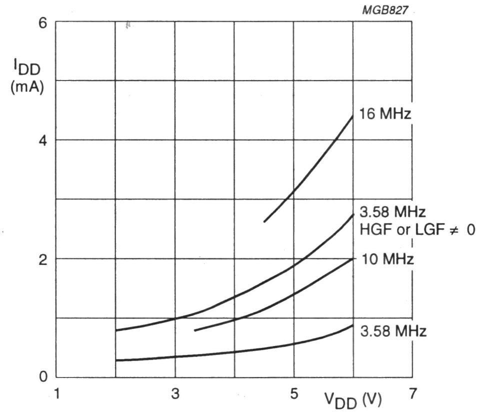
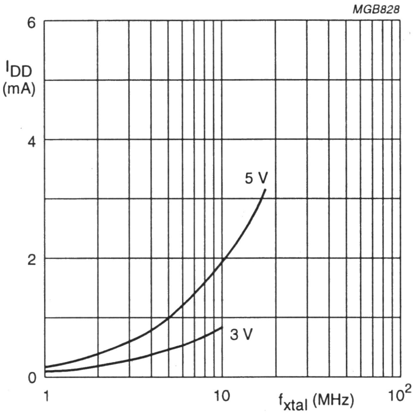


Fig.7 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



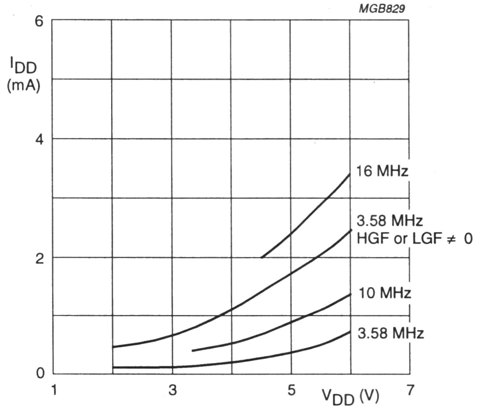
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



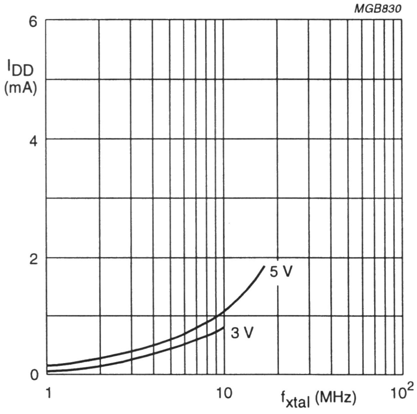
Measured with function generator on XTAL1.

Fig.9 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



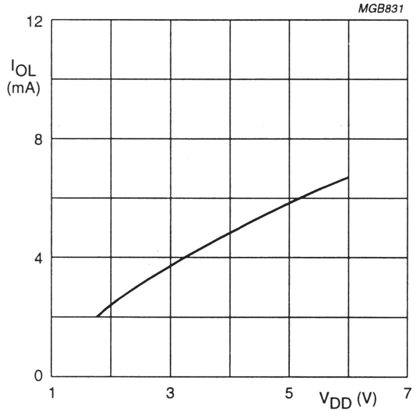
Measured with crystal between XTAL1 and XTAL2.

Fig.10 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.11 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V.

Fig.12 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

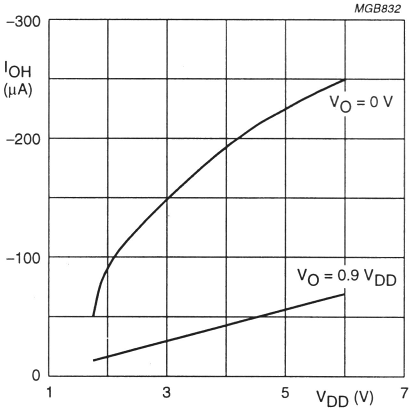
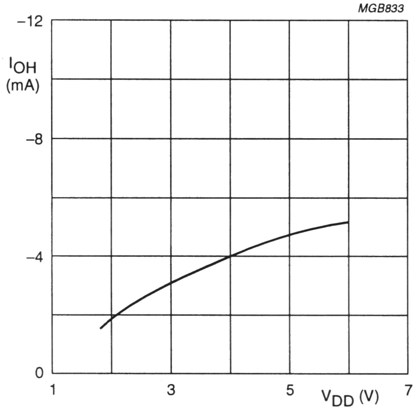


Fig.13 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.14 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

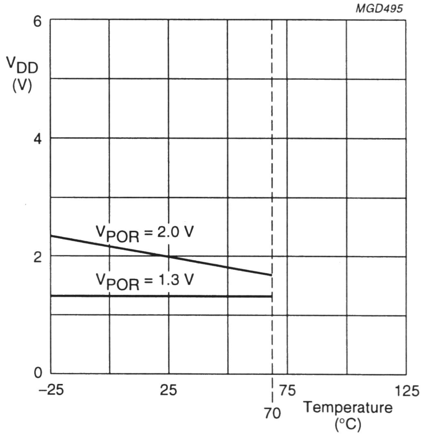


Fig.15 Typical Power-on-reset level (V_{POR}) as function of temperature.

19 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA335xC) or −25 to +70 °C (PCD335xA); all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.16	1	–	16	MHz
Oscillator (see Fig.17)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

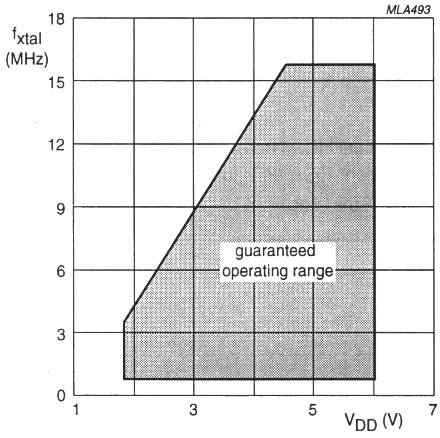


Fig.16 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

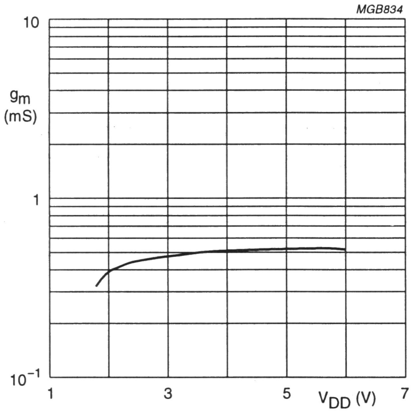


Fig.17 Typical transconductance as a function of supply voltage (V_{DD}).

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FREQUENCY GENERATOR
6.1 Frequency generator derivative registers
6.2 Melody output (P1.7/MDY)
6.3 DTMF clock divider and output (DP1.7/DCO)
6.4 Frequency registers
6.5 DTMF frequencies
6.6 Modem frequencies
6.7 Musical scale frequencies
7 EEPROM AND TIMER 2 ORGANIZATION
7.1 EEPROM registers
7.2 EEPROM latches
7.3 EEPROM flags
7.4 EEPROM macros
7.5 EEPROM access
7.6 Timer 2
8 DERIVATIVE INTERRUPTS
9 TIMING
10 RESET
11 IDLE MODE
12 STOP MODE
13 SUMMARY OF I/O PORTS AND MASK OPTIONS
14 SUMMARY OF DERIVATIVE REGISTERS
15 LIMITING VALUES
16 HANDLING
17 DC CHARACTERISTICS
18 AC CHARACTERISTICS
19 PACKAGE OUTLINES
20 SOLDERING
20.1 Introduction
20.2 Reflow soldering
20.3 Wave soldering
20.4 Repairing soldered joints
21 DEFINITIONS
22 LIFE SUPPORT APPLICATIONS

8-bit microcontrollers with DTMF generator and 256 bytes EEPROM

PCA3354C; PCD3354A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; all in a 44-lead quad flat package
- 8 kbytes ROM; 256 bytes RAM
- 256 bytes Electrically Erasable Programmable Read Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 36 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU clock frequency: 1 to 16 MHz (3.58 MHz or 10.74 MHz for DTMF)
- Operating temperature:
  - −25 to 70 °C (PCD3354A)
  - 0 to 50 °C (PCA3354C)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCA3354C and PCD3354A are microcontrollers oriented towards telephony applications. They include 8 kbytes ROM, 256 bytes RAM, 36 I/O lines, and an on-chip dual tone multifrequency (DTMF) generator.
In addition to dialling, the generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation.

The PCA3354C and PCD3354A also incorporate 256 bytes of EEPROM, permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family. This data sheet details the specific properties of the PCA3354C and PCD3354A.
The shared characteristics of the PCD33xxA family of microcontrollers are described in the:

> *"PCD33xxA Family"* data sheet or
>
> *"Data Handbook IC03; Section PCD33xxA Family"*,

which should be read in conjunction with this publication.

Differences between PCA3354C and PCD3354A are shown in Table 1.

Table 1 Differences: PCA3354C and PCD3354A

TYPE	V_{POR}	TEMP. RANGE
PCA3354C	fixed at 2.0 V ±0.3 V	0 to 50 °C
PCD3354A	(1.2 to 3.6 V) ±0.5 V(1)	−25 to 70 °C

Note

1. See Chapter 13, Table 25.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA3354CH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1
PCD3354AH			

4 BLOCK DIAGRAM

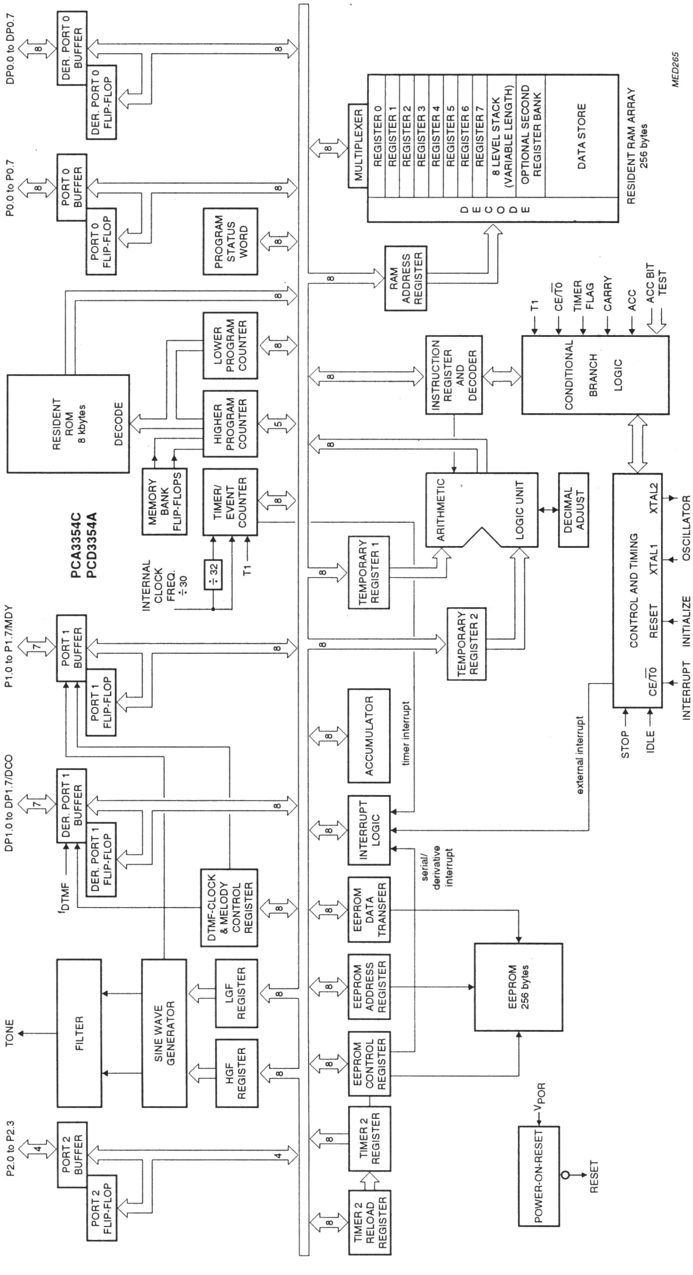

DP0.0 to DP0.7
DER. PORT 0 BUFFER
DER. PORT 0 FLIP-FLOP
P0.0 to P0.7
PORT 0 BUFFER
PORT 0 FLIP-FLOP
PROGRAM STATUS WORD
LOWER PROGRAM COUNTER
HIGHER PROGRAM COUNTER
RESIDENT ROM 8 kbytes
DECODE
MEMORY BANK FLIP-FLOPS
TIMER/ EVENT COUNTER
PCA3354C
PCD3354A
INTERNAL CLOCK FREQ. ÷ 30
÷ 32
T1
P1.0 to P1.7/MDY
PORT 1 BUFFER
PORT 1 FLIP-FLOP
DP1.0 to DP1.7/DCO
DER. PORT 1 BUFFER
DER. PORT 1 FLIP-FLOP
f_{DTMF}
DTMF-CLOCK & MELODY CONTROL REGISTER
TONE
FILTER
SINE WAVE GENERATOR
LGF REGISTER
HGF REGISTER
P2.0 to P2.3
PORT 2 BUFFER
PORT 2 FLIP-FLOP
8
7
5
4
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
DECODE
RESIDENT RAM ARRAY 256 bytes
MED265
RAM ADDRESS REGISTER
INSTRUCTION REGISTER AND DECODER
CONDITIONAL BRANCH LOGIC
T1
CE/$\overline{T0}$
TIMER FLAG
CARRY
ACC
ACC BIT TEST
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
TEMPORARY REGISTER 1
TEMPORARY REGISTER 2
CONTROL AND TIMING
XTAL2
XTAL1
RESET
CE/$\overline{T0}$
OSCILLATOR
INITIALIZE
INTERRUPT
STOP
IDLE
external interrupt
timer interrupt
ACCUMULATOR
INTERRUPT LOGIC
serial/ derivative interrupt
EEPROM DATA TRANSFER
EEPROM ADDRESS REGISTER
EEPROM CONTROL REGISTER
EEPROM 256 bytes
TIMER 2 REGISTER
TIMER 2 RELOAD REGISTER
POWER-ON-RESET
V_{POR}
RESET

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

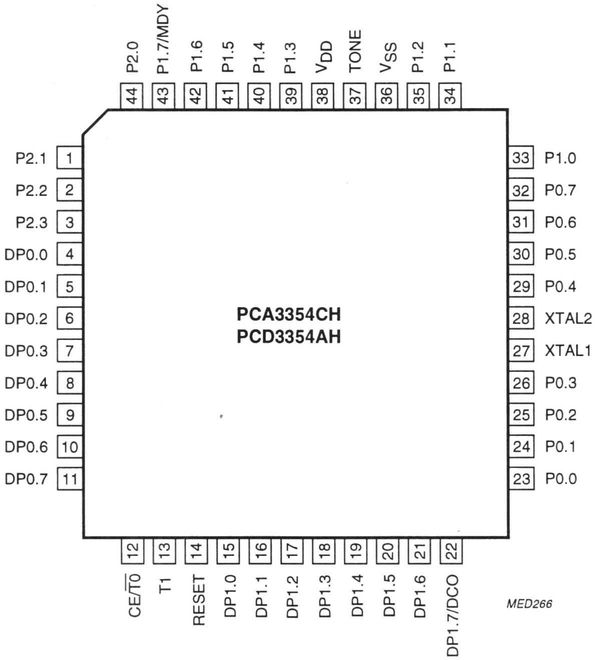

P2.0
P1.7/MDY
P1.6
P1.5
P1.4
P1.3
V_DD
TONE
V_SS
P1.2
P1.1
44
43
42
41
40
39
38
37
36
35
34
P2.1 1
P2.2 2
P2.3 3
DP0.0 4
DP0.1 5
DP0.2 6
DP0.3 7
DP0.4 8
DP0.5 9
DP0.6 10
DP0.7 11
33 P1.0
32 P0.7
31 P0.6
30 P0.5
29 P0.4
28 XTAL2
27 XTAL1
26 P0.3
25 P0.2
24 P0.1
23 P0.0
PCA3354CH
PCD3354AH
12 CE/T̅0̅
13 T1
14 RESET
15 DP1.0
16 DP1.1
17 DP1.2
18 DP1.3
19 DP1.4
20 DP1.5
21 DP1.6
22 DP1.7/DCO
MED266

Fig.2 Pin configuration (SOT205-1).

5.2 Pin description

Table 2 SOT205-1 package (for information on parallel I/O ports, see Chapter 13)

SYMBOL	PIN	DESCRIPTION
P2.0 to P2.3	44, 1 to 3	Port 2: 4 quasi-bidirectional I/O lines
DP0.0 to DP0.7	4 to 11	Derivative Port 0: 8 quasi-bidirectional I/O lines
CE/$\overline{\text{T0}}$	12	Chip Enable or Test 0
T1	13	Test 1/count input of 8-bit Timer/event counter 1
RESET	14	reset input
DP1.0 to DP1.6	15 to 21	Derivative Port 1: 7 quasi-bidirectional I/O lines
DP1.7/DCO	22	Derivative Port 1: quasi-bidirectional I/O line or DTMF clock output
P0.0 to P0.7	23 to 26, 29 to 32	Port 0: 8 quasi-bidirectional I/O lines
XTAL1	27	crystal oscillator/external clock input
XTAL2	28	crystal oscillator output
P1.0 to P1.6	33 to 35, 39 to 42	Port 1: 7 quasi-bidirectional I/O lines
V_{SS}	36	ground
TONE	37	DTMF output
V_{DD}	38	positive supply voltage
P1.7/MDY	43	Port 1: quasi-bidirectional I/O line or melody output

6 FREQUENCY GENERATOR

A versatile frequency generator section with built-in programmable clock divider is provided (see Fig.3).
The clock divider allows the DTMF section to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = \frac{1}{3} \times f_{xtal}$) depending on the state of the divider control bit DIV3 (see Table 5). The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available. Their frequencies are provided either in purely sinusoidal form on the TONE output or as a square wave on the port line P1.7/MDY. The latter is typically for ringer applications in telephone sets. In case no tones are generated the TONE output is in tri-state mode.

6.1 Frequency generator derivative registers

6.1.1 HIGH AND LOW GROUP FREQUENCY REGISTERS

Table 3 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers HGF (High Group Frequency) and LGF (Low Group Frequency); access type W.

Table 3 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
11H	HGF	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 CLOCK AND MELODY CONTROL REGISTER (MDYCON; access type R/W)

Table 4 Clock and Melody Control Register (address 13H)

7	6	5	4	3	2	1	0
0	0	0	0	0	EDCO	DIV3	EMO

Table 5 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 3	–	These bits are set to a logic 0.
2	EDCO	Enable DTMF clock output. If bit EDCO = 0, then DP1.7/DCO is a general purpose derivative port line. If bit EDCO = 1, then DP1.7/DCO is the DTMF clock output. EDCO = 1 does not inhibit the port instructions for DP1.7/DCO. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of DP1.7/DCO must remain set to avoid conflicts between DTMF clock and port outputs.
1	DIV3	Enable DTMF clock divider. If bit DIV3 = 0, then the DTMF clock $f_{DTMF} = f_{xtal}$. If bit DIV3 = 1, then $f_{DTMF} = \frac{1}{3} \times f_{xtal}$.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the HIGH state.

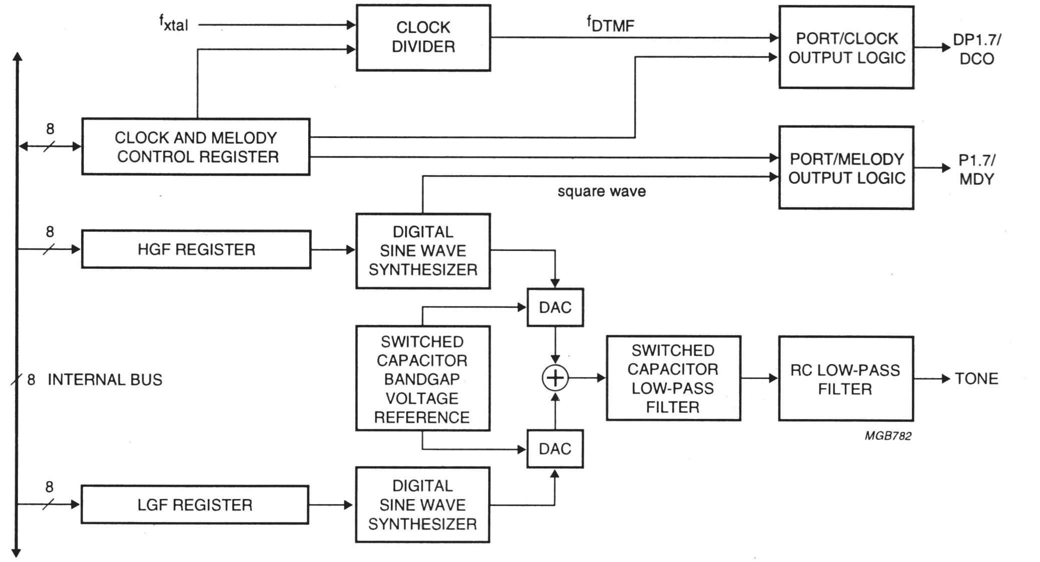

f_{xtal}
CLOCK DIVIDER
f_{DTMF}
PORT/CLOCK OUTPUT LOGIC
DP1.7/ DCO
8
CLOCK AND MELODY CONTROL REGISTER
PORT/MELODY OUTPUT LOGIC
P1.7/ MDY
square wave
8
HGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER
DAC
SWITCHED CAPACITOR BANDGAP VOLTAGE REFERENCE
8 INTERNAL BUS
SWITCHED CAPACITOR LOW-PASS FILTER
RC LOW-PASS FILTER
TONE
MGB782
DAC
8
LGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER

Fig.3 Block diagram of the frequency generator, melody output (P1.7/MDY) and DTMF clock output (DP1.7/DCO).

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the limitation $60 \leq x \leq 255$ is relaxed to $2 \leq x \leq 255$ in this application; x = decimal value of the HGF register contents. Due to the low-pass filters, the simultaneous signal on the TONE output is not useful for $x < 60$.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set high before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 13, Table 24.

6.3 DTMF clock divider and output (DP1.7/DCO)

The DTMF clock divider allows the DTMF part to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = ^1/_3 \times f_{xtal}$) depending on the state of the divider control bit DIV3 in register MDYCON.

For low power applications, a 3.58 MHz quartz crystal or PXE resonator can be chosen together with the divide-by-one function of the clock divider.

For applications a 10.74 MHz quartz crystal or PXE resonator may be chosen together with the divide-by-three function of the clock divider. This triples the program speed of the microcontroller, thereby keeping the assumed DTMF frequency of 3.58 MHz.

Since a 3.58 MHz clock is needed for peripheral telephony circuits such as the analog voice scrambler/descrambler PCD4440, a switchable DTMF clock output is provided depending on the state of the enable clock output bit EDCO in register MDYCON.

If EDCO = 1 and DIV3 = 1 in the MDYCON register: a square wave with the frequency $f_{DTMF} = ^1/_3 \times f_{xtal}$ is output on the derivative port line DP1.7/DCO. If EDCO = 1 and DIV3 = 0: a square wave with the frequency $f_{DTMF} = f_{xtal}$ is output on the derivative port line DP1.7/DCO.

The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 13, Table 24.

6.4 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the Low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value ‘x’ held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23(x+2)]}; \text{ where } 60 \le x \le 255.$$

The frequency limitation given by $x \ge 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.5 DTMF frequencies

Assuming a oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 6.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 7.

Table 6 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 7 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.6 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 8 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low group frequency generation.

Table 8 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980(1)	978.82	−0.12	−1.18
82	1180(1)	1179.03	−0.08	−0.97
8F	1070(2)	1073.33	0.31	3.33
79	1270(2)	1265.30	−0.37	−4.70
80	1200(3)	1197.17	−0.24	−2.83
45	2200(3)	2192.01	−0.36	−7.99
76	1300(4)	1296.94	−0.24	−3.06
48	2100(4)	2103.14	0.15	3.14
5C	1650(1)	1655.66	0.34	5.66
52	1850(1)	1852.77	0.15	2.77
4B	2025(2)	2021.20	−0.19	−3.80
44	2225(2)	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.7 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 9). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low group frequency generation.

Table 9 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD(1)	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCA3354C; PCD3354A has 256 bytes of Electrically Erasable Programmable Read Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCA3354C; PCD3354A.

First, the EEPROM array is structured into 64 four-byte pages (see Fig.4) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes.

Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

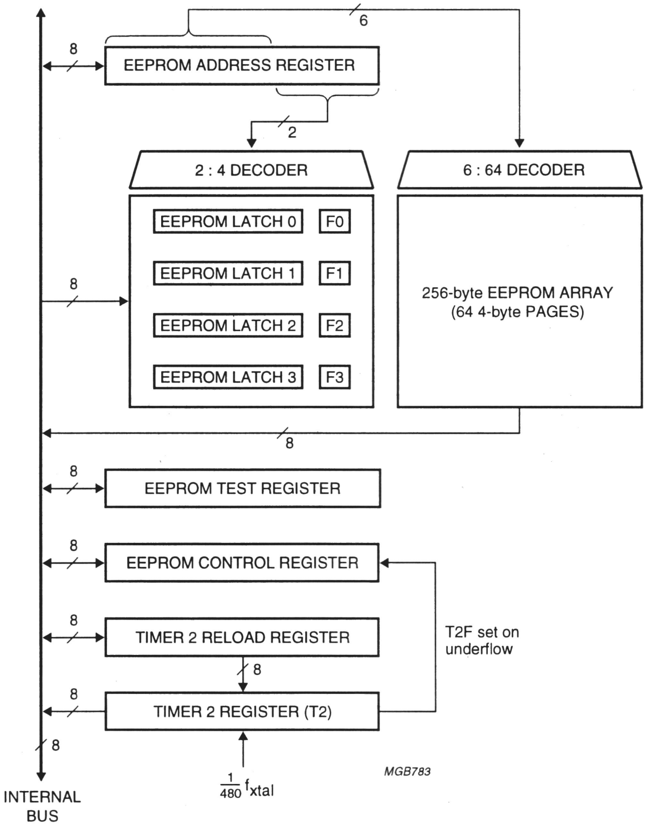

6
8
EEPROM ADDRESS REGISTER
2
2 : 4 DECODER
6 : 64 DECODER
EEPROM LATCH 0
F0
EEPROM LATCH 1
F1
EEPROM LATCH 2
F2
EEPROM LATCH 3
F3
8
256-byte EEPROM ARRAY
(64 4-byte PAGES)
8
8
EEPROM TEST REGISTER
8
EEPROM CONTROL REGISTER
8
TIMER 2 RELOAD REGISTER
T2F set on underflow
8
8
TIMER 2 REGISTER (T2)
8
INTERNAL BUS
$\frac{1}{480} f_{xtal}$
MGB783

Fig.4 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. The register access type is R/W.

Table 10 EEPROM Control Register (address 04H)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 11 Description of the EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 12.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 12 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed. The register access type is R/W.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 13 EEPROM Address Register (address 01H)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 14 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 12) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 15 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 16 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.4) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.4) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.4) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 23). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 10.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 13), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.4) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM latches 0 to 3 (Fig.4) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect.

Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 17).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 12) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 18.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 17 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 18 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 19 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 20.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of ‘write page’.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 20 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	‘write page’ control word
MOV EPCR, A	start ‘write page’ cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of ‘erase/write page’.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 21 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	‘erase/write page’ control word
MOV EPCR, A	start ‘erase/write page’ cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 22 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $^1/_{480} \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $^1/_{480} \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 23 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 23 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE(1) (HEX)
1	0A
2	14
3.58	25
6	3E
10.74	6F
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times {}^1/_{480} \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer 2 Register T2 (see Table 26) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 10 and 11).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds.
- No external interrupt request is pending.
- The derivative interrupt is enabled.
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

9 TIMING

Although the PCA3354C; PCD3354A operates over a clock frequency range from 1 MHz to 16 MHz, f_{xtal} = 3.58 MHz or 10.74 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33xxA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{\text{T0}}$, Timer 2 proceeds from the held state.

13 SUMMARY OF I/O PORTS AND MASK OPTIONS

All standard quasi-bidirectional I/O ports are available; see *"PCD33xxA Family"* data sheet.

- Port 0: 8 parallel port lines P0.0 to P0.7
- Port 1: 8 parallel port lines P1.0 to P1.7
- Port 2: 4 parallel port lines P2.0 to P2.3.

In addition to the standard ports, 2 derivative I/O ports are available:

- Derivative Port 0: 8 parallel port lines DP0.0 to DP0.7 (register DP0I)
- Derivative Port 1: 8 parallel port lines DP1.0 to DP1.7 (register DP1I).

See Table 26 for the addresses of DP0I and DP1I.

Table 24 Port mask options

PORT NAME	PORT OUTPUT DRIVE(1)			PORT STATE AFTER RESET	
	OPTION 1	OPTION 2	OPTION 3	SET (H)	RESET (L)
P0.0 to P0.7	X	X	X	X	X
P1.0 to P1.6	X	X	X	X	X
P1.7/MDY(2)	X	X	X	X	X
P2.0 to P2.3	X	X	X	X	X
DP0.0 to DP0.7	X	X	X	X	X
DP1.0 to DP1.6	X	X	X	X	X
DP1.7/DCO(3)	X	X	X	X	X

Notes

1. Port output drive (see *"PCD33xxA Family"* data sheet):
    a) Option 1: standard I/O.
    b) Option 2: open-drain I/O.
    c) Option 3: push-pull output.
2. If Option 1 or 3 is chosen, the melody output becomes a push-pull output; if Option 2 is chosen, the melody output becomes an open-drain output.
3. If Option 1 or 3 is chosen, the DTMF clock output becomes a push-pull output; if Option 2 is chosen, the DTMF clock output becomes an open-drain output.

Table 25 Mask options

FEATURE	DESCRIPTION
ROM Code: program/data	Any mix of instructions and data up to ROM size of 8 kbytes
Power-on-reset voltage level: V_{POR} PCD3354A	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

14 SUMMARY OF DERIVATIVE REGISTERS

Table 26 Register map

ADDR. (HEX)	REGISTER	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**R/W**
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Clock and Melody Control Register (MDYCON)	0	0	0	0	0	DCO	DIV3	EMO	R/W
14 to 2F	not used									
30	Derivative Port 0 lines (DP0I)	D0.7	D0.6	D0.5	D0.4	D0.3	D0.2	D0.1	D0.0	R
31	Derivative Port 1 lines (DP1I)	D1.7	D1.6	D1.5	D1.4	D1.3	D1.2	D1.1	D1.0	R
32	Derivative Port 0 flip-flop (DP0FF)	F0.7	F0.6	F0.5	F0.4	F0.3	F0.2	F0.1	F0.0	R/W
33	Derivative Port 1 flip-flop (DP1FF)	F1.7	F1.6	F1.5	F1.4	F1.3	F1.2	F1.1	F1.0	R/W
34 to FF	not used									

15 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

16 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

17 DC CHARACTERISTICS

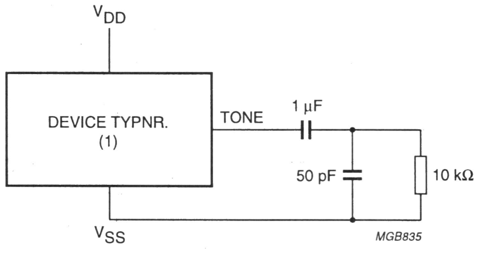
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA3354C) or −25 to +70 °C (PCD3354A); all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL})

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 6, 7 and 8)						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V; value HGF = LGF = 0	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF ≠ LGF ≠ 0; DIV3 = 1	–	2.7	6.2	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.7	4.2	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	3.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(ID)}$	supply current Idle mode; note 2	$V_{DD} = 3$ V; value HGF $\neq 0$ and/or LGF $\neq 0$	–	0.7	1.4	mA
		$V_{DD} = 3$ V; value HGF = LGF =0	–	0.25	0.5	mA
		$V_{DD} = 5$ V; $f_{xtal} = 10.74$ MHz (g_{mM}); value HGF $\neq$ LGF $\neq 0$; DIV3 = 1	–	2.3	5.5	mA
		$V_{DD} = 5$ V; $f_{xtal} = 10.74$ MHz (g_{mM}); value HGF = LGF = 0	–	1.3	3.5	mA
		$V_{DD} = 5$ V; $f_{xtal} = 16$ MHz (g_{mH}); value HGF = LGF = 0	–	2.4	–	mA
$I_{DD(ST)}$	supply current Stop mode; notes 2 and 3	$V_{DD} = 1.8$ V; $T_{amb} = 25$ °C	–	1.0	5.5	μA
		$V_{DD} = 1.8$ V; $T_{amb} = -25$ to 70 °C	–	–	10	μA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	μA
Port outputs (see Figs 10, 11 and 12)						
I_{OL}	LOW level port sink current	$V_{DD} = 3$ V; $V_O = 0.4$ V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	$V_{DD} = 3$ V; $V_O = 2.7$ V	–10	–30	–	μA
		$V_{DD} = 3$ V; $V_O = 0$ V	–	–140	–300	μA
I_{OH}	HIGH level port push-pull source current	$V_{DD} = 3$ V; $V_O = 2.6$ V	–0.7	–3.5	–	mA
TONE output (see Fig.5; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	$T_{amb} = 25$ °C; note 5	–	–25	–	dB
EEPROM (notes 1 and 6)						
n_{cyc}	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention		10	–	–	years
Power-on-reset						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 8; for PCD3354A	–0.5	0	+0.5	V
V_{POR}	Power-on-reset level	for PCA3354C	1.7[9]	2.0	2.3	V

Notes to the DC characteristics

1. TONE output; EEPROM erase and write require $V_{DD} \geq 2.5$ V:
    a) TONE output requires $f_{xtal} < 4$ MHz in case DIV3 = 0.
    b) TONE output requires $f_{xtal} < 12$ MHz in case DIV3 = 1.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open:
    a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
    b) Typical values: 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/$\overline{\text{T0}}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; open-drain outputs connected to V_{SS}; all other outputs open.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is typically logic 1.
7. Verified on sampling basis.
8. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.
9. Each device is tested on the condition: $V_{DD(min)} < V_{POR}$; to ensure a correct start-up, even for slow rising supply voltages.



(1) Device typenr.: PCA3354C or PCD3354A.

Fig.5 TONE output test circuit.

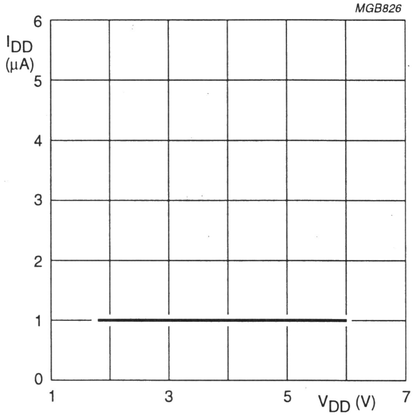
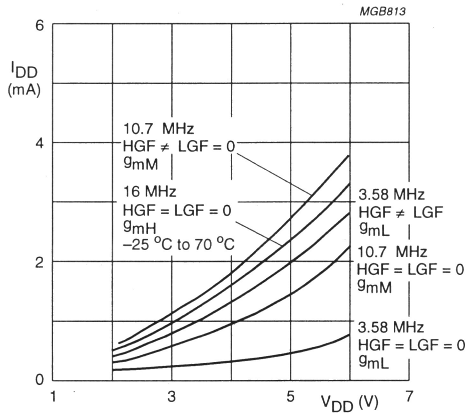
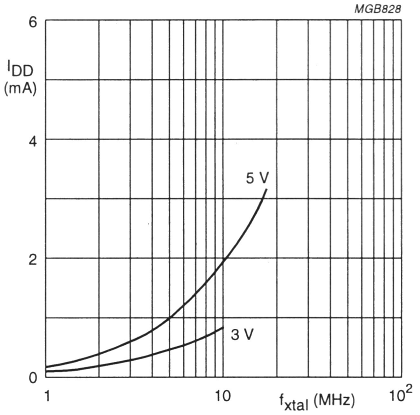


Fig.6 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



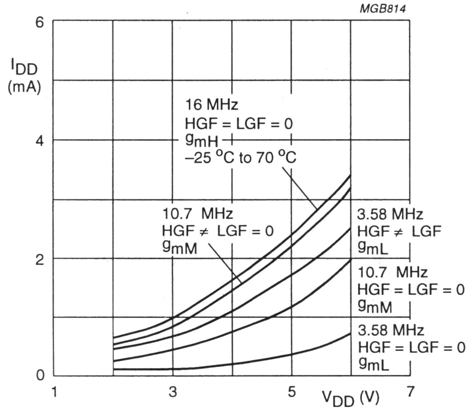
Measured with crystal between XTAL1 and XTAL2.

Fig.7 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



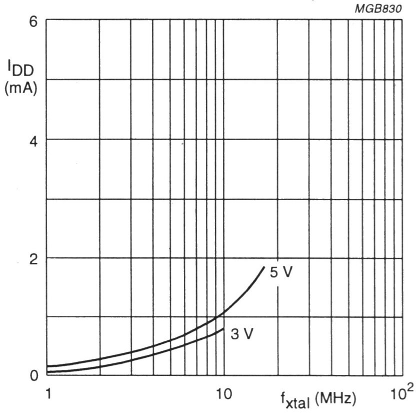
Measured with function generator on XTAL1.

Fig.8 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



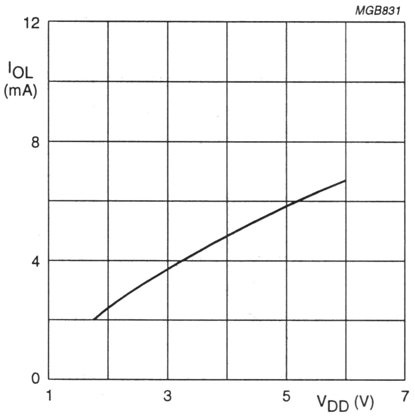
Measured with crystal between XTAL1 and XTAL2.

Fig.9 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.10 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V.

Fig.11 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

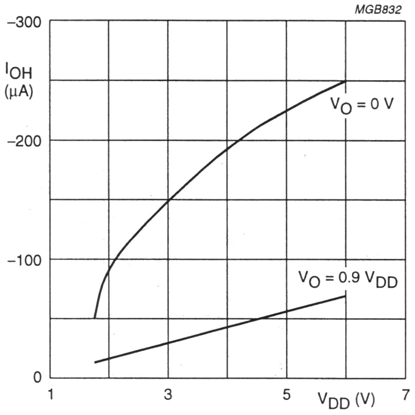
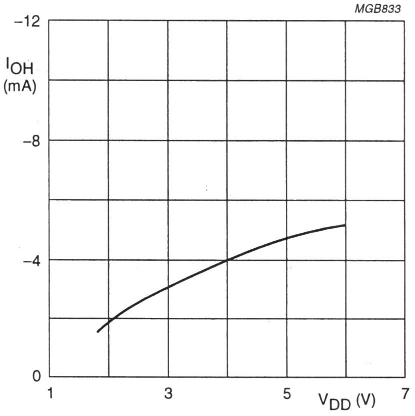


Fig.12 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.13 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

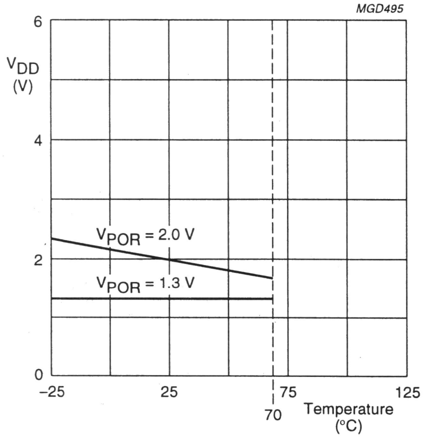


Fig.14 Typical Power-on-reset level (V_{POR}) as function of temperature.

18 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA3354C) or –25 to +70 °C (PCD3354A); all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.13	1	–	16	MHz
Oscillator (see Fig.14)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance		0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance		3	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

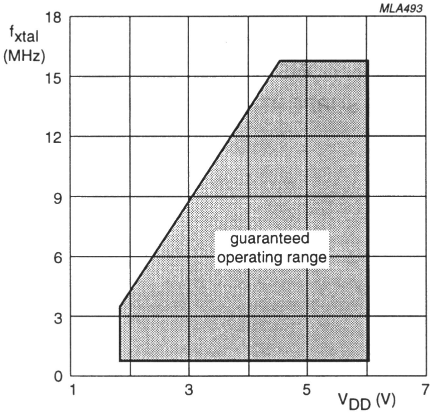


Fig.15 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

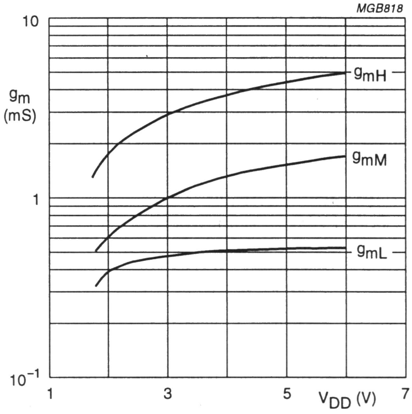


Fig.16 Typical transconductance as a function of supply voltage (V_{DD}).

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FREQUENCY GENERATOR
6.1 Frequency generator derivative registers
6.2 Melody output (P1.7/MDY)
6.3 Frequency registers
6.4 DTMF frequencies
6.5 Modem frequencies
6.6 Musical scale frequencies
7 EEPROM AND TIMER 2 ORGANIZATION
7.1 EEPROM registers
7.2 EEPROM latches
7.3 EEPROM flags
7.4 EEPROM macros
7.5 EEPROM access
7.6 Timer 2
8 INTERRUPTS
8.1 Derivative interrupt
8.2 Port 0 Wake-up interrupts
9 TIMING
10 RESET
11 IDLE MODE
12 STOP MODE
13 INSTRUCTION SET RESTRICTIONS
14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATION
15 SUMMARY OF DERIVATIVE REGISTERS
16 LIMITING VALUES
17 HANDLING
18 DC CHARACTERISTICS
19 AC CHARACTERISTICS
20 PACKAGE OUTLINES
21 SOLDERING
21.1 Reflow soldering
21.2 Wave soldering
21.3 DIP
21.4 Repairing soldered joints
22 DEFINITIONS
23 LIFE SUPPORT APPLICATIONS

8-bit microcontrollers with DTMF generator and 128 bytes EEPROM

PCD3356A; PCD3357A; PCD3359A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; in a single 28-lead or 32-lead package
- ROM:
  - 8 kbytes (PCD3356A)
  - 6 kbytes (PCD3357A)
  - 2 kbytes (PCD3359A)
- RAM:
  - 128 bytes (PCD3356A and PCD3357A)
  - 64 bytes (PCD3359A)
- 128 bytes EEPROM
- OTP version available.
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- 3 single-level vectored interrupts:
  - external
  - Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Wake-up via external or Port 0 interrupt
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating temperature: –25 to 70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3356A, PCD3357A and PCD3359A are low voltage microcontrollers oriented towards telephony applications. They include an on-chip dual tone multifrequency (DTMF) generator. In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation (in which case the TONE output is disabled).
A wake-up function via Port 0 interrupt facilitates keyboard interfacing. The PCD3356A, PCD3357A and PCD3359A can be emulated with the OTP microcontroller PCD3756A.

The PCD3359A also incorporate 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family. This data sheet details the specific properties of the PCD3356A, PCD3357A and PCD3359A.
The shared characteristics of the PCD33XXA family of microcontrollers are described in the

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER[(1)]	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD335xAP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD335xAT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD335xAH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

Note

1. 'x' denotes 6, 7 or 9.

4 BLOCK DIAGRAM

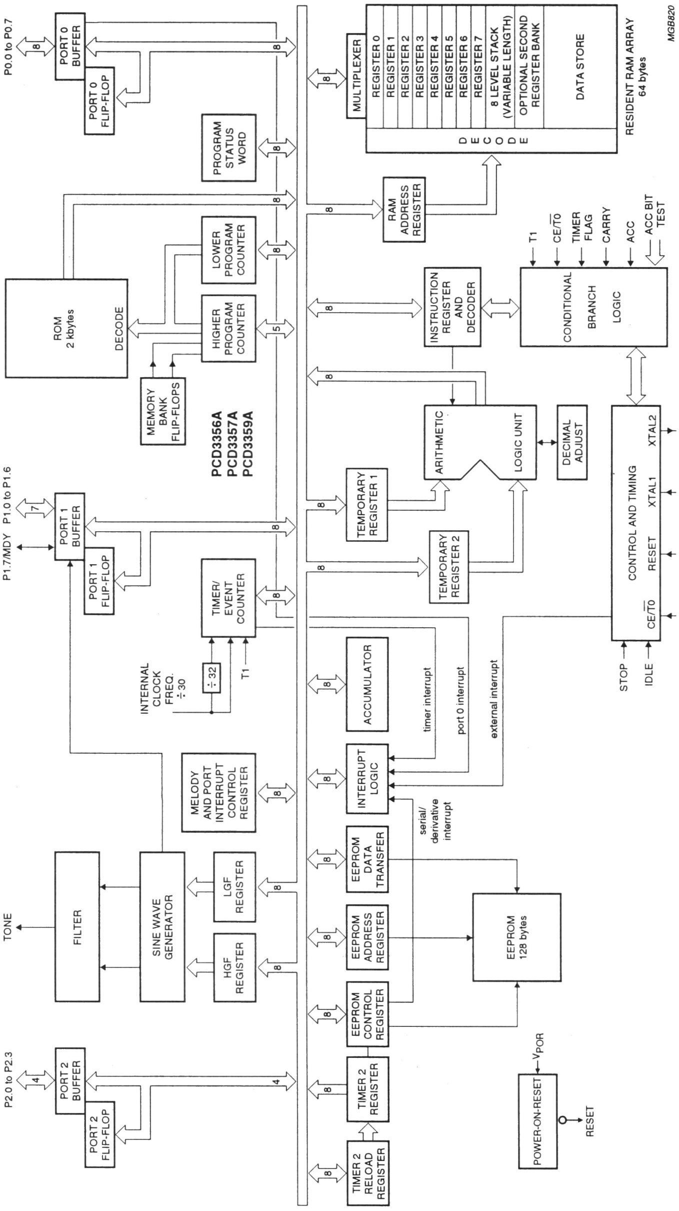

P0.0 to P0.7
8
PORT 0 BUFFER
PORT 0 FLIP-FLOP
PROGRAM STATUS WORD
LOWER PROGRAM COUNTER
HIGHER PROGRAM COUNTER
ROM 2 kbytes
DECODE
MEMORY BANK FLIP-FLOPS
PCD3356A
PCD3357A
PCD3359A
P1.7/MDY
P1.0 to P1.6
7
PORT 1 BUFFER
PORT 1 FLIP-FLOP
TIMER/ EVENT COUNTER
INTERNAL CLOCK FREQ. ÷ 30
÷ 32
T1
MELODY AND PORT INTERRUPT CONTROL REGISTER
TONE
FILTER
SINE WAVE GENERATOR
LGF REGISTER
HGF REGISTER
P2.0 to P2.3
4
PORT 2 BUFFER
PORT 2 FLIP-FLOP
8
5
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
DECODE
RESIDENT RAM ARRAY 64 bytes
MGB820
RAM ADDRESS REGISTER
T1
CE/$\overline{T0}$
TIMER FLAG
CARRY
ACC
ACC BIT TEST
INSTRUCTION REGISTER AND DECODER
CONDITIONAL BRANCH LOGIC
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
TEMPORARY REGISTER 1
TEMPORARY REGISTER 2
CONTROL AND TIMING
XTAL2
XTAL1
OSCILLATOR
RESET
INITIALIZE
CE/$\overline{T0}$
INTERRUPT
STOP
IDLE
ACCUMULATOR
timer interrupt
port 0 interrupt
external interrupt
INTERRUPT LOGIC
serial/ derivative interrupt
EEPROM DATA TRANSFER
EEPROM ADDRESS REGISTER
EEPROM CONTROL REGISTER
EEPROM 128 bytes
TIMER 2 REGISTER
TIMER 2 RELOAD REGISTER
POWER-ON-RESET
V_{POR}
RESET

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

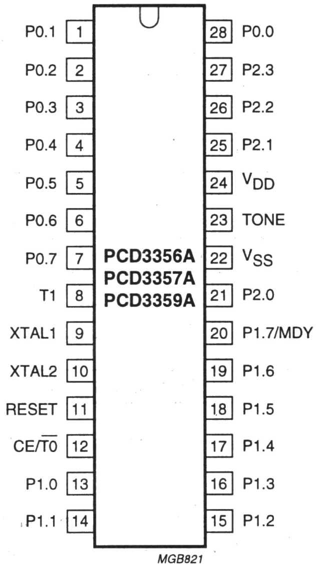

P0.1 1
P0.2 2
P0.3 3
P0.4 4
P0.5 5
P0.6 6
P0.7 7
T1 8
XTAL1 9
XTAL2 10
RESET 11
CE/$\overline{T0}$ 12
P1.0 13
P1.1 14
28 P0.0
27 P2.3
26 P2.2
25 P2.1
24 V_{DD}
23 TONE
22 V_{SS}
21 P2.0
20 P1.7/MDY
19 P1.6
18 P1.5
17 P1.4
16 P1.3
15 P1.2
PCD3356A
PCD3357A
PCD3359A
MGB821

Fig.2 Pin configuration (SOT117-1 and SOT136-1).

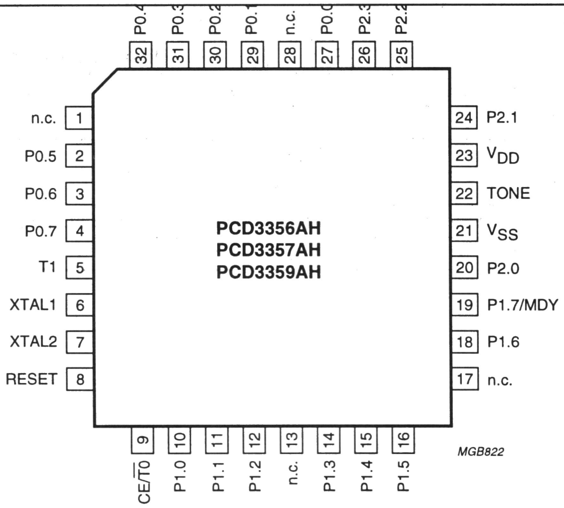

P0.4 32
P0.3 31
P0.2 30
P0.1 29
n.c. 28
P0.0 27
P2.3 26
P2.2 25
n.c. 1
P0.5 2
P0.6 3
P0.7 4
T1 5
XTAL1 6
XTAL2 7
RESET 8
24 P2.1
23 V_{DD}
22 TONE
21 V_{SS}
20 P2.0
19 P1.7/MDY
18 P1.6
17 n.c.
9 CE/$\overline{T0}$
10 P1.0
11 P1.1
12 P1.2
13 n.c.
14 P1.3
15 P1.4
16 P1.5
PCD3356AH
PCD3357AH
PCD3359AH
MGB822

Fig.3 Pin configuration (SOT358-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines or wake-up interrupts
T1	8	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{\text{T0}}$	12	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	20	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	21, 25 to 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

Table 2 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
T1	5	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	crystal oscillator or external clock input
XTAL2	7	crystal oscillator output
RESET	8	reset input
CE/$\overline{\text{T0}}$	9	Chip Enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	19	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	20, 24 to 26	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	21	ground
TONE	22	DTMF output
V_{DD}	23	positive supply voltage
P0.0 to P0.7	27, 29 to 32, 2 to 4	Port 0: 8 quasi-bidirectional I/O lines or wake-up interrupts
n.c.	1, 13, 17, 28	not connected

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the P1.7/MDY output.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

In case no tones are generated, or the melody function is used, the TONE output is in tri-state mode.

6.1 Frequency generator derivative registers

6.1.1 HIGH AND LOW GROUP FREQUENCY REGISTERS

Table 3 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers HGF (High Group Frequency) and LGF (Low Group Frequency); access type W.

Table 3 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
11H	HGF	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 MELODY AND PORT INTERRUPT CONTROL REGISTER (MDYCON)

The Melody and Port Interrupt Control Register has two functions: bit 0 defines the behaviour of the melody output; bits 4 to 7 individually enable/disable specific pairs of Port 0 interrupts. MDYCON is a R/W register.

Table 4 Melody and Port Interrupt Control Register (address 13H)

7	6	5	4	3	2	1	0
EPI3	EPI2	EPI1	EPI0	0	0	0	EMO

Table 5 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 4	EPI3 to EPI0	Enable Port 0 interrupts. Bits 7 to 4 individually enable/disable specific pairs of Port 0 interrupts; see Table 6 and Section 8.2 for details.
3 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line and the TONE output is enabled. If bit EMO = 1, then P1.7/MDY is the melody output and the TONE output is disabled (tri-state). EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

Table 6 Port 0 Interrupts control bits

BIT	STATE	INTERRUPTS			
		P0.0 AND P0.1	**P0.2 AND P0.3**	**P0.4 AND P0.5**	**P0.6 AND P0.7**
EPI0	1	enabled	–	–	–
	0	disabled	–	–	–
EPI0	1	–	enabled	–	–
	0	–	disabled	–	–
EPI0	1	–	–	enabled	–
	0	–	–	disabled	–
EPI0	1	–	–	–	enabled
	0	–	–	–	disabled

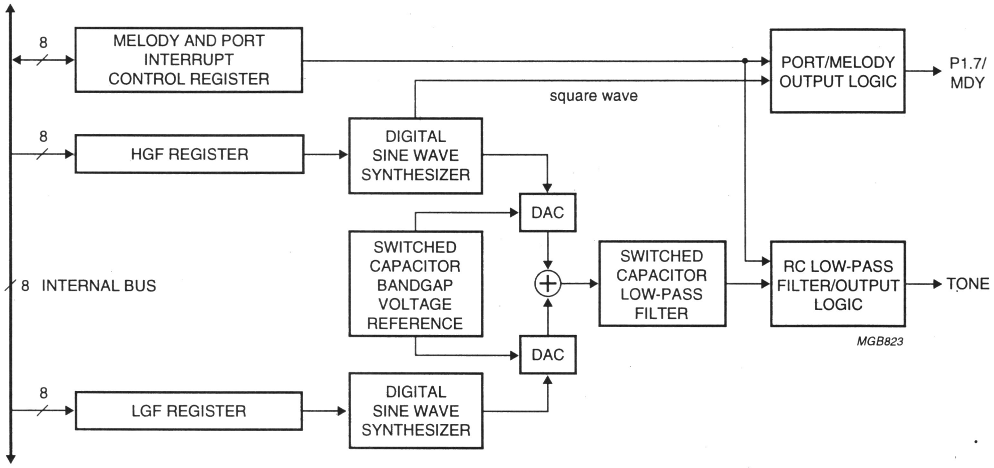

8
MELODY AND PORT INTERRUPT CONTROL REGISTER
PORT/MELODY OUTPUT LOGIC
P1.7/ MDY
square wave
8
HGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER
DAC
SWITCHED CAPACITOR BANDGAP VOLTAGE REFERENCE
8 INTERNAL BUS
SWITCHED CAPACITOR LOW-PASS FILTER
RC LOW-PASS FILTER/OUTPUT LOGIC
TONE
MGB823
DAC
8
LGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER

Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

If bit EMO = 1 in the Melody and Port Interrupt Control Register the TONE output is disabled (tri-state) and a square wave with the frequency defined by the HGF contents is output on line P1.7/MDY. The square wave (duty cycle = $^{12}\!/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the limitation $60 \leq x \leq 255$ is relaxed to $2 \leq x \leq 255$ in this application; x = decimal value of the HGF register contents. Due to the low-pass filters, the simultaneous signal on the TONE output is not useful for $x < 60$.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY; see Chapter 14, Table 25.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave. The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value ‘x’ held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x+2)\,]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 7. The relationship between telephone keyboard symbols and the frequency register contents are given in Table 8.

Table 7 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 8 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 9 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 9 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980(1)	978.82	−0.12	−1.18
82	1180(1)	1179.03	−0.08	−0.97
8F	1070(2)	1073.33	0.31	3.33
79	1270(2)	1265.30	−0.37	−4.70
80	1200(3)	1197.17	−0.24	−2.83
45	2200(3)	2192.01	−0.36	−7.99
76	1300(4)	1296.94	−0.24	−3.06
48	2100(4)	2103.14	0.15	3.14
5C	1650(1)	1655.66	0.34	5.66
52	1850(1)	1852.77	0.15	2.77
4B	2025(2)	2021.20	−0.19	−3.80
44	2225(2)	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 10). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 10 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD(1)	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3356A, PCD3357A and PCD3359A have 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCD3356A, PCD3357A and PCD3359A.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

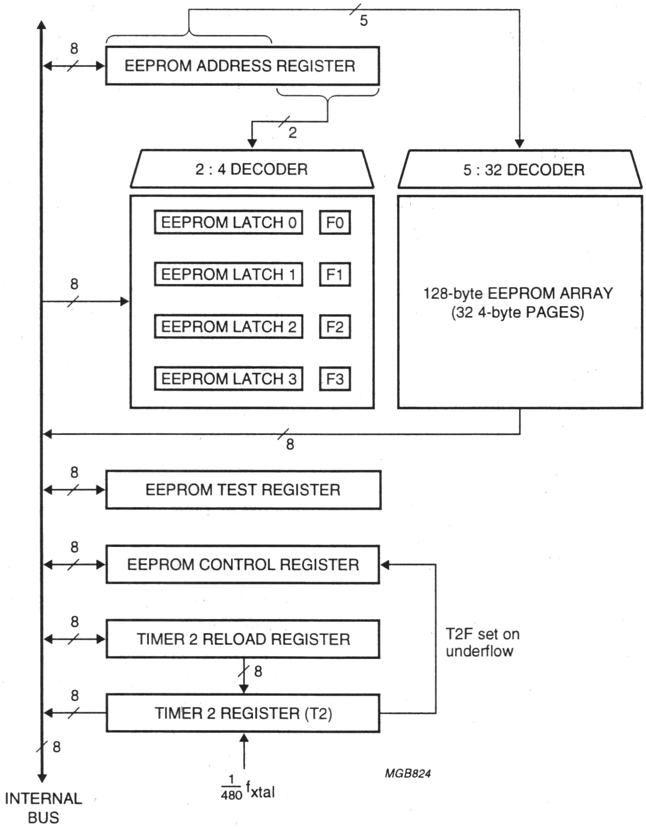

5
8
EEPROM ADDRESS REGISTER
2
2 : 4 DECODER
5 : 32 DECODER
EEPROM LATCH 0
F0
EEPROM LATCH 1
F1
EEPROM LATCH 2
F2
EEPROM LATCH 3
F3
8
128-byte EEPROM ARRAY
(32 4-byte PAGES)
8
8
EEPROM TEST REGISTER
8
EEPROM CONTROL REGISTER
8
TIMER 2 RELOAD REGISTER
T2F set on underflow
8
8
TIMER 2 REGISTER (T2)
8
INTERNAL BUS
$\frac{1}{480}$ fxtal
MGB824

Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. The register access type is R/W.

Table 11 EEPROM Control Register (address 04H)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 12 Description of EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 13.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 13 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed. The register access type is R/W.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 14 EEPROM Address Register (address 01H)

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 15 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 13) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 16 EEPROM Data Register (address 03H; access type R/W)

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	D6	D5	D4	D3	D2	D1	D0

Table 17 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 24). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 11.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 14), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 18).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 13) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 10.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 18 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 19 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 20 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 21.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of ‘write page’.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 21 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	‘write page’ control word
MOV EPCR, A	start ‘write page’ cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of ‘erase/write page’.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM latch 0 (by AD0 and AD1).
This allows efficient coding of multi-page erase/write operations.

Table 22 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	‘erase/write page’ control word
MOV EPCR, A	start ‘erase/write page’ cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 23 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $\frac{1}{480} \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $\frac{1}{480} \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 23 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 24 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times \frac{1}{480} \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 26) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 INTERRUPTS

8.1 Derivative interrupt

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 12).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

8.2 Port 0 Wake-up interrupts

In addition to the external interrupt CE, the PCD3356A; PCD3357A; PCD3359A contains 8 level-sensitive external interrupt sources on Port 0. This function generates an interrupt request if any of the enabled lines of Port 0 (P0.0 to P0.7) is pulled LOW. Like the external interrupt (and contrary to the derivative interrupt) the Port 0 interrupt operates also in Stop mode and forces the CPU to exit the Stop mode.

The Port 0 Wake-up interrupts are controlled by the Enable Port 0 Interrupt bits EPI3 to EPI0 in the Melody and Port Interrupt Control Register MDYCON. Pairs of Port 0 interrupts are individually enabled/disabled via bits 4, 5, 6 and 7. For details see Section 6.1.2. As the Port 0 interrupt is directly linked to the external interrupt, it uses the same flag (EIF), enable instructions (EN I, DIS I) and interrupt vector.

A Port 0 Wake-up interrupt is serviced if:

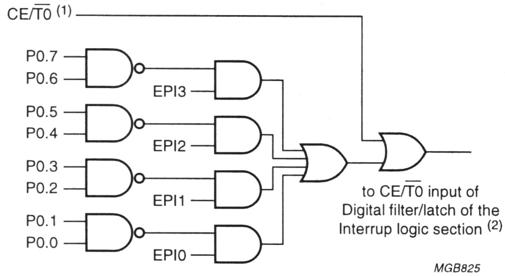
- No interrupt routine is in progress
- The external interrupt is enabled
- It's corresponding enable bit in register MDYCON is set to a logic 1.

If a Port 0 interrupt is to be used, the port flip-flop must first be set to a logic 1 (set to input mode) before it's corresponding EPIn bit is set.

If only a portion of the Port 0 interrupts are used, the remaining port lines may still be used as normal I/O.

In order to configure an I/O as an input, a logic 1 must first be written to it. If a logic 0 is written to one of these port lines (e.g. ANL P0, 00H) while it's corresponding interrupt is enabled, a Port 0 interrupt will be generated.

For more details see data sheet *"PCD33xxA Family; Section External Interrupt"*.


CE/$\overline{\text{T0}}$ (1)
P0.7
P0.6
P0.5
P0.4
P0.3
P0.2
P0.1
P0.0
EPI3
EPI2
EPI1
EPI0
to CE/$\overline{\text{T0}}$ input of Digital filter/latch of the Interrup logic section (2)
MGB825

(1) From pin CE/$\overline{\text{T0}}$.

(2) See the *"PCD33XXA Family"* data sheet.

Fig.6 Simplified External/Port 0 interrupt structure.

9 TIMING

Although the PCD3356A, PCD3357A and PCD3359A operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *“PCD33XXA Family”* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{\text{T0}}$, Timer 2 proceeds from the held state.

The Port 0 Wake-up interrupt function remains operative during Stop mode (depending only on the EPIn bits in register MDYCON). In addition to the description in the *“PCD33xxA Family”* data sheet, Stop mode may be left by a Port 0 Wake-up interrupt event (see Section 8.2).

13 INSTRUCTION SET RESTRICTIONS

- For PCD3359A only:
  - ROM space being restricted to 2 kbytes, the ‘SEL MB1/2/3’ instructions would define non-existing program memory banks and should therefore be avoided.
  - RAM space being restricted to 64 bytes, care should be taken to avoid accesses to non-existing RAM locations.
- For PCD3357A only:
  - ROM space being restricted to 6 kbytes, the ‘SEL MB2/3’ instructions would define non-existing program memory banks and should therefore be avoided.
- For the PCD3356A and PCD3357A, RAM space is restricted to 128 bytes, thus care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF PORT AND POWER-ON-RESET CONFIGURATION

All standard quasi-bidirectional I/O ports are available; see *"PCD33xxA Family"* data sheet.

- Port 0: 8 parallel port lines P0.0 to P0.7 or wake-up interrupts
- Port 1: 8 parallel port lines P1.0 to P1.7
- Port 2: 4 parallel port lines P2.0 to P2.3.

Table 25 Port and Power-on-reset configuration

See notes 1 and 2.

COVERED BY OTP	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3756A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R(3)	2S	2S	2S	2S	1.3 V

Notes

1. Port output drive: 1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* datasheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The melody output drive type is push-pull.

15 SUMMARY OF DERIVATIVE REGISTERS

Table 26 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody and Port Interrupt Control Register (MDYCON)	EPI3	EPI2	EPI1	EPI0	0	0	0	EMO	R/W
14 to FF	not used									

16 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+7.0	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	–50	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

17 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

18 DC CHARACTERISTICS

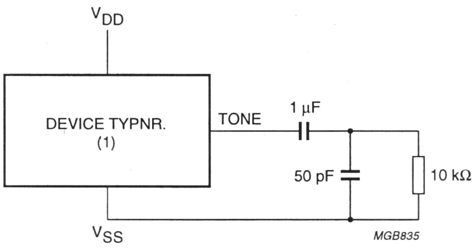
V_{DD} = 1.8 to 6 V (note 1); V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 8 to 12)						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 3	–	1.0	5.5	μA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 3	–	–	10	μA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	1	μA
Port outputs (see Figs 13 to 15)						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	–10	–30	–	μA
		V_{DD} = 3 V; V_O = 0 V	–	–140	–300	μA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–3.5	–	mA
TONE output (see Fig.7; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 7)						
$CY_{t/w}$	endurance (erase/write cycles)	note 6	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset						
V_{POR}	Power-on-reset level	configuration PCD3756A; see Table 25	0.8	1.3	1.8	V

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
    a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
    b) Typical values: 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; $\overline{\text{RESET}}$, T1 and CE/$\overline{\text{T0}}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{\text{T0}}$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. Verified on sampling basis.
7. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.



(1) Device typenr.: PCD3356A, PCD3357A or PCD3359A.

Fig.7 TONE output test circuit.

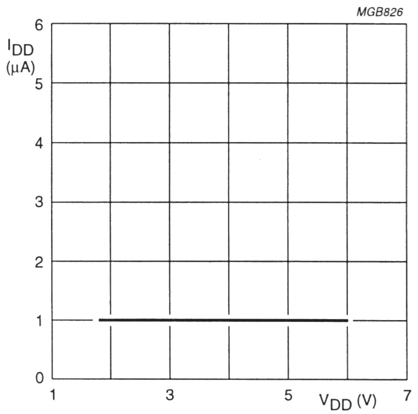
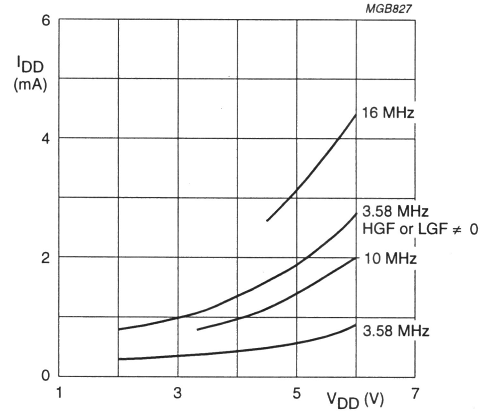
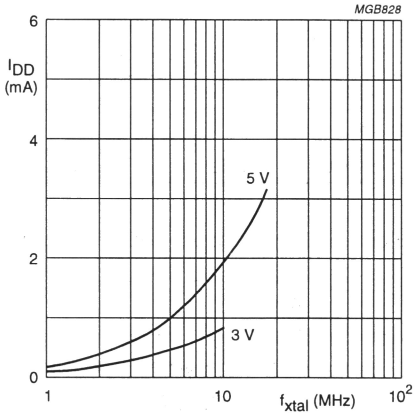


Fig.8 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



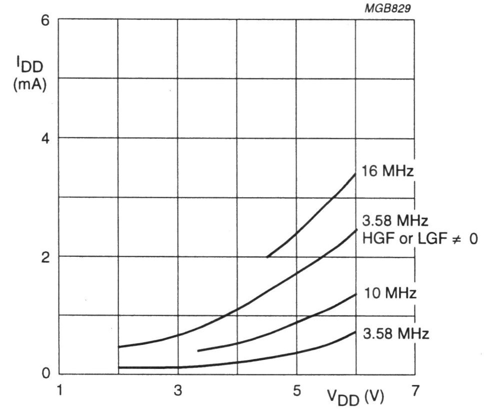
Measured with crystal between XTAL1 and XTAL2.

Fig.9 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



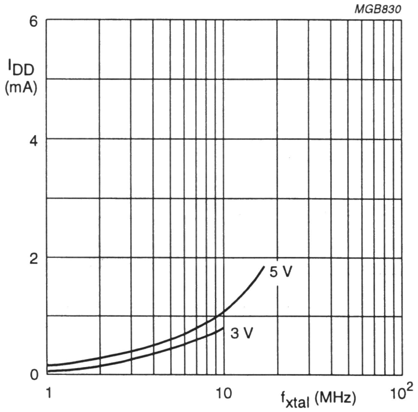
Measured with function generator on XTAL1.

Fig.10 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



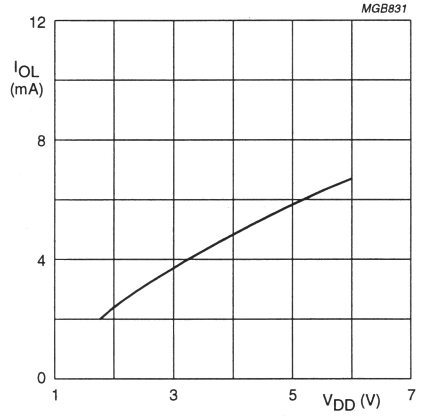
Measured with crystal between XTAL1 and XTAL2.

Fig.11 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.12 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



$V_O = 0.4$ V.

Fig.13 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

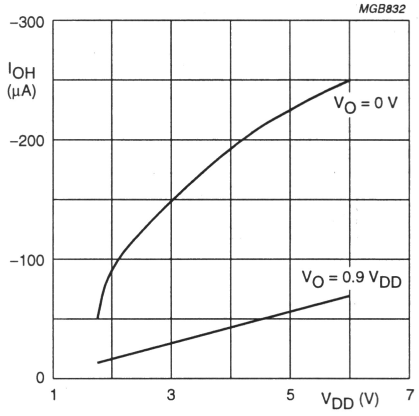
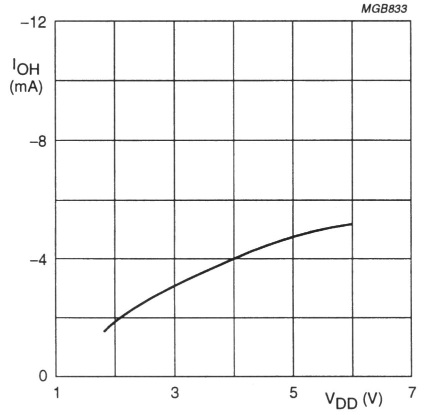


Fig.14 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.15 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

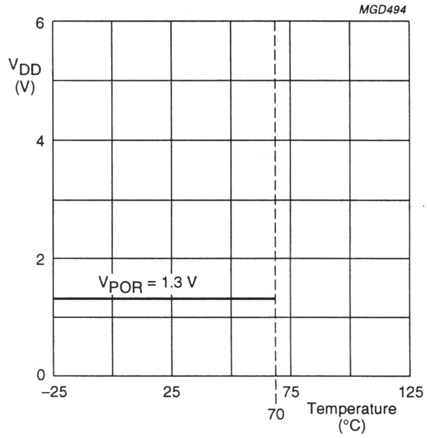


Fig.16 Typical Power-on-reset level (V_{POR}) as function of temperature.

19 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.17	1	–	16	MHz
Oscillator (see Fig.18)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

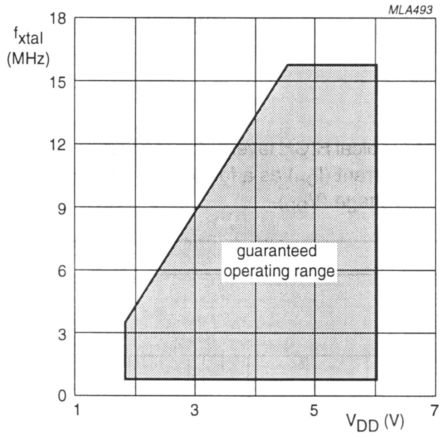


Fig.17 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

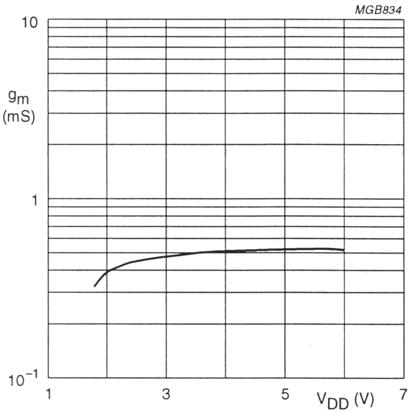


Fig.18 Typical transconductance as a function of supply voltage (V_{DD}).

PROGRAMMABLE MULTI-TONE TELEPHONE RINGER

GENERAL DESCRIPTION

The PCD3360 is a CMOS integrated circuit, designed to replace the electro-mechanical bell in telephone sets. It meets most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. No audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell
- Delta-modulated output signal that approximates a sinewave
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333	Hz
Number of intervals per tone sequence		15 or 16	
Lower limits of frequency discriminator		13,33 or 20	Hz
Upper limits of frequency discriminator		30 or 60	Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5	kΩ
Switch-on delay at 25 Hz	max.	60	ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT38).
PCD3360T: 16-lead mini-pack; plastic (SO16L; SOT162A).

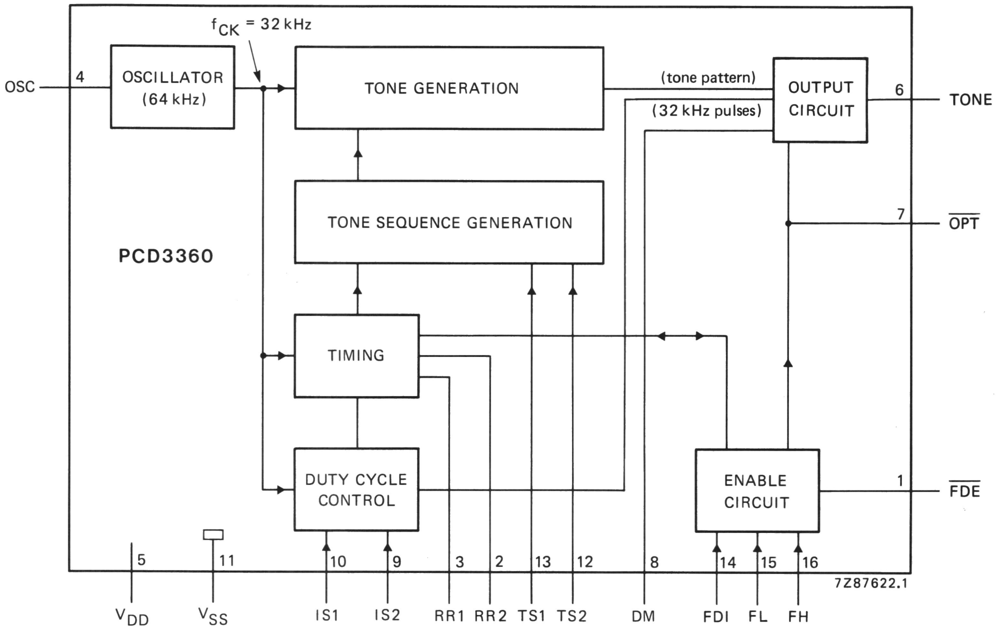

f_{CK} = 32 kHz
OSC
4
OSCILLATOR (64 kHz)
TONE GENERATION
(tone pattern)
(32 kHz pulses)
OUTPUT CIRCUIT
6
TONE
TONE SEQUENCE GENERATION
7
OPT
PCD3360
TIMING
DUTY CYCLE CONTROL
ENABLE CIRCUIT
1
FDE
5
11
10
9
3
2
13
12
8
14
15
16
7Z87622.1
V_{DD}
V_{SS}
IS1
IS2
RR1
RR2
TS1
TS2
DM
FDI
FL
FH

Fig. 1 Block diagram.

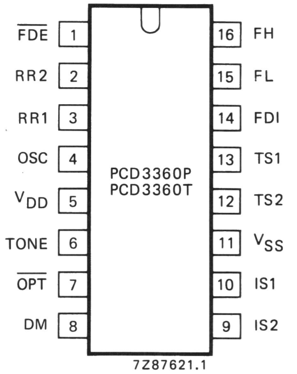

FDE 1
RR2 2
RR1 3
OSC 4
V_{DD} 5
TONE 6
OPT 7
DM 8
16 FH
15 FL
14 FDI
13 TS1
12 TS2
11 V_{SS}
10 IS1
9 IS2
PCD3360P
PCD3360T
7Z87621.1

Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{\text{FDE}}$	frequency discriminator enable
2	RR2	repetition rate selection
3	RR1	
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{\text{OPT}}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	
11	V_{SS}	negative supply
12	TS2	tone sequence selection
13	TS1	
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	upper frequency limit selection

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

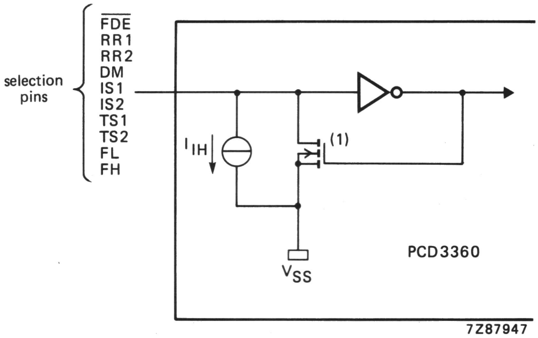
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{\text{FDE}}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 3). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 3 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{\text{FDE}}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{\text{FDE}}$.

When $\overline{\text{FDE}}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{\text{FDE}}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{\text{FDE}}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

FUNCTIONAL DESCRIPTION (continued)

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 8) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $<$ 0,1 μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 4.

tone key	–	c	d	e	g	b	c	e
frequency (Hz)	0	533	600	667	800	1000	1067	1333
frequency ratio		8 :	9 :	10 :	12 :	15 :	16 :	20
tone code	0	1	2	3	4	5	6	7

7Z87948

Fig. 4 Available tones and their corresponding internal ROM tone code.

Four tone sequences are programmed in the internal ROM (see Fig. 5). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{\text{FDE}}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 5.

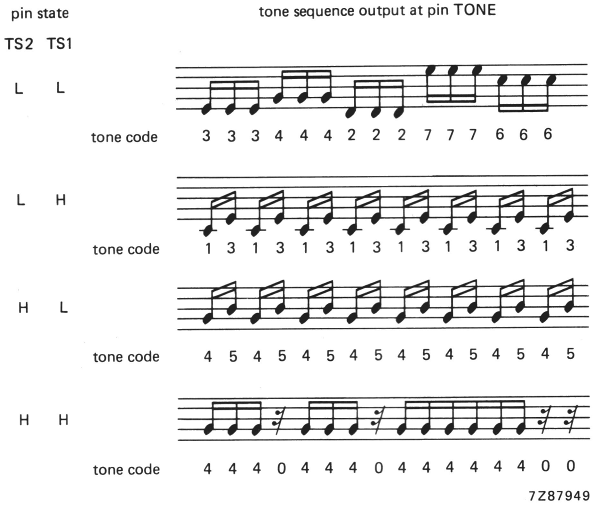

pin state
tone sequence output at pin TONE
TS2 TS1
L L
tone code
3 3 3 4 4 4 2 2 2 7 7 7 6 6 6
L H
tone code
1 3 1 3 1 3 1 3 1 3 1 3 1 3 1 3
H L
tone code
4 5 4 5 4 5 4 5 4 5 4 5 4 5 4 5
H H
tone code
4 4 4 0 4 4 4 0 4 4 4 4 4 4 0 0
7Z87949

Fig. 5 Tone sequences mask-programmed in the PCD3360.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval ms
RR1	RR2	
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

FUNCTIONAL DESCRIPTION (continued)

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 6.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 8), the input impedance Z_I and and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
			1	1,9	–	40	tbf	tbf
L	L	automatic swell	2	2,9	–	20	17,5	–4
			>2	4,1	1,8	5	7	0
L	H	constant level	–	2,9	–	20	17,5	–4
H	L		–	3,8	–	10	10,5	tbf
H	H		–	5,4	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} at 25 Hz in Fig. 8.

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 8) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 7). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{\text{OPT}}$)

The $\overline{\text{OPT}}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

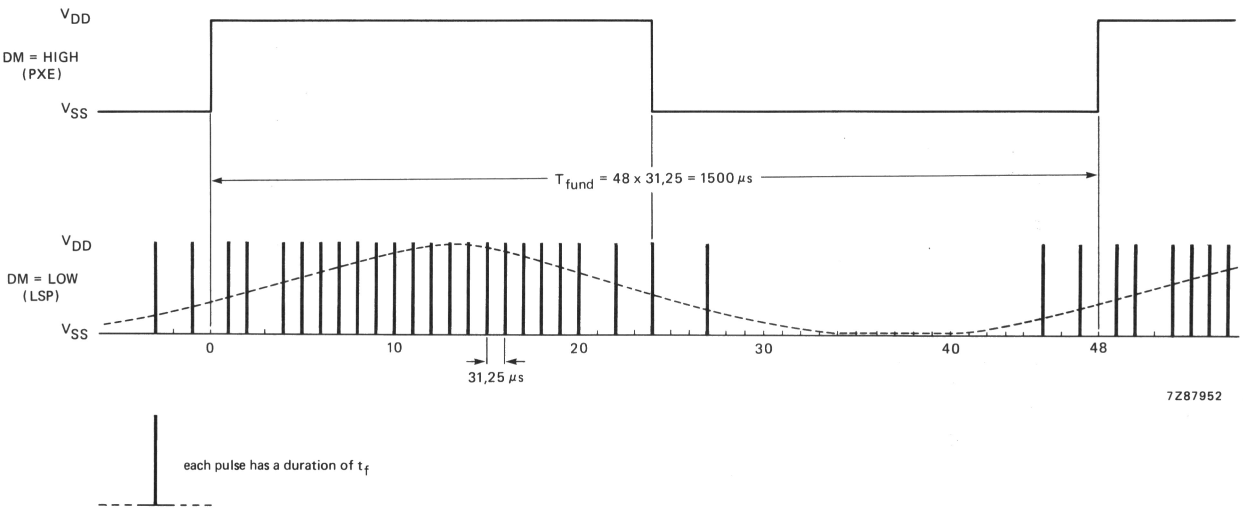

V$_{DD}$
DM = HIGH
(PXE)
V$_{SS}$
T$_{fund}$ = 48 x 31,25 = 1500 μs
V$_{DD}$
DM = LOW
(LSP)
V$_{SS}$
0
10
20
30
40
48
31,25 μs
7Z87952
each pulse has a duration of t$_f$

Fig. 6 Fundamental signal (667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

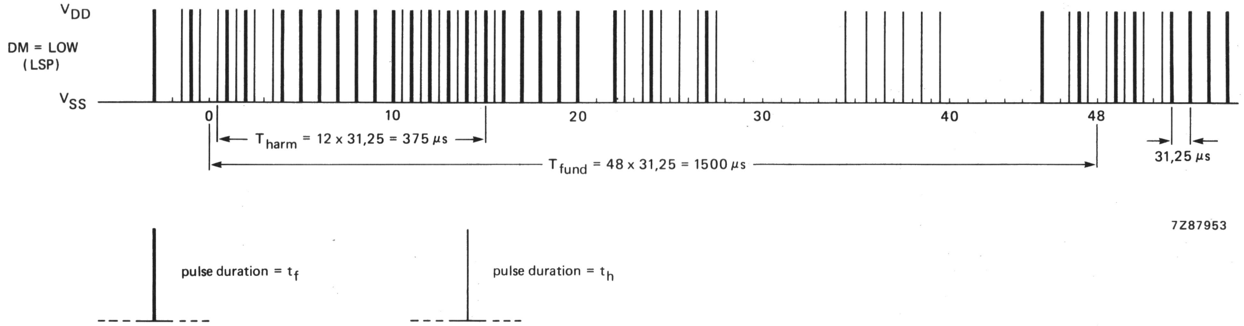

V$_{DD}$
DM = LOW
(LSP)
V$_{SS}$
0
10
20
30
40
48
T$_{harm}$ = 12 x 31,25 = 375 μs
T$_{fund}$ = 48 x 31,25 = 1500 μs
31,25 μs
7Z87953
pulse duration = t$_f$
pulse duration = t$_h$

Fig. 7 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I$, $\pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	$V_{SB}+0,1$	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	3,9	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	$0,5V_{SB}$	–	V
Operating supply current (note 3)	I_{DD}	–	110	140	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 4)	I_{SB}	–	3	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	$0,3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0,7V_{DD}$	–	V_{DD}	V
Pull-down circuits of inputs					
FDE, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with $V_{FDI} = 0,3V_{DD}$; T_{amb} = 25 °C	I_{SL}	14	23	32	μA
temperature coefficient of I_{SL}	$-\Delta I_{SL}$	–	0,5	–	%/°C
pull-down current with $V_{FDI} = 0,8V_{DD}$	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 5)	$\pm I_{IS}$	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at $V_{OH} = V_{DD}-0,5$ V	$-I_{OH}$	1	2	–	mA

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = –25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 6
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	50	ms
at FL = HIGH	$t_{d(off)}$	–	–	75	ms
Oscillator frequency at R_{osc} = 365 kΩ; C_{osc} = 56 pF; T_{amb} = 25 °C (note 7)	f_{osc}	60	64	68	kHz
Frequency variation					
as a function of V_{DD}	$-\Delta f_{osc}$	–	1	–	%/V
as a function of T_{amb}	$-\Delta f_{osc}$	–	0,05	–	%/K

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. R_{osc} = 365 kΩ; C_{osc} = 56 pF; FDI = $\overline{FDE}$ = V_{DD}; all other inputs and outputs open circuit.
4. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
5. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
6. The switch-on delay is measured in cycles of incoming ringing frequency.
7. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 8.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0,5V_{DD}$ typ. 3,4 V for $V_{DD} = 6,8$ V)
- The pull-down current of input FDI (20 μA typ. for FDI $<$ 3,4 V)
- The value of R2 (680 kΩ in Fig. 8)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$$V_H = 3,4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17 \text{ V}.$$

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus $V_L = 3,4$ V.

The minimum operating voltage across C3 is 17,8 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,8 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R3 (100 kΩ in Fig. 8)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72A (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 9. The only significant difference between Fig. 8 and Fig. 9 is the output stage. Two BST72A transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

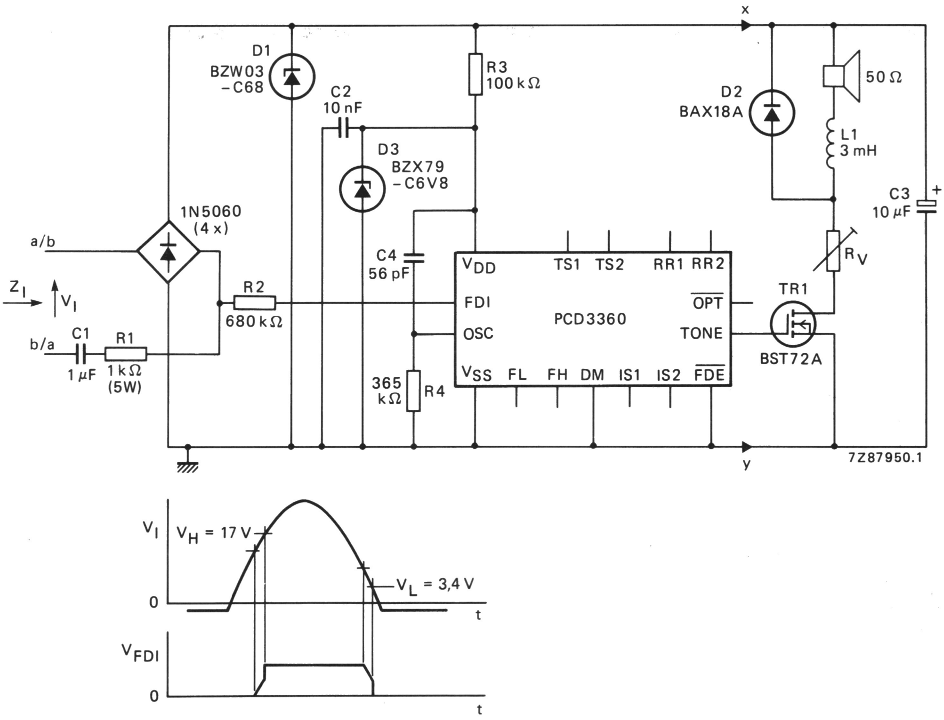

x
D1
BZW03
–C68
C2
10 nF
R3
100 kΩ
D2
BAX18A
50 Ω
L1
3 mH
D3
BZX79
–C6V8
C3
10 μF
1N5060
(4 x)
a/b
C4
56 pF
V_{DD}
TS1
TS2
RR1
RR2
R_V
Z_I
V_I
R2
680 kΩ
FDI
PCD3360
$\overline{OPT}$
TR1
b/a
C1
1 μF
R1
1 kΩ
(5W)
OSC
TONE
BST72A
365 kΩ
R4
V_{SS}
FL
FH
DM
IS1
IS2
$\overline{FDE}$
y
7Z87950.1
V_I
V_H = 17 V
V_L = 3,4 V
0
t
V_{FDI}
0
t

Fig. 8 Transformerless electronic ringer with PCD3360 and a loudspeaker.

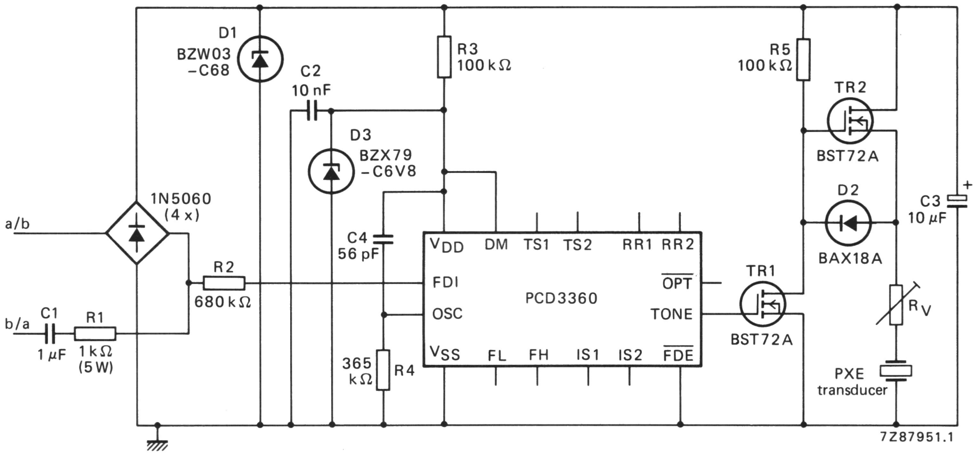

D1
BZW03
–C68
C2
10 nF
R3
100 kΩ
R5
100 kΩ
TR2
BST72A
D3
BZX79
–C6V8
D2
C3
10 μF
1N5060
(4 x)
a/b
C4
56 pF
V_{DD}
DM
TS1
TS2
RR1
RR2
BAX18A
R2
680 kΩ
FDI
PCD3360
$\overline{OPT}$
TR1
R_V
b/a
C1
1 μF
R1
1 kΩ
(5 W)
OSC
TONE
BST72A
365 kΩ
R4
V_{SS}
FL
FH
IS1
IS2
$\overline{FDE}$
PXE
transducer
7Z87951.1

Fig. 9 PCD3360 ringer with PXE transducer.

CONTENTS

1 INTRODUCTION
2 FEATURES
3 GENERAL DESCRIPTION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FUNCTIONAL DESCRIPTION
6.1 Central processing unit
6.2 Program memory
6.3 Data memory
6.3.1 Working registers
6.3.2 Program Counter stack
6.4 Program Counter
6.5 Program Status Word
6.6 Interrupts
6.6.1 External interrupt
6.6.2 Derivative interrupt
6.6.3 Timer/event counter interrupt
6.7 Timer/event counter 1
6.7.1 Test 1/count input (T1)
6.8 Parallel ports
6.9 Timing
6.10 Reduced power modes
6.10.1 Idle mode
6.10.2 Stop mode
6.11 Oscillator
6.12 Reset
6.12.1 Passive external reset
6.12.2 Active external reset
6.12.3 Internal reset
6.12.4 Reset state
6.13 Derivative logic
7 INSTRUCTION SET
7.1 Instruction map
8 DEFINITIONS
9 LIFE SUPPORT APPLICATIONS

1 INTRODUCTION

This data sheet describes the shared properties of the PCD33xxA Family of microcontrollers and its quickly growing number of derivative microcontrollers. For a particular microcontroller, this data sheet should be read in conjunction with the individual data sheet of the specific device.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O all in one package
- Up to 8 kbytes ROM
- Up to 256 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, timer/event counter, derivative
- Two test inputs, one of which also serves as the external interrupt input
- Power-on-reset, Stop and Idle modes
- Supply voltage range: 1.8 to 6 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: −25 to +70 °C
- Manufactured in silicon gate CMOS process.

3 GENERAL DESCRIPTION

The PCD33xxA Family of microcontrollers provide up to 8 kbytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the well-known MAB8048. Being similar to the MAB8400 family of NMOS controllers, some devices can serve as CMOS replacements, especially where the lower power consumption and higher speed provide advantages.

A range of One Time Programmable (OTP) devices with external program memory and ‘Piggy-backs’, as well as emulation probes and prototyping systems are available.

4 BLOCK DIAGRAM

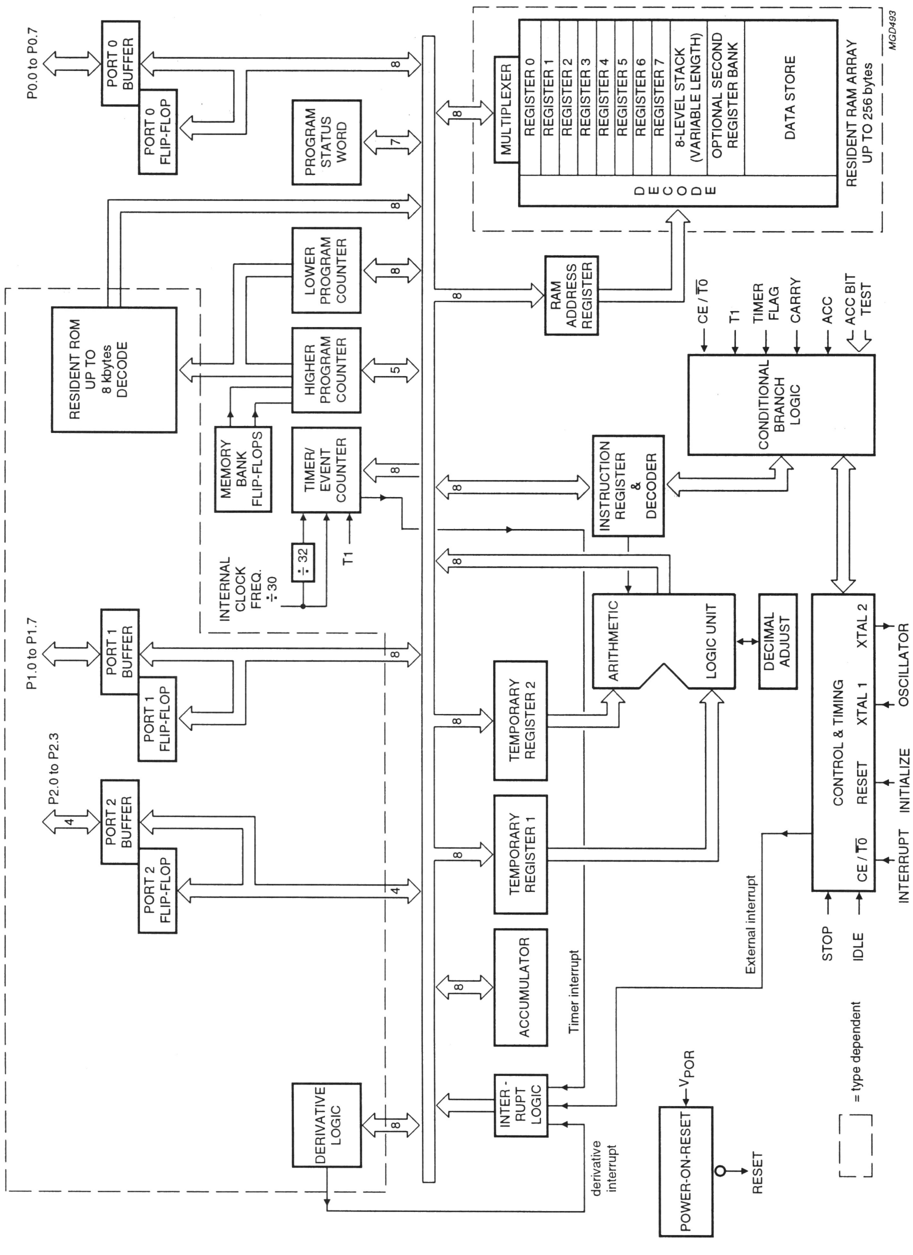

P0.0 to P0.7
PORT 0 BUFFER
PORT 0 FLIP-FLOP
PROGRAM STATUS WORD
7
8
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8-LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
D E C O D E
RESIDENT RAM ARRAY UP TO 256 bytes
MGD493
RESIDENT ROM UP TO 8 kbytes DECODE
LOWER PROGRAM COUNTER
HIGHER PROGRAM COUNTER
5
RAM ADDRESS REGISTER
CE / T0
T1
TIMER FLAG
CARRY
ACC
ACC BIT TEST
CONDITIONAL BRANCH LOGIC
MEMORY BANK FLIP-FLOPS
TIMER/ EVENT COUNTER
INSTRUCTION REGISTER & DECODER
÷ 32
T1
INTERNAL CLOCK FREQ. ÷ 30
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
P1.0 to P1.7
PORT 1 BUFFER
PORT 1 FLIP-FLOP
TEMPORARY REGISTER 2
CONTROL & TIMING
XTAL 2
XTAL 1
OSCILLATOR
RESET
INITIALIZE
CE / T0
INTERRUPT
P2.0 to P2.3
4
PORT 2 BUFFER
PORT 2 FLIP-FLOP
TEMPORARY REGISTER 1
External interrupt
STOP
IDLE
ACCUMULATOR
Timer interrupt
= type dependent
POWER-ON-RESET
V_POR
RESET
DERIVATIVE LOGIC
INTER-RUPT LOGIC
derivative interrupt

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

For individual pinning configurations consult the data sheet of the specific device.

5.2 Pin description

Table 1 describes the common functions of the devices. For full details of pin descriptions consult the data sheet of the specific device.

Table 1 Common functions

SYMBOL	TYPE	DESCRIPTION
V_{SS}	P	ground
V_{DD}	P	positive supply voltage
XTAL1	I	crystal oscillator/external clock input
XTAL2	O	crystal oscillator output
RESET	I	reset input
CE/$\overline{\text{T0}}$	I	Chip enable/Test 0
T1	I	Test 1/count input of 8-bit timer/event counter 1
P0.0 to P0.7	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 to P1.7	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 to P2.3	I/O	Port 2: quasi-bidirectional I/O lines

6 FUNCTIONAL DESCRIPTION

6.1 Central processing unit

The PCD33xxA Family provides an adequate instruction set with arithmetic, logic, branching, input/output and control facilities. Special highlights are the instructions for BCD arithmetic, nibble handling, conditional branches, loop control (DJNZ) and table look-up (MOVP).

Code and execution efficiency is achieved by using a maximum of two bytes and two execution cycles per instruction (see Chapter 7).

6.2 Program memory

The program memory consists of up to 8 kbytes of read-only memory (ROM). Each location is directly addressable by the Program Counter. The program memory is mask-programmed at the factory. Figure 2 illustrates the program memory map.

Four program memory locations are of special importance:

- Location 0: first instruction to be executed after the processor is reset
- Location 3: first instruction of an external interrupt (CE/$\overline{\text{T0}}$) routine
- Location 5: first instruction of a derivative interrupt routine
- Location 7: first instruction of a timer/event counter interrupt routine.

Only 11 bits of the 13-bit Program Counter function as a counter. The two most significant bits can only be preset. The program memory is therefore, structured into banks of 2 kbytes. Transfer of control to other memory banks is performed by unconditional branches (JMP) or subroutine calls (CALL) when another memory bank has been pre-selected (by SEL MB instruction).

Each program memory bank is further divided into 8 pages of 256 bytes. Indirect (JMPP) and conditional branches cannot cross page boundaries.

6.3 Data memory

Data memory consists of up to 256 bytes of random access memory (RAM). All locations are indirectly addressable using RAM pointer registers. Up to 16 register locations are directly addressable.
Data memory also includes an 8-level Program Counter stack addressed by a 3-bit Stack Pointer. All RAM locations make efficient program loop counters if used with the decrement register and test instruction (DJNZ).
Figure 3 illustrates the data memory map.

6.3.1 WORKING REGISTERS

Locations 0 to 7 are working registers. They are accessible by efficient one byte/one cycle instructions, thus making these locations suitable for frequently accessed intermediate results.

As an alternative to locations 0 to 7, locations 24 to 31 may be used as working registers. Register Bank selection is made by SEL RB0/RB1 instructions. Register Bank 1 may be used as an extension of Register Bank 0, as an alternative register bank for interrupt service or as general purpose data memory.

The first two locations of each bank (R0, R1, R0' and R1') serve as RAM pointers that indirectly address all RAM locations.

6.3.2 PROGRAM COUNTER STACK

Locations 8 to 23 may be used as an 8-level Program Counter stack reserving 2 locations per level, or as general purpose RAM. The stack (see Fig.5) saves return addresses and status during interrupt or subroutine servicing. Nesting of subroutines and/or interrupts is permitted up to 8-levels deep.

The 3-bit Stack Pointer always points to the next free stack level. Following device reset, the Stack Pointer points to level 0 (locations 8 and 9). On each subroutine call (CALL) or interrupt, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are transferred to the level indicated by the Stack Pointer. The Stack Pointer increments and points to the next free level. Overflow from level 7 to level 0 occurs after nesting eight levels deep. Further subroutine calls and/or interrupts must not occur at this stage since this would result in loss of program content; overriding level 0 content.

Return from interrupt must be performed by the RETR instruction, which decrements the Stack Pointer and restores the Program Counter and Program Status Word, valid before the interrupt occurred. Return from subroutine should be performed by the RET instruction. In contrast to RETR, RET does not restore the Program Status Word.

As a general rule, the use of RETR in conjunction with a subroutine call is not recommended. The use of RETR must also be avoided with subroutines called from interrupt routines because it prematurely terminates the interrupt state (see Section 6.6).

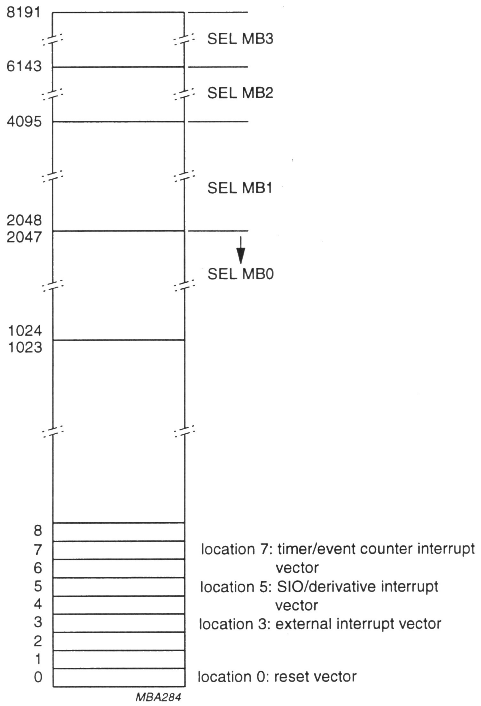

8191
SEL MB3
6143
SEL MB2
4095
SEL MB1
2048
2047
SEL MB0
1024
1023
8
7
6
5
4
3
2
1
0
location 7: timer/event counter interrupt vector
location 5: SIO/derivative interrupt vector
location 3: external interrupt vector
location 0: reset vector
MBA284

Fig.2 Program memory map.

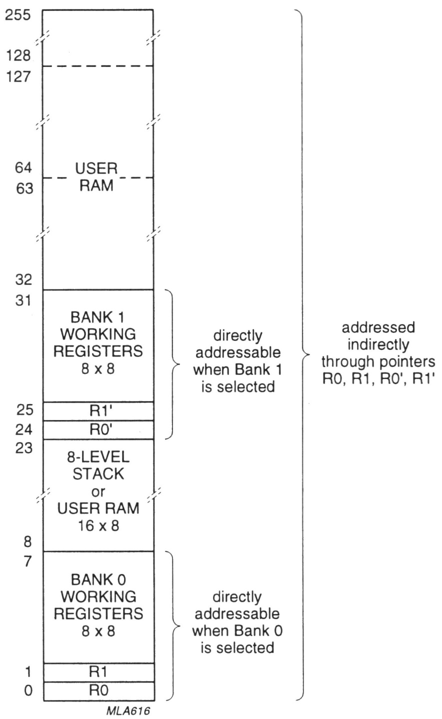

255
128
127
64
63
USER RAM
32
31
BANK 1 WORKING REGISTERS 8 x 8
25
R1'
24
R0'
23
8-LEVEL STACK or USER RAM 16 x 8
8
7
BANK 0 WORKING REGISTERS 8 x 8
1
R1
0
R0
directly addressable when Bank 1 is selected
directly addressable when Bank 0 is selected
addressed indirectly through pointers R0, R1, R0', R1'
MLA616

Fig.3 Data memory map.

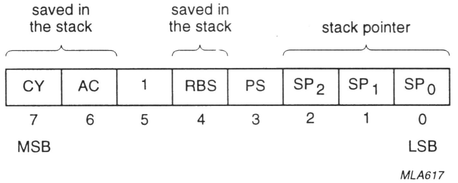

saved in the stack
saved in the stack
stack pointer
CY
AC
1
RBS
PS
SP2
SP1
SP0
7
6
5
4
3
2
1
0
MSB
LSB
MLA617

Fig.4 Program Status Word.

6.4 Program Counter

The 13-bit Program Counter is able to address up to 8 kbytes of ROM (see Fig.6). 11 bits (PC0 to PC10) are auto-incrementing. The two most significant bits (PC11 and PC12) must be changed under program control by SEL MB followed by a JMP or CALL instruction.

6.5 Program Status Word

The Program Status Word (PSW) is an 8-bit register in the CPU which stores information about the current status of the microcontroller (see Fig.4).

The PSW bits are:

- Bits 0 to 2: Stack Pointer bits (SP0, SP1, SP2)
- Bit 3: timer Prescaler Select (PS); 0 = modulo-32, 1 = modulo-1 (no prescaling)
- Bit 4: working Register Bank Select (RBS); 0 = register bank 0, 1 = register bank 1
- Bit 5: not used (fixed at 1)
- Bit 6: Auxiliary Carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7: Carry (CY); the carry flag indicates that the previous operation resulted in an overflow of the Accumulator.

All bits can be read using the MOV A, PSW instruction. Bits 0, 1 and 2 are affected by CALL, RET, RETR and interrupts. Bit 3 can be controlled by MOV PSW, A and bit 4 by SEL RB instructions. Bit 6 is set and cleared as a side-effect of ADD and ADDC instructions. Bit 7 is affected by ADD, ADDC, DA, RLC, RRC, CLR C and CPL C instructions.

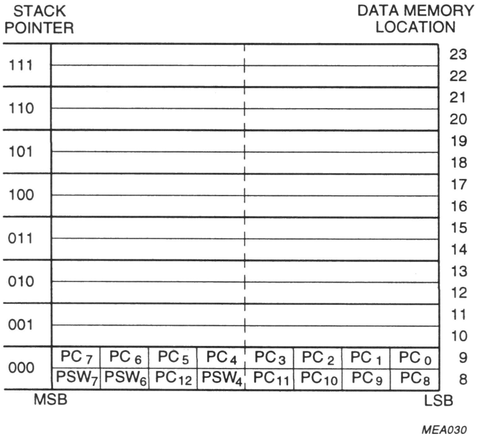

STACK POINTER
DATA MEMORY LOCATION
111
110
101
100
011
010
001
000
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
PC_7 PC_6 PC_5 PC_4 PC_3 PC_2 PC_1 PC_0
PSW_7 PSW_6 PC_{12} PSW_4 PC_{11} PC_{10} PC_9 PC_8
MSB
LSB
MEA030

Fig.5 Program Counter Stack.

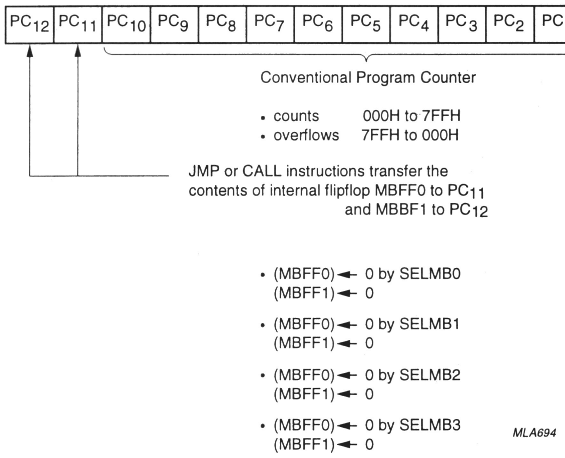

PC12
PC11
PC10
PC9
PC8
PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
Conventional Program Counter
• counts 000H to 7FFH
• overflows 7FFH to 000H
JMP or CALL instructions transfer the contents of internal flipflop MBFF0 to PC11 and MBBF1 to PC12
• (MBFF0)← 0 by SELMB0
(MBFF1)← 0
• (MBFF0)← 0 by SELMB1
(MBFF1)← 0
• (MBFF0)← 0 by SELMB2
(MBFF1)← 0
• (MBFF0)← 0 by SELMB3
(MBFF1)← 0
MLA694

Fig.6 Program Counter.

6.6 Interrupts

External, derivative and timer/event counter interrupts are handled by the PCD33xxA Family. The interrupt mechanism is single level, i.e. an executing interrupt routine cannot be pre-empted unless by reset. Further interrupt requests are latched. If several interrupt requests are detected simultaneously, they are honoured according to their priority:

- External interrupt (highest priority)
- Derivative interrupt
- Timer/event counter interrupt (lowest priority).

An interrupt request is only sensed if the corresponding enable flag is set (see Fig.7). When the request is honoured, the contents of the Program Counter and bits 4, 6 and 7 of the Program Status Word are saved on the Program Counter stack. The Program Counter is loaded with the appropriate interrupt vector, thereby indicating the beginning of the interrupt routine. Since the Accumulator is not automatically saved, it must be saved and restored by user software. The interrupt routine must be terminated by the RETR (return and restore) instruction. At least one instruction of the main program will then be executed before another interrupt routine is entered.

To avoid erroneous real-time programs, a few words of caution:

- While the interrupt is in progress, the two most significant bits of the Program Counter are frozen at zero. Thus, interrupt routines and subroutines called from interrupt routines must reside entirely in Bank 0.
- The SEL MB instruction must not be used in interrupt routines and in subroutines called from interrupt routines. Otherwise, the changed contents of MBFF0 and MBFF1 (see Fig.6) may lead to erroneous JMP and CALL destinations after return from interrupt.
- Subroutines and nested subroutines called from the interrupt routine must all end with RET since RETR clears the Interrupt In Progress flag (IIP), as a side-effect (see Figs 7 and 8). Further pending interrupts would then interfere with the interrupt routine in progress.

6.6.1 EXTERNAL INTERRUPT

A LOW-to-HIGH transition on the $\mathrm{CE}/\overline{\mathrm{T0}}$ pin is latched in the digital filter/latch if the HIGH state exceeds 7 clock periods after a LOW state of more than 4 clock periods. If the external interrupt is enabled the External Interrupt Flag (EIF) is also asserted, thus constituting a valid external interrupt request. As soon as the IIP is clear, indicating that no interrupt routine is in progress, the external interrupt is invoked by a forced CALL to location 3. The EIF is simultaneously cleared (see Figs 7 and 8). The interrupt routine may acknowledge the interrupt via port lines. Execution of a DIS I (disable external interrupt) instruction cancels a stored interrupt request by clearing both the digital filter/latch and the EIF.

For some devices the external interrupt is shared between the $\mathrm{CE}/\overline{\mathrm{T0}}$ pin and additional wake-up interrupts from the derivative logic. Software polling may be necessary to determine the origin of request. Since the interrupt flags of the derivative logic are not cleared by DIS I, the external interrupt routine must include instructions that will remove the cause of the external interrupt. For more details about shared external interrupts consult the data sheet of the specific device.

6.6.1.1 Chip Enable/Test 0 Input ($\mathrm{CE}/\overline{\mathrm{T0}}$)

The $\mathrm{CE}/\overline{\mathrm{T0}}$ input has two purposes:

- External interrupt input (see Section 6.6.1)
- Test 0 input.

When used as a Test 0 input (external interrupt disabled) the conditional branch instruction JT0 will cause a jump if $\mathrm{CE}/\overline{\mathrm{T0}} = 1$. The conditional branch instruction JNT0 will also cause a jump if $\mathrm{CE}/\overline{\mathrm{T0}} = 0$. If $\mathrm{CE}/\overline{\mathrm{T0}}$ is not used, it must be tied to V_{DD} or V_{SS}.

6.6.2 DERIVATIVE INTERRUPT

The derivative interrupt is shared between all the interrupt sources in the derivative logic. Software polling may be necessary to determine the origin of a request.

An interrupt condition in the derivative logic will pull the PIN line LOW. If the derivative interrupt is enabled and no interrupt routine is in progress, the derivative interrupt routine will be invoked by a forced CALL to program memory location 5. The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt and thus reset PIN to its inactive HIGH state. For derivative interrupts, consult the data sheet of the specific device.

6.6.3 TIMER/EVENT COUNTER INTERRUPT

If the timer/event counter interrupt is enabled, a timer/event counter 1 overflow sets the Timer Interrupt Flag (TIF). As soon as IIP is clear, meaning that no interrupt routine is in progress, the timer/event counter interrupt routine is invoked by a forced CALL to program memory location 7. The TIF is simultaneously cleared (see Figs 7 and 8). Execution of a DIS TCNTI (disable timer/event counter interrupt) instruction cancels a stored interrupt request by clearing TIF.

The timer/event counter interrupt may also be used to simulate a second external interrupt. After an enable timer/event counter interrupt (EN TCNTI), the counter mode is enabled by a STRT CNT instruction which loads FFH (the state preceding overflow) into the counter.
A positive edge on the T1 pin will overflow the counter and set TIF.

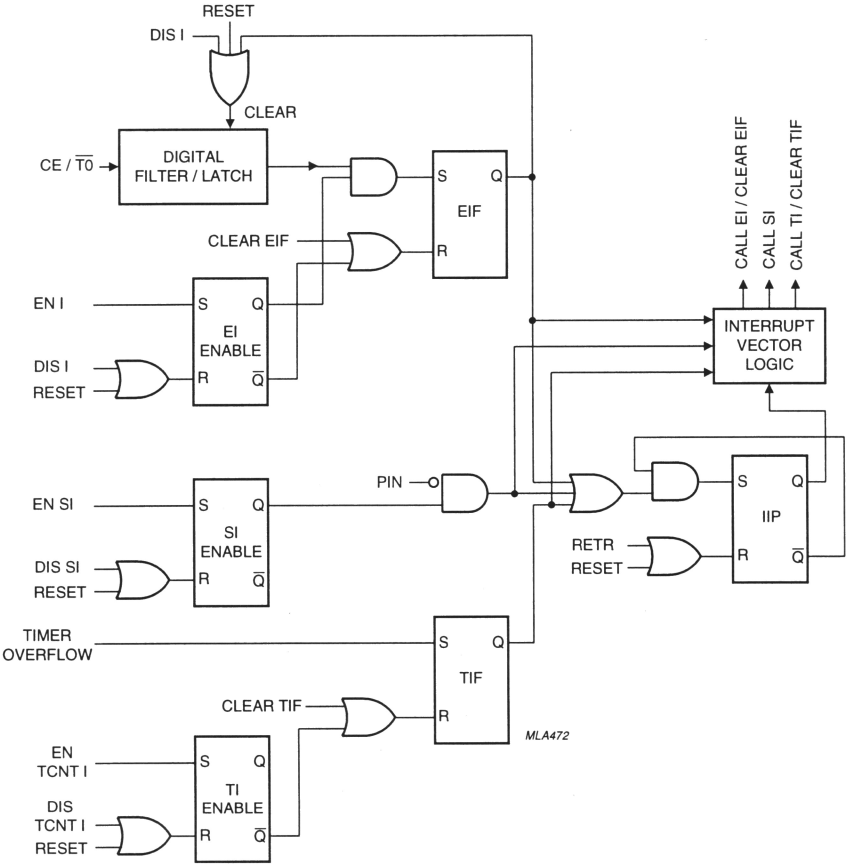

RESET
DIS I
CLEAR
CE / $\overline{T0}$
DIGITAL FILTER / LATCH
S
Q
EIF
R
CLEAR EIF
EN I
EI ENABLE
$\overline{Q}$
DIS I
RESET
CALL EI / CLEAR EIF
CALL SI
CALL TI / CLEAR TIF
INTERRUPT VECTOR LOGIC
PIN
IIP
RETR
RESET
EN SI
SI ENABLE
DIS SI
RESET
TIMER OVERFLOW
TIF
CLEAR TIF
MLA472
EN TCNT I
TI ENABLE
DIS TCNT I
RESET

Fig.7 Simplified interrupt logic schematic (the R input overrules the S input for all flags).

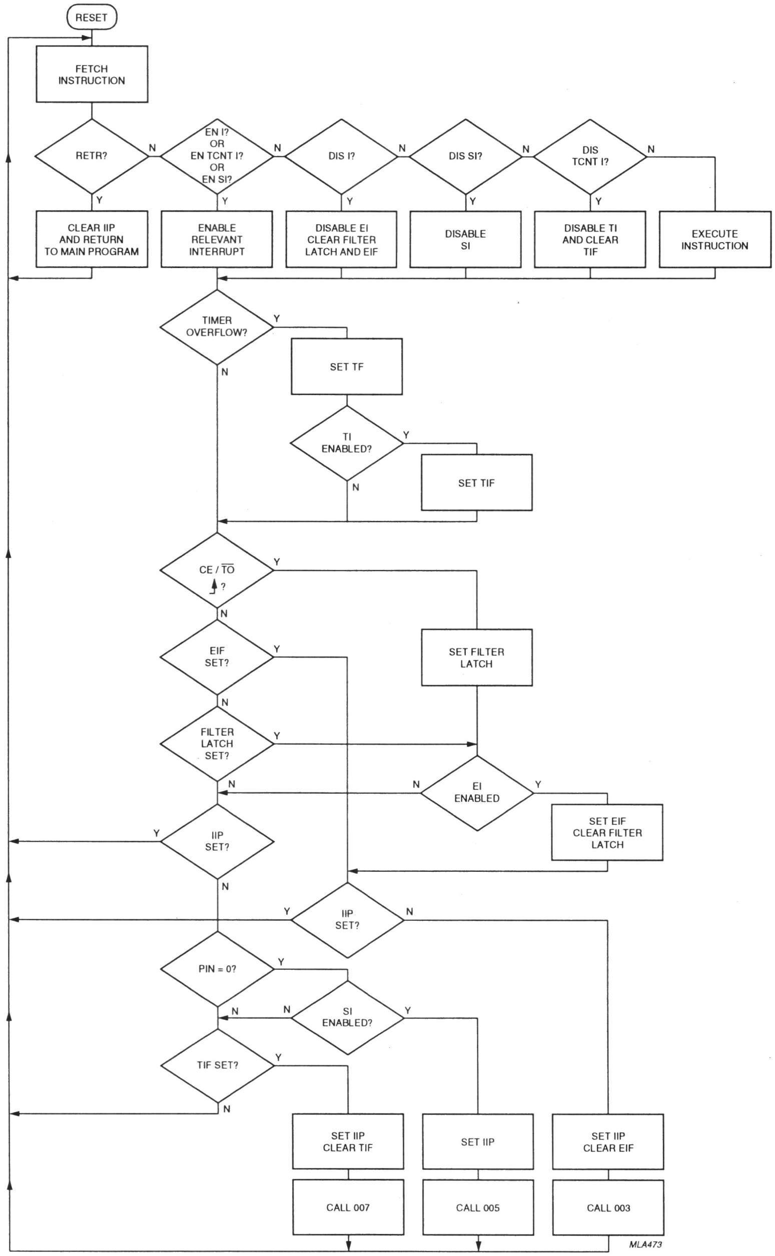

RESET
FETCH INSTRUCTION
RETR?
EN I? OR EN TCNT I? OR EN SI?
DIS I?
DIS SI?
DIS TCNT I?
Y
N
CLEAR IIP AND RETURN TO MAIN PROGRAM
ENABLE RELEVANT INTERRUPT
DISABLE EI CLEAR FILTER LATCH AND EIF
DISABLE SI
DISABLE TI AND CLEAR TIF
EXECUTE INSTRUCTION
TIMER OVERFLOW?
SET TF
TI ENABLED?
SET TIF
CE / $\overline{\text{TO}}$?
SET FILTER LATCH
EIF SET?
FILTER LATCH SET?
EI ENABLED
SET EIF CLEAR FILTER LATCH
IIP SET?
IIP SET?
PIN = 0?
SI ENABLED?
TIF SET?
SET IIP CLEAR TIF
SET IIP
SET IIP CLEAR EIF
CALL 007
CALL 005
CALL 003
MLA473

Fig.8 Flow chart illustrating CPU control in the presence of interrupts.

6.7 Timer/event counter 1

An internal 8-bit up counter is provided. The counter can be preset and read by the MOV T, A and MOV A, T instructions.

When the counter is to be used in the timer mode, a STRT T (start timer) instruction must be executed. Depending on the PS bit in the Program Status Word, the counter will increment every machine cycle (PS = 1, $\frac{1}{30} \times f_{xtal}$) or every 32 machine cycles (PS = 0, $\frac{1}{960} \times f_{xtal}$). STRT T clears the prescaler (see Fig.9) which is not otherwise accessible.

To count external events a STRT CNT (start event counter) instruction must be executed. A LOW-to-HIGH transition on pin T1 is counted if the HIGH state exceeds 4 clock periods after a LOW state of more than 4 clock periods. The maximum count rate is one increment per machine cycle ($\frac{1}{30} \times f_{xtal}$).

The timer mode and the event counter mode are both inhibited after reset or by executing a STOP TCNT (stop timer/event counter) instruction (see Fig.9).

In both the timer and in event counter modes, overflow has two effects:

- If the timer/event counter interrupt is enabled TIF is asserted thereby generating a timer/event counter interrupt request (see Section 6.6).
- The Timer Flag (TF) is set. TF can be tested by conditional branch instructions JTF (jump if TF = 1) or JNTF (jump if TF = 0). The JTF and JNTF instruction, as a side-effect, reset TF. The only other way to clear TF is to reset the microcontroller.

6.7.1 TEST 1/COUNT INPUT (T1)

The T1 input has two purposes:

- Count input of 8-bit timer/event counter 1 (see Section 6.7)
- Test 1 input.

When used as a Test 1 input the conditional branch instruction JT1 will cause a jump if T1 = 1. The conditional branch instruction JNT1 will also cause a jump if T1 = 0. If T1 is not used, it must be tied to V_{DD} or V_{SS}.

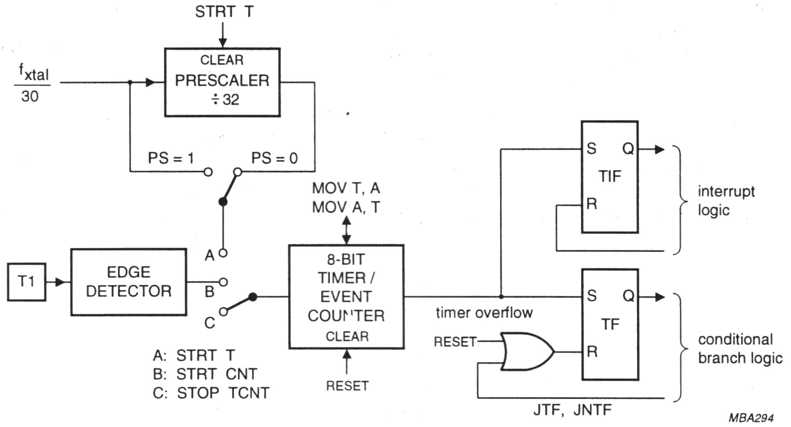

STRT T
$\frac{f_{xtal}}{30}$
CLEAR
PRESCALER
÷32
PS = 1
PS = 0
MOV T, A
MOV A, T
T1
EDGE DETECTOR
A
B
C
8-BIT TIMER / EVENT COUNTER
CLEAR
RESET
A: STRT T
B: STRT CNT
C: STOP TCNT
timer overflow
RESET
S
Q
TIF
R
interrupt logic
S
Q
TF
R
conditional branch logic
JTF, JNTF
MBA294

Fig.9 Timer/event counter 1.

6.8 Parallel ports

Three standard quasi-bidirectional I/O ports are defined:

- Port 0: parallel port of 8 lines (P0.0 to P0.7)
- Port 1: parallel port of 8 lines (P1.0 to P1.7)
- Port 2: parallel port of 4 lines (P2.0 to P2.3).

Several members of the PCD33xxA Family provide all 20 port lines. The eight Port 0 lines (P0.0 to P0.7) are available as a minimum. In addition to the standard ports, many PCD33xxA microcontrollers offer a variety of derivative ports. Please consult the data sheet of the specific device.

In general, all parallel ports can be used as either inputs or outputs. Output data written to a port is latched and remains unchanged until rewritten. If the port is used as an input, the external data is not latched and must remain stable until it is accessed by the CPU.

The standard port configuration is illustrated in Fig.11. When a logic 0 is written to the master/slave flip-flop, TR2 and TR3 are both in the OFF condition. TR1 turns ON and drives the output to V_{SS}.

When a logic 1 is written to the master/slave flip-flop, TR1 turns OFF. TR2 and TR3 both turn ON driving the output rapidly to V_{DD}. TR2 remains in the ON condition for the duration of the write pulse only. The constant current source is responsible for keeping the output line high. Sufficient source current is available for a TTL load HIGH level; the line can, however, be overridden by an external device. This is used when the port line serves as an input, but it may also be useful for wired-OR applications. In the latter case, unnecessary current through external devices is avoided since repeated logic 1 write operations will not activate TR2. The booster transistor TR2 is only asserted during a LOW-to-HIGH transition of the master/slave flip-flop. If the port line is to be used as an input, a logic 1 should first be stored in the master/slave flip-flop to turn TR1 OFF.

Access to Ports 0, 1 and 2 is provided by the parallel input/output instructions IN, OUTL, ANL and ORL.
IN inputs port data to the Accumulator. OUTL outputs Accumulator data to the port. ANL and ORL are used for data manipulation in the port flip-flop. In contrast to Ports 0, 1 and 2, derivative ports are accessed by the derivative input/output instructions MOV, ANL and ORL. ANL and ORL are used for data manipulation in the port flip-flop. MOV is used for all data transfers between port and Accumulator. The source data for the Accumulator can be loaded from either the port line or the port flip-flop.
Two derivative addresses are therefore provided per port (see Table 2).

All standard and derivative port accesses are performed by two-cycle instructions. Their instruction timing is shown in Fig.10. For input, data on port lines is sensed during timeslots 3 and 4 of machine cycle 2 (see Sections 6.9 and 6.11). For output, the data change occurs in timeslot 7. For OUTL, data changes during machine cycle 1. For ANL, ORL and MOV Dx, A, data changes during machine cycle 2.

Table 2 Derivative port address pair

ADDRESS	TYPE	ACCESS
8-bit line address	R	derivative port line
8-bit flip-flop address	R/W	derivative port flip-flop

Three port output configurations are available:

1. Standard Port; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and p-channel booster transistor TR2. TR2 is only active for 1 clock cycle during LOW-to-HIGH transitions (see Fig.11).
2. Open-drain; quasi-bidirectional I/O with only an n-channel open-drain output. Application as an output requires connection of an external pull-up resistor (see Fig.12). If unused, an Option 2 output should be tied to V_{SS}. This keeps the input path from floating, thereby avoiding undesirable current flow through input stages.
3. Push-pull; drive capability of the output will be 5 mA (typ.) at V_{DD} = 3 V in both polarities. Since short circuit currents would flow during input, push-pull lines must only be used as outputs (see Fig.13).

Besides port output configurations, the port flip-flop state, after reset, is specified for each individual port line. Usually the 'set option' will be selected, which avoids short-circuits for ports intended as inputs. However, there may be cases in which the port should output a logic zero after reset. The user may then specify the 'reset option' for certain port lines.

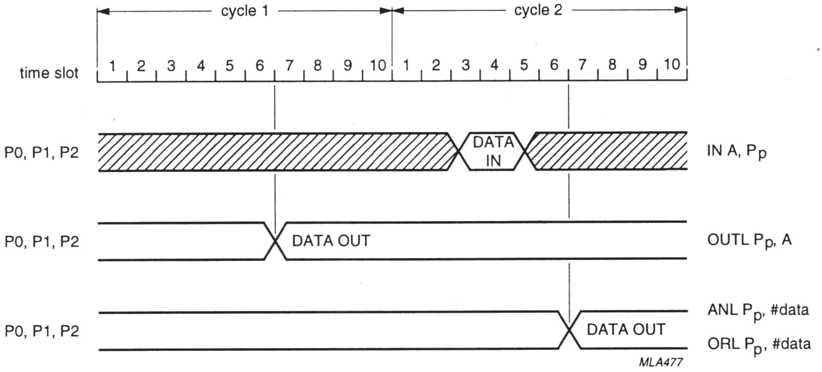

cycle 1
cycle 2
time slot
1
2
3
4
5
6
7
8
9
10
P0, P1, P2
DATA IN
IN A, Pp
P0, P1, P2
DATA OUT
OUTL Pp, A
P0, P1, P2
DATA OUT
ANL Pp, #data
ORL Pp, #data
MLA477

Fig.10 Input /output timing of standard and derivative ports.

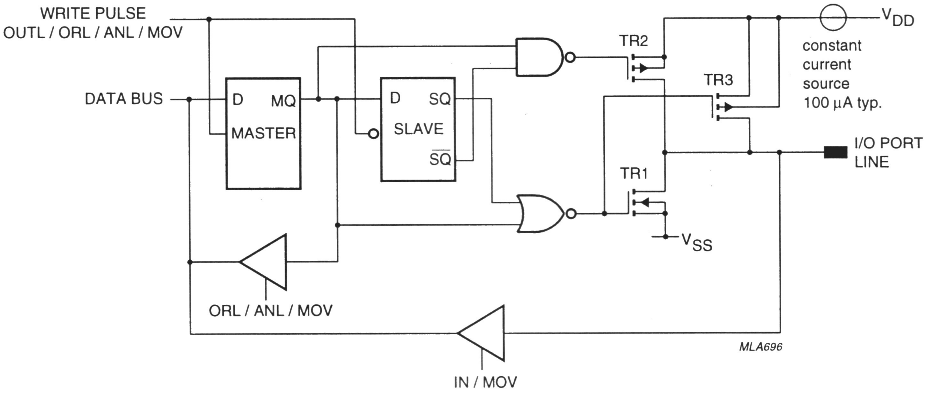

WRITE PULSE
OUTL / ORL / ANL / MOV
DATA BUS
D
MQ
MASTER
D
SQ
SLAVE
SQ
TR2
TR3
TR1
VDD
constant
current
source
100 µA typ.
I/O PORT
LINE
VSS
ORL / ANL / MOV
IN / MOV
MLA696

Fig.11 Standard output with switched current source.

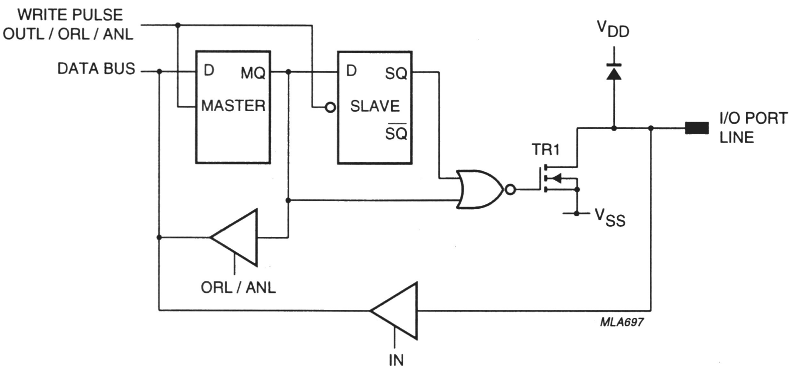

WRITE PULSE
OUTL / ORL / ANL
DATA BUS
D
MQ
MASTER
D
SQ
SLAVE
$\overline{SQ}$
V_{DD}
I/O PORT
LINE
TR1
V_{SS}
ORL / ANL
IN
MLA697

Fig.12 Open-drain output.

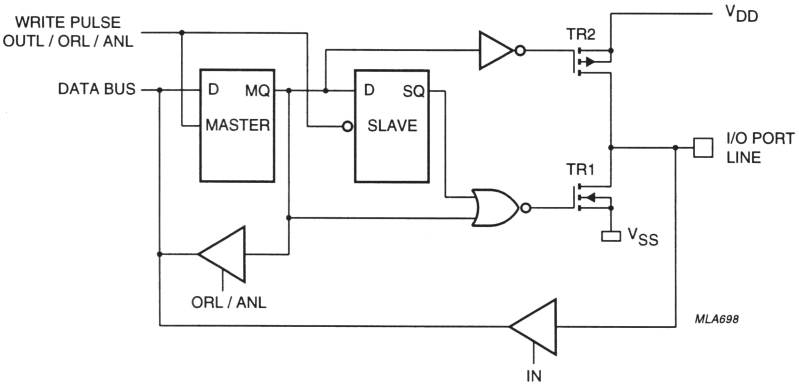

WRITE PULSE
OUTL / ORL / ANL
DATA BUS
D
MQ
MASTER
D
SQ
SLAVE
V_{DD}
TR2
I/O PORT
LINE
TR1
V_{SS}
ORL / ANL
IN
MLA698

Fig.13 Push-pull output.

6.9 Timing

Every machine cycle consists of 10 time slots which are again subdivided into 3 clock periods each (see Fig.14).

Permitted clock frequencies range from 1 MHz to a maximum, which is a function of the supply voltage. At $V_{DD} \geq 4.5$ V, a 16 MHz maximum clock frequency is guaranteed.

The clock signal may be internally generated by an on-chip oscillator. Alternatively, an external clock may be applied to pin XTAL1. In this configuration, a short circuit with an internal pull-up transistor on XTAL1 may occur while the oscillator is inhibited (see Section 6.11). Care should be taken to avoid excessive current flow.

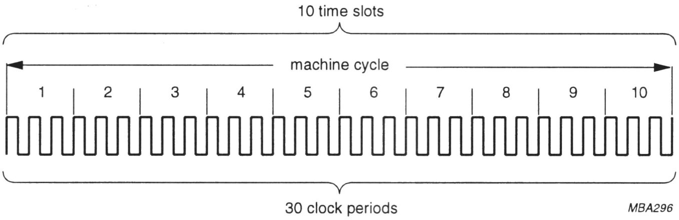


Fig.14 Timing of a machine cycle.

6.10 Reduced power modes

6.10.1 IDLE MODE

The Idle mode is very useful in low-power applications. When all computational tasks are completed, the device can be put into standby instead of into a busy waiting loop. Nevertheless, the device is on the alert and ready to respond rapidly to any interrupt.

The microcontroller enters the Idle mode via the IDLE instruction. In the Idle mode, all activity is halted except for the oscillator, the timer/event counter 1 and the serial I/O interface (if available).

The microcontroller leaves the Idle mode when an enabled interrupt occurs. The interrupt routine is executed before operation resumes with the instruction following the IDLE opcode.

For timer/event counter interrupts and derivative interrupts, termination of the Idle mode is straightforward. However, care must be taken when the Idle mode is left by the external interrupt since CE/$\overline{\text{T0}}$ is triggered on the rising edge. If CE/$\overline{\text{T0}}$ was HIGH prior to entering the Idle mode, it must be taken LOW before the positive edge can be generated. Figure 15 specifies the exact timing for leaving the Idle mode via the external interrupt CE/$\overline{\text{T0}}$.

If no interrupt is enabled, the Idle mode can only be terminated by an active signal on the RESET pin. A normal reset sequence is executed (see Fig.15).

6.10.2 STOP MODE

The Stop mode allows very low-power applications. When all computational tasks are completed, the device can be almost completely shut off by stopping its oscillator. In contrast to the Idle mode, the device is not ready to respond rapidly to any interrupt.

When the microcontroller enters the Stop mode via the STOP instruction; the oscillator is switched off. All internal states and I/O levels are maintained.

The microcontroller leaves the Stop mode by a HIGH level on CE/$\overline{\text{T0}}$ or a reset. In the latter case, a normal reset sequence is executed (see Fig.16).

In contrast to the Idle mode and the external interrupt mechanism, the microcontroller responds to a HIGH level on CE/$\overline{\text{T0}}$ rather than to a positive edge. If CE/$\overline{\text{T0}}$ is HIGH when the STOP instruction is executed, the Stop mode will not be entered.

A positive edge on CE/$\overline{\text{T0}}$ continues program execution after a 1866 clock cycle delay, which ensures proper oscillator start-up. If the external interrupt is enabled, the device executes the instruction following the STOP opcode before diverting to the interrupt routine. If the external interrupt is disabled, program execution continues with the instructions following the STOP opcode (see Fig.16).

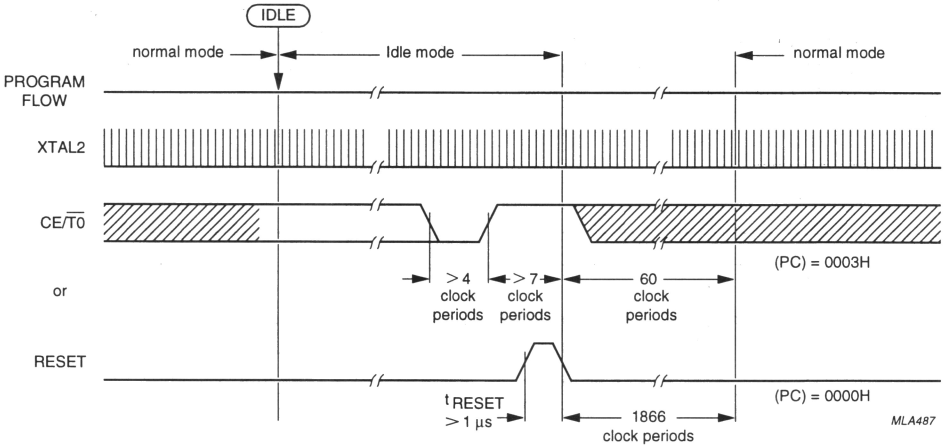

IDLE
normal mode
Idle mode
normal mode
PROGRAM FLOW
XTAL2
CE/$\overline{T0}$
or
RESET
> 4 clock periods
> 7 clock periods
60 clock periods
(PC) = 0003H
tRESET > 1 μs
1866 clock periods
(PC) = 0000H
MLA487

Fig.15 Entering and leaving the Idle mode.

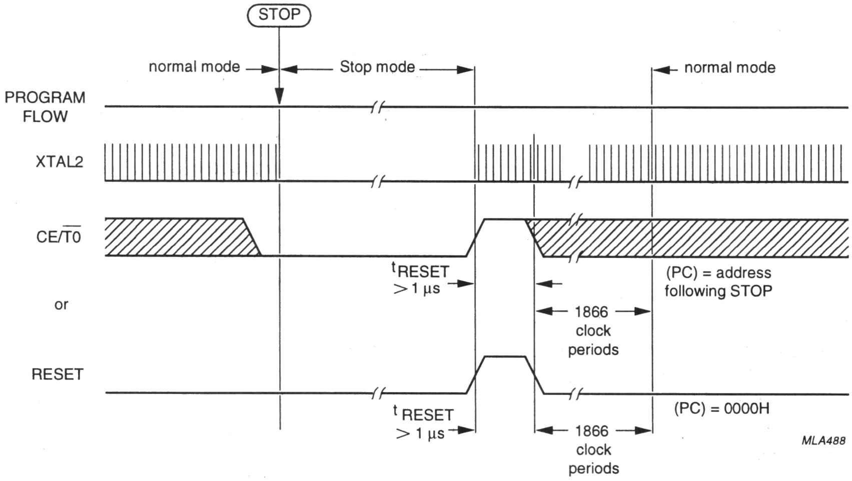

STOP
normal mode
Stop mode
normal mode
PROGRAM FLOW
XTAL2
CE/$\overline{T0}$
or
RESET
tRESET > 1 μs
1866 clock periods
(PC) = address following STOP
tRESET > 1 μs
1866 clock periods
(PC) = 0000H
MLA488

Fig.16 Entering and leaving the Stop mode.

6.11 Oscillator

The on-chip oscillator basically consists of an inverter stage which includes a feedback resistor and load capacitors (see Fig.17). In most applications, a quartz crystal will be connected between XTAL1 and XTAL2. Alternatively, a ceramic resonator or an inductor may be used as a timing element.

When the supply voltage drops below the power-on reference level, the oscillator is inhibited. The internal oscillator can also be inhibited by the STOP instruction under software control (see Section 6.10.2).

The transconductance (g_m) of the inverter stage can be mask-programmed, thereby optimizing the oscillator for a specific frequency and resonator.

Three standard transconductance options, referred to as LOW, MEDIUM and HIGH, can be specified by the user depending on the device chosen.

With $C_1 = C_2 = 10$ pF on-chip, external capacitors are not required for quartz oscillators. However, for adequate frequency stability, PXE resonators need external capacitors in the order of the static resonator capacitance C_0, such as external $C_1 = C_2 = 30$ to 100 pF.

Oscillator start-up time depends mainly on the external timing element. The start-up time of a quartz crystal is several milliseconds because of the narrow crystal bandwidth. For proper oscillator start-up, the transconductance (g_m) of the inverter stage must fulfil relationship (1) and (2); shown below.

$$g_m > 4.2\left[R_X\omega^2(C_L + C_0 + C_F)^2 + \frac{1}{R_P}\right] \qquad (1)$$

$$g_m < \frac{C1 \times C2}{\left[R_X(C_0 + C_F)^2 + \frac{1}{\omega^2 R_P}\right]} \qquad (2)$$

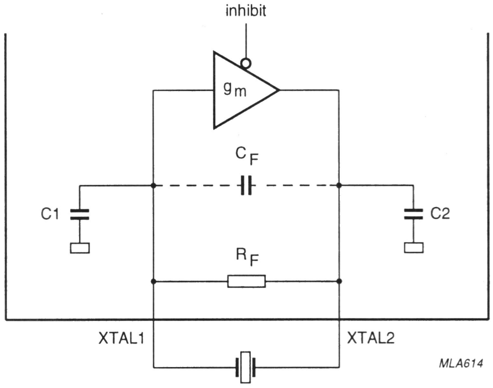


Fig.17 Oscillator with integrated elements.

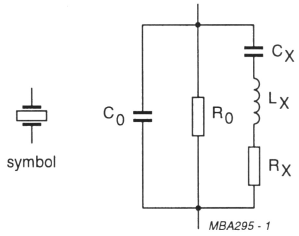


Fig.18 Crystal unit equivalent circuit.

Table 3 Notation to relationship (see Figs 17 and 18)

SYMBOL	DEFINITION
R_X	resonator series resistance
C_0	static resonator capacitance
R_0	resonator loss resistance
R_P	R_0 // R_F
R_F	feedback resistor
C_L	C1 × C2/(C1 + C2) (load capacitance)
C_F	parasitic feedback capacitance (typically 2 pF on-chip, external value depends on printed-circuit board wiring)
ω	$2\pi f_{osc}$

6.12 Reset

To ensure proper start-up, the microcontroller must be initialized to a defined starting condition. The device executes the first instruction 1 866 clock cycles after the falling edge of the internal reset.

6.12.1 PASSIVE EXTERNAL RESET

A passive reset is generated by the RC circuit illustrated in Fig.19. While V_{DD} rises, the discharged C_{reset} keeps the RESET pin near the V_{DD} level. When V_{DD} crosses the power-on reference level (V_{POR}) the Power-on-reset circuit generates a reset pulse of approximately 50 μs. This pulse is without effect since it feeds into the reset signal forced by the pulse on the RESET pin.

The f_{xtal} dependent minimum V_{DD} must be reached before the voltage on RESET drops below $V_{IH} = 0.7V_{DD}$. This translates into a lower bound for $C_{reset}R_{reset}$ equal to twice the rise time of V_{DD} (for linearly rising V_{DD}) or eight times the time constant of V_{DD} (for exponentially rising V_{DD}). The internal diode rapidly discharges C_{reset} when V_{DD} falls off, ensuring reliable reset even after short interruptions of supply voltage. To avoid overload of the internal diode, an external diode should be added in parallel if $C_{reset} > 2.2$ μF.

6.12.2 ACTIVE EXTERNAL RESET

An active reset can be generated by driving the RESET pin HIGH from an external logic device. Such an active reset pulse should not fall off before V_{DD} has reached its f_{xtal} dependent minimum operating value.

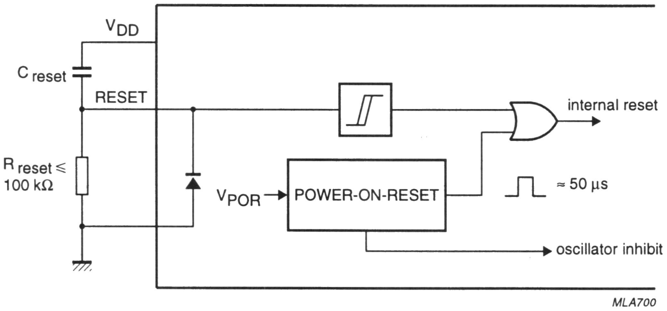


Fig.19 Passive external Power-on-reset.

6.12.3 INTERNAL RESET

In systems where V_{DD} reaches its f_{xtal} dependent minimum operating value before the clock f_{xtal} is applied, reset can be performed without external components. This condition is generally fulfilled with quartz and PXE resonators since oscillator start-up takes several milliseconds. Besides, rapid power-up is usually available in battery-powered systems.

If the internal Power-on-reset is used the RESET pin should be connected to V_{SS}. When V_{DD} increases above the power-on reference level V_{POR}, the Power-on-reset circuit generates a reset pulse of approximately 50 µs.

This pulse guarantees proper initialization under the conditions defined above.

The power-on reference level V_{POR} is a mask option. The user can select a reference voltage between 1.2 V and 3.6 V in discrete steps of 100 mV.

The chosen V_{POR} should have sufficient margin regarding the minimum intended V_{DD}.

A mask option without an internal Power-on-reset circuit is also available. It is recommended if the user does not intend to use the internal Power-on-reset circuit. In this case, the supply current requirements in Stop mode (see Section 6.10.2) will reduce to the level of leakage currents, i.e. virtually zero at ambient temperature.

6.12.4 RESET STATE

After a reset, the device state is characterized as follows:

- Program Counter 00H
- Memory bank 00H
- Register Bank 00H - Stack Pointer 00H (location pair 8 and 9)
- All interrupts disabled
- Timer/event counter 1 stopped and cleared
- Timer prescaler modulo-32 (PS = 0)
- Timer flag cleared
- All port flip-flops set to logic 1 or logic 0 depending on the port configuration
- Idle and Stop modes cancelled.

6.13 Derivative logic

Derivative logic is provided with many members of the PCD33xxA Family. The detailed description of the derivative circuitry is given in the data sheet of the specific device. In this section, the shared principles of derivative logic are briefly reviewed.

Derivative registers are accessed over the internal bus. The derivative registers are write-only, read-only or read/write (see Fig.20). They are addressed through the derivative Address Register when the derivative input/output instructions (MOV A, Dx; MOV Dx, A; ANL Dx, A and ORL Dx, A) are executed.

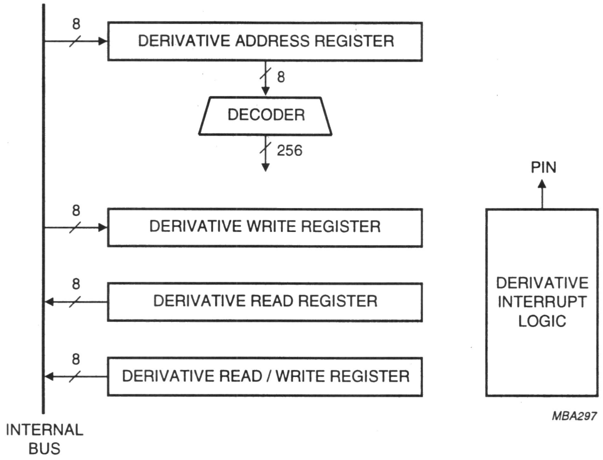

8
DERIVATIVE ADDRESS REGISTER
8
DECODER
256
8
DERIVATIVE WRITE REGISTER
8
DERIVATIVE READ REGISTER
8
DERIVATIVE READ / WRITE REGISTER
PIN
DERIVATIVE INTERRUPT LOGIC
MBA297
INTERNAL BUS

Fig.20 Block diagram of derivative logic.

Table 4 Summary of configurations

FEATURE	CONFIGURATION	DESCRIPTION
ROM	any mix of instructions	program; size restricted by ROM size (see Tables 5 and 6)
Ports	configuration 1	standard output (see Fig.11)
	configuration 2	open-drain output (see Fig.12)
	configuration 3	push-pull output (see Fig.13)
	set	flip-flop at logic 1 after reset
	reset	flip-flop at logic 0 after reset
Power-on reference	V_{POR}	1.2 to 3.6 V in increments of 100 mV; with ±500 mV accuracy
Oscillator	g_{mL}	LOW transconductance
	g_{mM}	MEDIUM transconductance
	g_{mH}	HIGH transconductance

7 INSTRUCTION SET

The PCD33xxA instruction set consists of over 100 one and two-byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256-byte page require only a single-byte address. Table 6 lists the symbols that are used in Table 5 and the Instruction map is shown in Section 7.1.

Table 5 PCD33xxA Family instruction set

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Accumulator					
ADD A, Rr(1)	6<8 + r>	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0 to 7
ADD A, @Rr(1)	6r	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((Rr))	r = 0, 1
ADD A, #data(1)	03 data	2/2	Add immediate data to A	(A)←(A) + data	
ADDC A, Rr(1)	7<8 + r>	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0 to 7
ADDC A, @Rr(1)	7r	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((Rr)) + (C)	r = 0, 1
ADDC A, #data(1)	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)	
ANL A, Rr	5<8 + r>	1/1	AND Rr with A	(A)←(A) AND (Rr)	r = 0 to 7
ANL A, @Rr	5r	1/1	AND RAM data addressed by Rr, with A	(A)←(A) AND ((Rr))	r = 0, 1
ANL A, #data	53 data	2/2	AND immediate data with A	(A)←(A) AND data	
ORL A, Rr	4<8 + r>	1/1	OR Rr with A	(A)←(A) OR (Rr)	r = 0 to 7
ORL A, @Rr	4r	1/1	OR RAM data, addressed by Rr, with A	(A)←(A) OR ((Rr))	r = 0, 1
ORL A, #data	43 data	2/2	OR immediate data with A	(A)←(A) OR data)	
XRL A, Rr	D<8 + r>	1/1	XOR Rr with A	(A)←(A) XOR (Rr)	r = 0 to 7
XRL A, @Rr	Dr	1/1	XOR RAM data, addressed by Rr, with A	(A)←(A) XOR ((Rr))	r = 0, 1
XRL A, #data	D3 data	2/2	XOR immediate data with A	(A)←(A) XOR data)	
INC A	17	1/1	Increment A by 1	(A)←(A) + 1	
DEC A	07	1/1	Decrement A by 1	(A)←(A) – 1	
CLR A	27	1/1	Clear A to zero	(A)←0	
CPL A	37	1/1	One's complement A	(A)←NOT(A)	
RL A	E7	1/1	Rotate A left	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(A_7)$	n = 0 to 6
RLC A(2)	F7	1/1	Rotate A left through carry	$(A_{n+1})\leftarrow(A_n)$, $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0 to 6
RR A	77	1/1	Rotate A right	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(A_0)$	n = 0 to 6
RRC A(2)	67	1/1	Rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$, $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0 to 6
DA A(2)	57	1/1	Decimal adjust A	(A)←(A) + 06H if AC = 1 or $(A_{0-3})>9$; (A)←(A) + 60H if $(A_{4-7})>9$	
SWAP A(2)	47	1/1	Swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Data moves					
MOV A, Rr	F<8 + r>	1/1	Move register contents to A	(A)←(Rr)	r = 0 to 7
MOV A, @Rr	Fr	1/1	Move RAM data addressed by Rr, to A	(A)←((Rr))	r = 0, 1
MOV A, #data	23 data	2/2	Move immediate data to A	(A)←data	
MOV Rr, A	A<8 + r>	1/1	Move Accumulator contents to register	(Rr)←(A)	r = 0 to 7
MOV@Rr, A	Ar	1/1	Move Accumulator contents to RAM location addressed by Rr	((Rr))←(A)	r = 0, 1
MOV Rr, #data	B<8 + r> data	2/2	Move immediate data to Rr	(Rr)←data	r = 0 to 7
MOV @Rr, #data	Br data	2/2	Move immediate data to RAM location addressed by Rr	((R0))←data	r = 0, 1
XCH A, Rr	2<8 + r>	1/1	Exchange A contents with Rr	(A)↔(Rr)	r = 0 to 7
XCH A, @Rr	2r	1/1	Exchange Accumulator contents with RAM data addressed by Rr	(A)↔((Rr))	r = 0, 1
XCHD A, @Rr	3r	1/1	Exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0\text{-}3})$↔$((Rr_{0\text{-}3}))$	r = 0, 1
MOV A, PSW	C7	1/1	Move PSW contents to Accumulator	(A)←(PSW)	
MOV PSW, A(3)	D7	1/1	Move Accumulator bit 3 to PSW_3 (PS)	(PS)←(A_3)	
MOV P A, @A	A3	1/2	Move indirectly addressed data in current page to A	$(PC_{0\text{-}7})$←(A), (A)←((PC))	
Carry flag					
CLR C(2)	97	1/1	Clear carry bit	(C)←0	
CPL C(2)	A7	1/1	Complement carry bit	(C)←NOT(C)	
Register					
INC Rr	1<8 + r>	1/1	Increment register by 1	(Rr)←(Rr) + 1	r = 0 to 7
INC @Rr	1r	1/1	Increment RAM data, addressed by Rr, by 1	((Rr))←((Rr)) + 1	r = 0,1
DEC Rr	C<8 + r>	1/1	Decrement register by 1	(Rr)←(Rr) – 1	r = 0 to 7
DEC @Rr	Cr	1/1	Decrement RAM data addressed by Rr, by 1	((Rr))←((Rr)) – 1	r = 0, 1

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Branch					
JMP addr	<2n>4 addr	2/2	Unconditional jump within a 2 kbyte bank	$(PC_{8-10}) \leftarrow n$ $(PC_{0-7}) \leftarrow addr$ $(PC_{11-12}) \leftarrow (MBFF0\text{-}1)$	n = 0 to 7
JMPP @A	B3	1/2	Indirect jump within a page	$(PC_{0-7}) \leftarrow ((A))$	
DJZN Rr, addr	E<8 + r> addr	2/2	Decrement Rr by 1 and jump if not zero to addr	$(Rr) \leftarrow (Rr) - 1$; if (Rr) not zero, then $(PC_{0-7}) \leftarrow addr$	r = 0 to 7
DJNZ @Rr, addr	Er	2/2	Decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	$((Rr)) \leftarrow ((Rr)) - 1$; if ((Rr)) not zero, then $(PC_{0-7}) \leftarrow addr$	r = 0 to 1
JBb addr	<2b + 1> 2 addr	2/2	Jump to addr if Accumulator bit b = 1	If $(A_b) = 1$, then $(PC_{0-7}) \leftarrow addr$	b = 0 to 7
JC addr	F6 addr	2/2	Jump to addr if C = 1	If (C) = 1, then $(PC_{0-7}) \leftarrow addr$	
JNC addr	E6 addr	2/2	Jump to addr if C = 0	If (C) = 0, then $(PC_{0-7}) \leftarrow addr$	
JZ addr	C6 addr	2/2	Jump to addr if A = 0	If (A) = 0, $(PC_{0-7}) \leftarrow addr$	
JNZ addr	96 addr	2/2	Jump to addr if A is NOT zero	If $(A) \neq 0$, then $(PC_{0-7}) \leftarrow addr$	
JT0 addr	36 addr	2/2	Jump to addr if T0 = 0	If T0 = 0, then $(PC_{0-7}) \leftarrow addr$	
JNT0 addr	26 addr	2/2	Jump to addr if T0 = 1	If T0 = 1, then $(PC_{0-7}) \leftarrow addr$	
JT1 addr	56 addr	2/2	Jump to addr if T1 = 1	If T1 = 1, then $(PC_{0-7}) \leftarrow addr$	
JNT1 addr	46 addr	2/2	Jump to addr if T1 = 0	If T0 = 0, then $(PC_{0-7}) \leftarrow addr$	
JTF addr(4)	16 addr	2/2	Jump to addr if Timer Flag = 1	If TF = 1, then $(PC_{0-7}) \leftarrow addr$	
JNTF addr(4)	06 addr	2/2	Jump to addr if Timer Flag = 0	If T0 = 0, then $(PC_{0-7}) \leftarrow addr$	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Timer/event counter					
MOV A,T	42	1/1	Move timer/event counter contents to A	(A)←(T)	
MOV T, A	62	1/1	Move A contents to timer/event counter	(T)←(A)	
STRT CNT	45	1/1	Start event counter		
STRT T	55	1/1	Start timer		
STOP TCNT	65	1/1	Stop timer/event counter		
EN TCNTI	25	1/1	Enable timer/event counter interrupt		
DIS TCNTI	35	1/1	Disable timer/event counter interrupt		
Control					
EN I	05	1/1	Enable external (chip enable) interrupt		
DIS I	15	1/1	Disable external (chip enable) interrupt		
SEL RB0(5)	C5	1/1	Select Register Bank 0	(RBS)←0	
SEL RB1(5)	D5	1/1	Select Register Bank 1	(RBS)←1	
SEL MB0(9)	E5	1/1	Select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
SEL MB1(9)	F5	1/1	Select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
SEL MB2(9)	A5	1/1	Select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
SEL MB3(9)	B5	1/1	Select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
STOP	22	1/1	Enter Stop mode		
IDLE	01	1/1	Enter Idle mode		
NOP	00	1/1	No operation		
Subroutine					
CALL addr(6)	<2n + 1> 4addr	2/2	Jump to subroutine	((SP))←(PC) ($PSW_{4,6,7}$), (SP)←(SP) + 1, (PC_{8-10})←n, (PC_{0-7})←addr, (PC_{11-12}) ←(MBFF0-1)	n = 0 to 7
RET(6)	83	1/2	Return from subroutine	(SP)←(SP) − 1, (PC)←((SP))	
RETR(6)	93	1/2	Return from interrupt and restore bits 4, 6 and 7 of PSW	(SP)←(SP) − 1, ($PSW_{4,6,7}$) + (PC)←((SP))	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION	NOTES
Parallel input/output					
IN A, P0	08	1/2	Input Port 0 data to Accumulator	(A)←(P0)	
IN A, P1	09	1/2	Input Port 1 data to Accumulator	(A)←(P1)	
IN A, P2(7)	0A	1/2	Input Port 2 data to Accumulator	(A)←(P2)	
OUTL P0, A	38	1/2	Output A data to Port 0	(P0)←(A)	
OUTL P1, A	39	1/2	Output A data to Port 1	(P1)←(A)	
OUTL P2, A	3A	1/2	Output A data to Port 2	(P2)←(A)	
ANL P0, #data	98 data	2/2	AND Port 0 data with immediate data	(P0)←(P0) AND data	
ANL P1, #data	99 data	2/2	AND Port 1 data with immediate data	(P1)←(P1) AND data	
ANL P2, #data	9A data	2/2	AND Port 2 data with immediate data	(P2)←(P2) AND data	
ORL P0, #data	88 data	2/2	OR Port 0 data with immediate data	(P0)←(P0) OR data	
ORL P1, #data	89 data	2/2	OR Port 1 data with immediate data	(P1)←(P1) OR data	
ORL P2, #data	8A data	2/2	OR Port 2 data with immediate data	(P2)←(P2) OR data	
Derivative input/output					
MOV A, Dx(8)	8C direct	2/2	Move derivative register contents to A	(A)←(Dx)	x = 0 to 255
MOV Dx, A(8)	8D direct	2/2	Move A contents to derivative register	(Dx)←(A)	x = 0 to 255
ANL Dx, A(8)	8E direct	2/2	AND derivative register with A	(Dx)←(Dx) AND (A)	x = 0 to 255
ORL Dx, A(8)	8F direct	2/2	OR derivative register with A	(Dx)←(Dx) OR (A)	x = 0 to 255
EN SI	85	1/1	Enable derivative interrupt		
DIS SI	95	1/1	Disable derivative interrupt		

Notes to Table 5

1. PSW CY, AC affected.
2. PSW CY affected.
3. PSW PS affected.
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected.
6. PSW SP_0, SP_1 and SP_2, affected.
7. (A) = 0000, P2.3, P2.2, P2.1 and P2.0.
8. For more information on the derivative I/O instructions of a particular microcontroller, consult the specific microcontroller data sheet.
9. SEL MB instructions may not be used within interrupt routines.

Table 6 Definitions of symbols used in Table 5

SYMBOL	DESCRIPTION
A	Accumulator
AC	auxiliary (half) carry
addr	program memory address
Bb	bit designation (b = 0 to 7)
CE/$\overline{\text{T0}}$	CE/$\overline{\text{T0}}$ input
CY	carry bit
Dx	mnemonic derivative register
data	8-bit number or expression
MB0	program memory bank 0
MB1	program memory bank 1
MB2	program memory bank 2
MB3	program memory bank 3
MBFF0	memory bank flip-flop 0
MBFF1	memory bank flip-flop 1
PC	Program Counter
PS	timer prescaler select
PSW	Program Status Word
RB0	Register Bank 0
RB1	Register Bank 1
RBS	Register Bank Select
Rr	register designation (r = 0 to 7)
SPn	Stack Pointer (n = 0, 1 or 2)
T	Timer 1
T1	T1 input
TF	Timer Flag
x	derivative register address (x = 0 to 255)
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with
#	immediate data prefix
@	indirect address prefix
*	hexadecimal; 8...F selects R0...R7
&	hexadecimal; 0, 2, 4, 6, 8, A, C, E selects page 0...7 in JMP, i.e. $(PC_{8\text{-}10}) \leftarrow \&_{1\text{-}3}$
%	hexadecimal; 1, 3, 5, 7, 9, B, D, F selects page 0...7 in CALL, i.e. $(PC_{8\text{-}10}) \leftarrow \&_{1\text{-}3}$ selects bit b = 0...7 in JBb, i.e. $b = \&_{1\text{-}3}$

7.1 Instruction map

first hexadecimal character of opcode second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	1	2					
1	INC @ Rr 0	1	JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	1	2	3	4	5	6	7
2	XCH A, @Rr 0	1	STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	1	2	3	4	5	6	7
3	XCHD A, @Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	1	2					
4	ORL A, @Rr 0	1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	1	2	3	4	5	6	7
5	ANL A, @Rr 0	1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	1	2	3	4	5	6	7
6	ADD A, @Rr 0	1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	1	2	3	4	5	6	7
7	ADDC A, @Rr 0	1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,#data 0	1	2		MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0	1	2					
A	MOV @ Rr,A 0	1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	1	2	3	4	5	6	7
B	MOV @Rr, #data 0	1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0	1	2	3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0	1	2	3	4	5	6	7
D	XRL A, @Rr 0	1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0	1	2	3	4	5	6	7
E	DJNZ @ Rr,addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr,addr 0	1	2	3	4	5	6	7
F	MOV A, @Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	1	2	3	4	5	6	7

MGD566

8-bit microcontrollers with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3755x

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FREQUENCY GENERATOR
6.1 Frequency generator derivative registers
6.2 Melody output (P1.7/MDY)
6.3 Frequency registers
6.4 DTMF frequencies
6.5 Modem frequencies
6.6 Musical scale frequencies
7 EEPROM AND TIMER 2 ORGANIZATION
7.1 EEPROM registers
7.2 EEPROM latches
7.3 EEPROM flags
7.4 EEPROM macros
7.5 EEPROM access
7.6 Timer 2
8 DERIVATIVE INTERRUPTS
9 TIMING
10 RESET
11 IDLE MODE
12 STOP MODE
13 INSTRUCTION SET RESTRICTIONS
14 OVERVIEW OF FAMILY MEMBERS
15 OTP PROGRAMMING
16 SUMMARY OF DERIVATIVE REGISTERS
17 LIMITING VALUES
18 HANDLING
19 DC CHARACTERISTICS
20 AC CHARACTERISTICS
21 PACKAGE OUTLINES
22 SOLDERING
22.1 Reflow soldering
22.2 Wave soldering
22.3 DIP
22.4 Repairing soldered joints
23 DEFINITIONS
24 LIFE SUPPORT APPLICATIONS

8-bit microcontrollers with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3755x

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; in a single 28-lead or 32-lead package
- 8 kbytes user-programmable ROM (One-Time Programmable)
- 128 bytes RAM
- 128 bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- 3 single-level vectored interrupts:
  - external
  - Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating temperature: –25 to 70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3755x comprising PCD3755A and PCD3755E are One-Time Programmable (OTP) microcontrollers oriented towards telephony applications.The different types differ in the Port and Power-on-reset configurations. All types include an on-chip dual tone multifrequency (DTMF) generator.
In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation.

The PCD3755x also incorporate 128 bytes of EEPROM. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.
The Power-on-reset circuitry is extra accurate to accommodate parallel telephones and fax equipment.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family. This data sheet details the specific properties of the PCD3755x. The shared characteristics of the PCD33xxA family of microcontrollers are described in the:

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3755AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3755EP			
PCD3755AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3755ET			
PCD3755AH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD3755EH			

4 BLOCK DIAGRAM

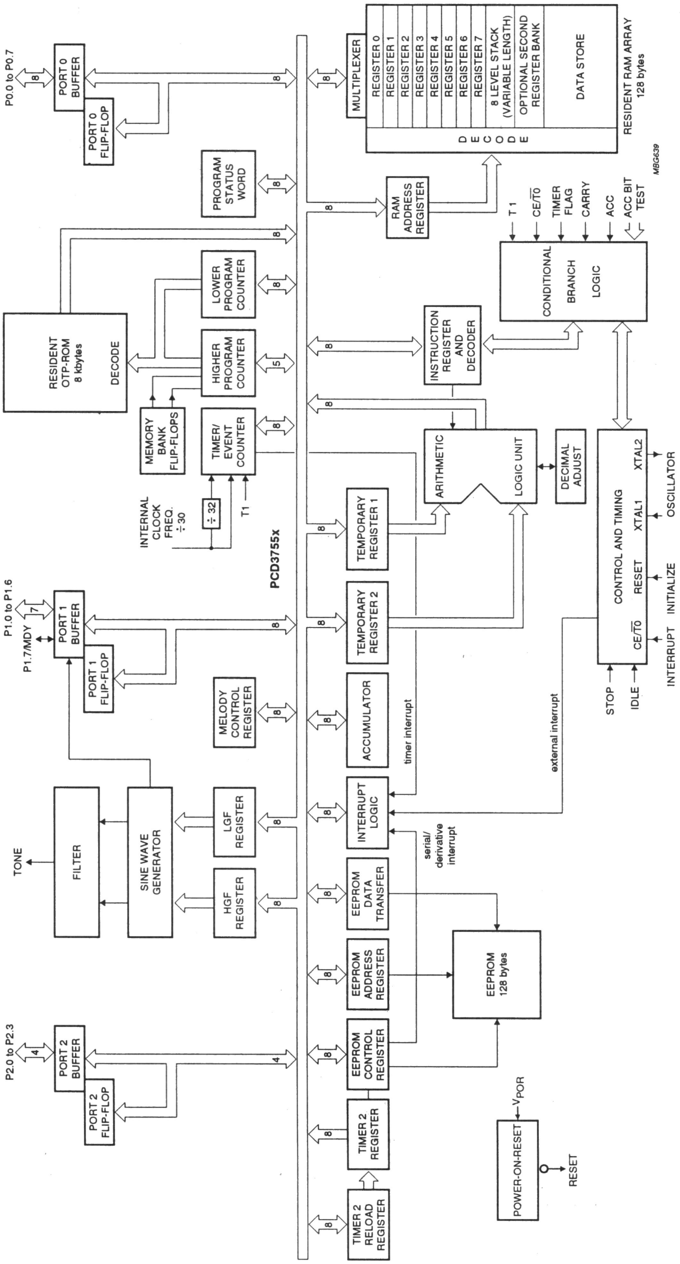

P0.0 to P0.7
8
PORT 0 BUFFER
PORT 0 FLIP-FLOP
8
PROGRAM STATUS WORD
8
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
DECODE
RESIDENT RAM ARRAY 128 bytes
MBG639
8
RAM ADDRESS REGISTER
T1
CE/T0
TIMER FLAG
CARRY
ACC
ACC BIT TEST
CONDITIONAL BRANCH LOGIC
8
RESIDENT OTP-ROM 8 kbytes
DECODE
LOWER PROGRAM COUNTER
8
HIGHER PROGRAM COUNTER
5
MEMORY BANK FLIP-FLOPS
TIMER/ EVENT COUNTER
8
INTERNAL CLOCK FREQ. ÷ 30
÷ 32
T1
8
INSTRUCTION REGISTER AND DECODER
8
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
CONTROL AND TIMING
XTAL2
XTAL1
OSCILLATOR
RESET
INITIALIZE
CE/T0
INTERRUPT
STOP
IDLE
PCD3755x
8
TEMPORARY REGISTER 1
P1.0 to P1.6
7
P1.7/MDY
PORT 1 BUFFER
PORT 1 FLIP-FLOP
8
8
TEMPORARY REGISTER 2
MELODY CONTROL REGISTER
8
8
ACCUMULATOR
timer interrupt
external interrupt
8
INTERRUPT LOGIC
serial/ derivative interrupt
TONE
FILTER
SINE WAVE GENERATOR
LGF REGISTER
8
HGF REGISTER
8
8
EEPROM DATA TRANSFER
8
EEPROM ADDRESS REGISTER
EEPROM 128 bytes
P2.0 to P2.3
4
PORT 2 BUFFER
PORT 2 FLIP-FLOP
4
8
EEPROM CONTROL REGISTER
8
TIMER 2 REGISTER
VPOR
POWER-ON-RESET
RESET
8
TIMER 2 RELOAD REGISTER

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

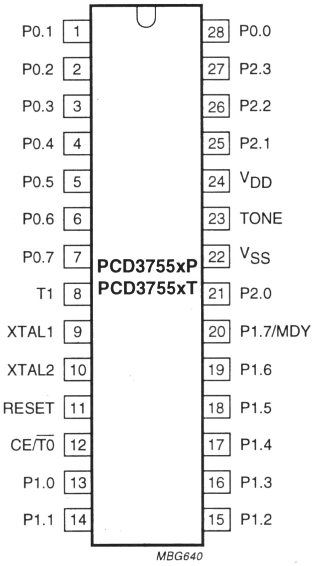

P0.1
1
P0.2
2
P0.3
3
P0.4
4
P0.5
5
P0.6
6
P0.7
7
T1
8
XTAL1
9
XTAL2
10
RESET
11
CE/$\overline{T0}$
12
P1.0
13
P1.1
14
28
P0.0
27
P2.3
26
P2.2
25
P2.1
24
V_{DD}
23
TONE
22
V_{SS}
21
P2.0
20
P1.7/MDY
19
P1.6
18
P1.5
17
P1.4
16
P1.3
15
P1.2
PCD3755xP
PCD3755xT
MBG640

Fig.2 Pin configuration (SOT117-1 and SOT136-1).

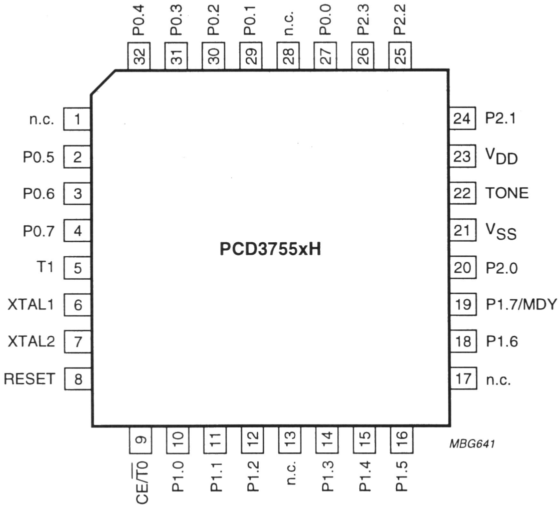

P0.4
32
P0.3
31
P0.2
30
P0.1
29
n.c.
28
P0.0
27
P2.3
26
P2.2
25
n.c.
1
P0.5
2
P0.6
3
P0.7
4
T1
5
XTAL1
6
XTAL2
7
RESET
8
24
P2.1
23
V_{DD}
22
TONE
21
V_{SS}
20
P2.0
19
P1.7/MDY
18
P1.6
17
n.c.
PCD3755xH
9
CE/$\overline{T0}$
10
P1.0
11
P1.1
12
P1.2
13
n.c.
14
P1.3
15
P1.4
16
P1.5
MBG641

Fig.3 Pin configuration (SOT358-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines
T1	8	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{\text{T0}}$	12	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	20	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	21, 25 to 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

Table 2 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
T1	5	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	crystal oscillator or external clock input
XTAL2	7	crystal oscillator output
RESET	8	reset input
CE/$\overline{\text{T0}}$	9	Chip Enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	19	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	20, 24 to 26	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	21	ground
TONE	22	DTMF output
V_{DD}	23	positive supply voltage
P0.0 to P0.7	27, 29 to 32, 2 to 4	Port 0: 8 quasi-bidirectional I/O lines
n.c.	1, 13, 17, 28	not connected

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the P1.7/MDY output.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

In case no tones are generated the TONE output is in tri-state mode.

6.1 Frequency generator derivative registers

6.1.1 HIGH AND LOW GROUP FREQUENCY REGISTERS

Table 3 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers HGF (High Group Frequency) and LGF (Low Group Frequency); access type W.

Table 3 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
11H	HGF	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 MELODY CONTROL REGISTER (MDYCON)

MDYCON is a R/W register.

Table 4 Melody Control Register (address 13H)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EMO

Table 5 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

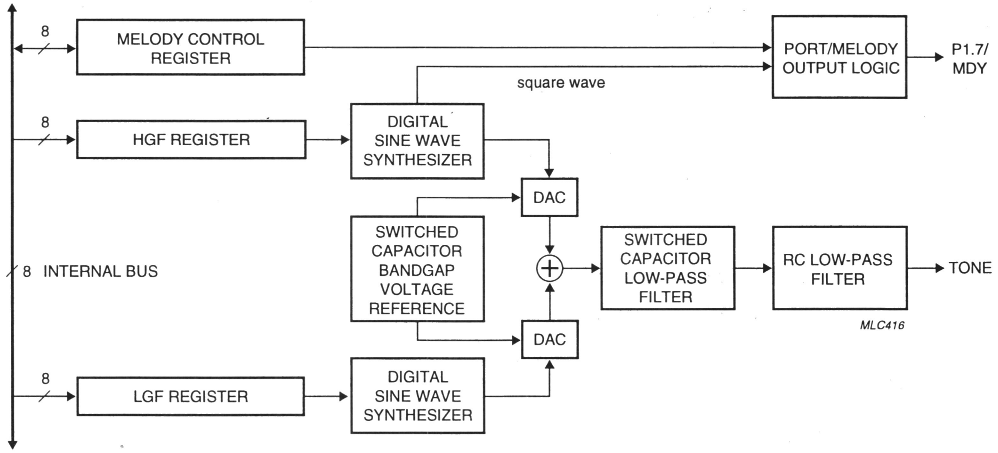

8
MELODY CONTROL REGISTER
PORT/MELODY OUTPUT LOGIC
P1.7/ MDY
square wave
8
HGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER
DAC
SWITCHED CAPACITOR BANDGAP VOLTAGE REFERENCE
8 INTERNAL BUS
SWITCHED CAPACITOR LOW-PASS FILTER
RC LOW-PASS FILTER
TONE
MLC416
DAC
8
LGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER

Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the limitation $60 \le x \le 255$ is relaxed to $2 \le x \le 255$ in this application; x = decimal value of the HGF register contents. Due to the low-pass filters, the simultaneous signal on the TONE output is not useful for $x < 60$.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY; see Chapter 14, Table 24.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value ‘x’ held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x + 2)\,]};\ \text{where } 60 \le x \le 255.$$

The frequency limitation given by $x \ge 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 6.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 7.

Table 6 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 7 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 8 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low group frequency generation.

Table 8 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980(1)	978.82	−0.12	−1.18
82	1180(1)	1179.03	−0.08	−0.97
8F	1070(2)	1073.33	0.31	3.33
79	1270(2)	1265.30	−0.37	−4.70
80	1200(3)	1197.17	−0.24	−2.83
45	2200(3)	2192.01	−0.36	−7.99
76	1300(4)	1296.94	−0.24	−3.06
48	2100(4)	2103.14	0.15	3.14
5C	1650(1)	1655.66	0.34	5.66
52	1850(1)	1852.77	0.15	2.77
4B	2025(2)	2021.20	−0.19	−3.80
44	2225(2)	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 9). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low group frequency generation.

Table 9 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD(1)	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3755x types have 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for.battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCD3755x.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes.
Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

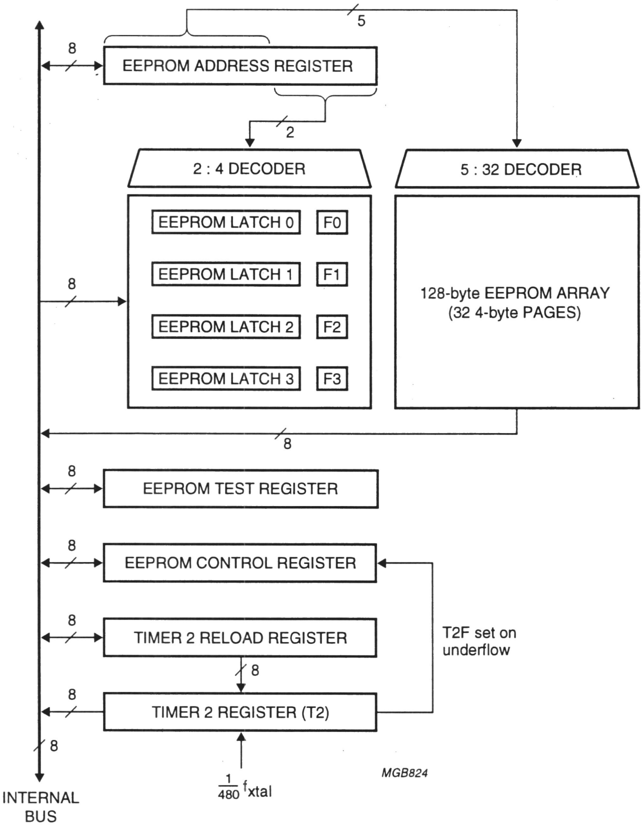

5
8
EEPROM ADDRESS REGISTER
2
2 : 4 DECODER
5 : 32 DECODER
EEPROM LATCH 0
F0
EEPROM LATCH 1
F1
EEPROM LATCH 2
F2
EEPROM LATCH 3
F3
8
128-byte EEPROM ARRAY
(32 4-byte PAGES)
8
8
EEPROM TEST REGISTER
8
EEPROM CONTROL REGISTER
8
TIMER 2 RELOAD REGISTER
T2F set on underflow
8
8
TIMER 2 REGISTER (T2)
8
INTERNAL BUS
$\frac{1}{480} f_{xtal}$
MGB824

Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. The register access type is R/W.

Table 10 EEPROM Control Register (address 04H)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 11 Description of EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 12.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 12 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed. The register access type is R/W.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 13 EEPROM Address Register (address 01H)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 14 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 12) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 15 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 16 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 23). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 10.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 13), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 17).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 12) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 18.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 17 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 18 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 19 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page.

To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 20.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 20 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM Latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 21 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 22 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $\frac{1}{480} \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $\frac{1}{480} \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 23 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 23 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE(1) (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times \frac{1}{480} \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 26) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 10 and 11).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

9 TIMING

Although the PCD3755x types operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33xxA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

13 INSTRUCTION SET RESTRICTIONS

RAM space is restricted to 128 bytes, care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF FAMILY MEMBERS

Table 24 Port and Power-on-reset configuration
See note 1 and 2.

TYPE	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3755A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R(3)	2S	2S	2S	2S	1.3 V
PCD3755E	1S	1S	1S	1S	1S	1S	1S	1S	2S	2S	2S	2S	2S	2S	1S	1S(3)	2S	1R	1R	1R	2.0 V

Notes

1. Port output drive: 1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* datasheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The Melody Output drive type is push-pull.

15 OTP PROGRAMMING

The programming of the PCD3755x and PCD3756x OTPs is based on the OM4260 programmer (Ceibo MP-51), available from Philips. The OM4260 works in conjunction with various adapters supporting the different package types available as listed in Table 25.

The low-voltage OTP program memory used is of Anti-Fuse-PROM type and can not be erased after programming.

Thus, the complete OTP memory cannot be tested by the factory, but only partially via a special test array.
The average expected yield is 97%.

Detailed information on the OTP programming is available in the *"PCD3755x Application Note"*, being available via your Philips Sales office.

Table 25 OTP programming overview

DEVICE	PHILIPS TYPE NUMBER	CEIBO TYPE NUMBER	SUPPORTED PACKAGE
Ceibo MP-51	OM4260	MP-51 programmer base	–
PCD3755x/56x	OM5007	PCD3755A / 56A adapter DIP	DIP28
PCD3755x/56x	OM5030	PCD3755A / 56A adapter SO	SO28
PCD3755x/56x	OM5037(1)	PCD3755A / 56A adapter QFP32	LQFP32

Note

1. As the OM5037 is only a socket converter, the OM5007 is also needed to program the PCD3755x/56x in the LQFP32 package.

16 SUMMARY OF DERIVATIVE REGISTERS

Table 26 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody Control Register (MDYCON)	0	0	0	0	0	0	0	EMO	R/W
14 to FF	not used									

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see note 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	−10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

18 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

19 DC CHARACTERISTICS

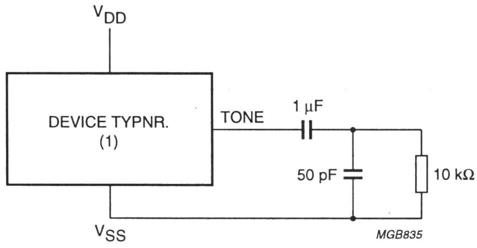
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 15 **to** 11**)**						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0;	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0;	–	0.7	1.4	mA
		V_{DD} = 3 V;	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 C; note3	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 C; note3	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	1	µA
Port outputs (see Figs 12 **to** 14**)**						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	–10	–30	–	µA
		V_{DD} = 3 V; V_O = 0 V	–	–140	–300	µA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–3.5	–	mA
Tone output (see Fig.6; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset						
V_{POR}	Power-on-reset level					
	PCD3755A		0.8	1.3	1.8	V
	PCD3755E		1.5	2.0	2.5	V

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
   a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
   b) Typical values: 25 C; crystal connected between XTAL1 and XTAL2.
3. VIL = VSS; VIH = VDD; RESET, T1 and CE/T0 at VSS; crystal connected between XTAL1 and XTAL2; pins T1 and $CE/\overline{T0}$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low group frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.



(1) Device typenr.: PCD3755x.

Fig.6 TONE output test circuit.

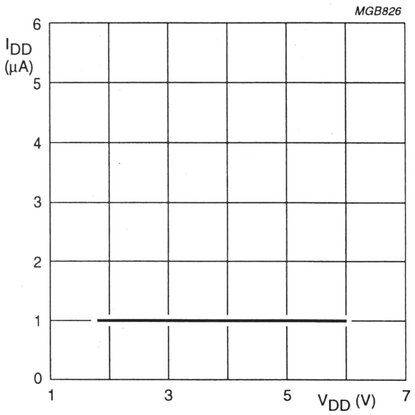
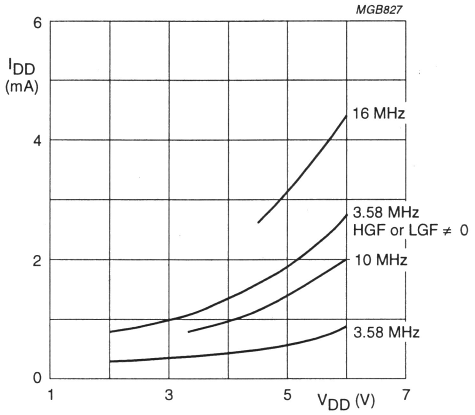
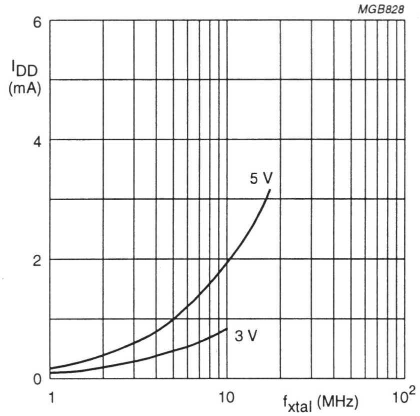


Fig.7 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



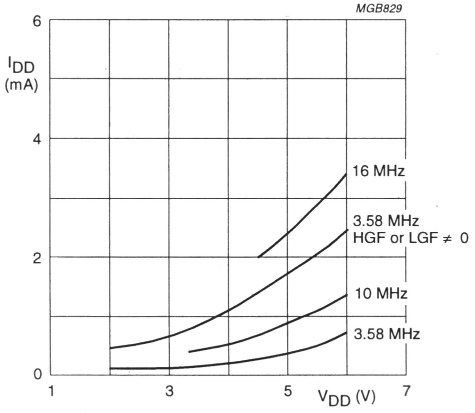
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



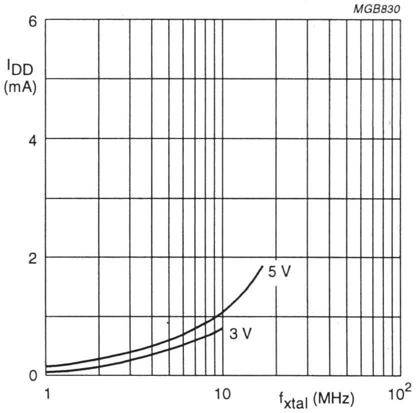
Measured with function generator on XTAL1.

Fig.9 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



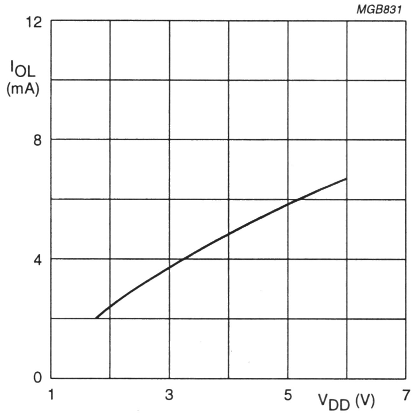
Measured with crystal between XTAL1 and XTAL2.

Fig.10 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.11 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V.

Fig.12 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

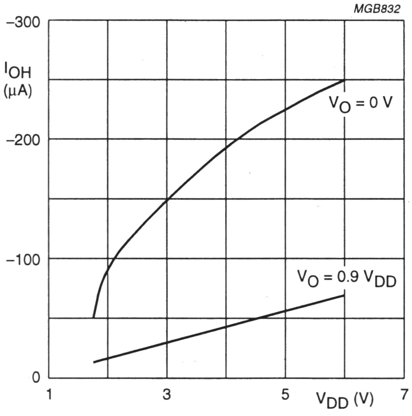
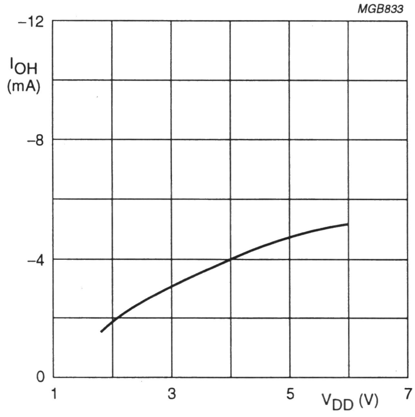


Fig.13 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.14 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

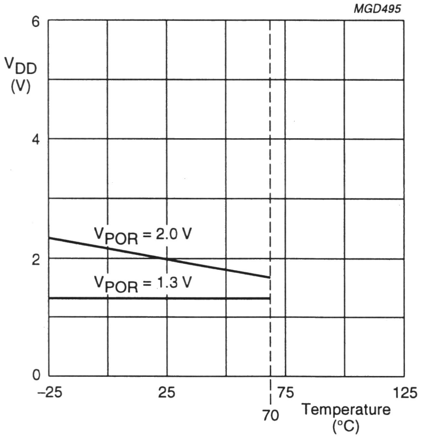


Fig.15 Typical Power-on-reset level (V_{POR}) as function of temperature.

20 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.15	1	–	16	MHz
Oscillator (see Fig.16)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

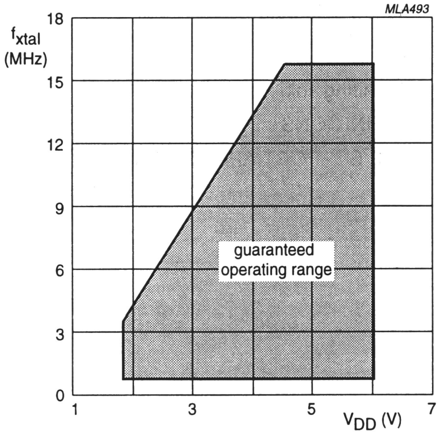


Fig.16 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

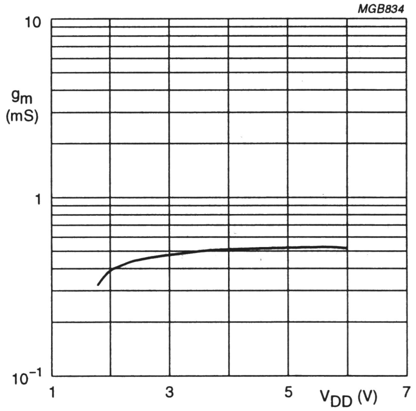


Fig.17 Typical transconductance as a function of supply voltage (V_{DD}).

8-bit microcontrollers with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3756x

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 FREQUENCY GENERATOR
6.1 Frequency generator derivative registers
6.2 Melody output (P1.7/MDY)
6.3 Frequency registers
6.4 DTMF frequencies
6.5 Modem frequencies
6.6 Musical scale frequencies
7 EEPROM AND TIMER 2 ORGANIZATION
7.1 EEPROM registers
7.2 EEPROM latches
7.3 EEPROM flags
7.4 EEPROM macros
7.5 EEPROM access
7.6 Timer 2
8 INTERRUPTS
8.1 Derivative interrupt
8.2 Port 0 Wake-up interrupts
9 TIMING
10 RESET
11 IDLE MODE
12 STOP MODE
13 INSTRUCTION SET RESTRICTIONS
14 OVERVIEW OF FAMILY MEMBERS
15 OTP PROGRAMMING
16 SUMMARY OF DERIVATIVE REGISTERS
17 LIMITING VALUES
18 HANDLING
19 DC CHARACTERISTICS
20 AC CHARACTERISTICS
21 PACKAGE OUTLINES
22 SOLDERING
22.1 Reflow soldering
22.2 Wave soldering
22.3 DIP
22.4 Repairing soldered joints
23 DEFINITIONS
24 LIFE SUPPORT APPLICATIONS

8-bit microcontrollers with DTMF generator, 8 kbytes OTP and 128 bytes EEPROM

PCD3756x

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; in a single 28-lead or 32-lead package
- 8 kbytes user-programmable ROM (One-Time Programmable)
- 128 bytes RAM
- 128 bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- 3 single-level vectored interrupts:
  - external
  - Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Wake-up via external or Port 0 interrupt
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Operating temperature: –25 to 70 °C
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3756x are One-Time Programmable (OTP) microcontrollers oriented towards telephony applications. The different types differ in the Port and Power-on-reset configurations. All types include an on-chip dual tone multifrequency (DTMF) generator. In addition to dialling, generated frequencies can be made available as square waves (P1.7/MDY) for melody generation, providing ringer operation (in which case the tone output is disabled).
A wake-up function via Port 0 interrupt facilitates keyboard interfacing.

The PCD3756x also incorporate 128 bytes of EEPROM. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family. This data sheet details the specific properties of the PCD3756x. The shared characteristics of the PCD33xxA family of microcontrollers are described in the:

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3756xP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3756xT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCD3756xH	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

4 BLOCK DIAGRAM

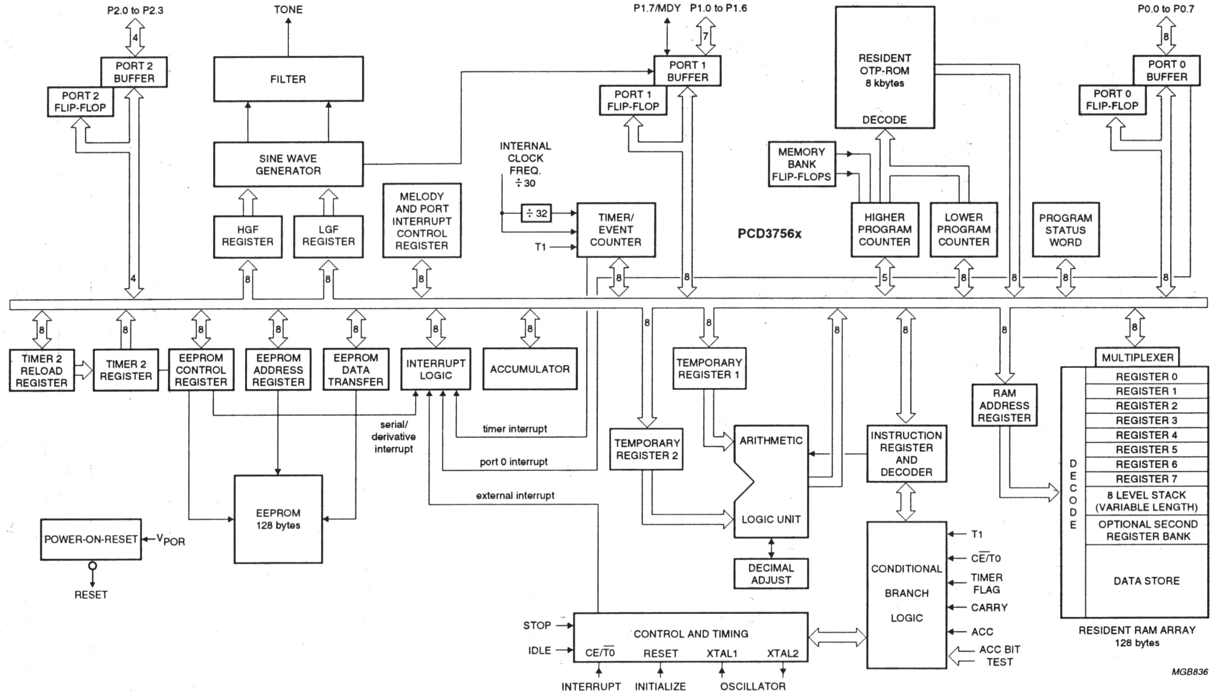

P2.0 to P2.3
4
PORT 2 BUFFER
PORT 2 FLIP-FLOP
TONE
FILTER
SINE WAVE GENERATOR
HGF REGISTER
LGF REGISTER
MELODY AND PORT INTERRUPT CONTROL REGISTER
INTERNAL CLOCK FREQ. ÷ 30
÷ 32
T1
TIMER/ EVENT COUNTER
P1.7/MDY
P1.0 to P1.6
7
PORT 1 BUFFER
PORT 1 FLIP-FLOP
PCD3756x
RESIDENT OTP-ROM 8 kbytes
DECODE
MEMORY BANK FLIP-FLOPS
HIGHER PROGRAM COUNTER
LOWER PROGRAM COUNTER
5
PROGRAM STATUS WORD
P0.0 to P0.7
8
PORT 0 BUFFER
PORT 0 FLIP-FLOP
TIMER 2 RELOAD REGISTER
TIMER 2 REGISTER
EEPROM CONTROL REGISTER
EEPROM ADDRESS REGISTER
EEPROM DATA TRANSFER
INTERRUPT LOGIC
ACCUMULATOR
serial/ derivative interrupt
timer interrupt
port 0 interrupt
external interrupt
EEPROM 128 bytes
POWER-ON-RESET
V_POR
RESET
TEMPORARY REGISTER 1
TEMPORARY REGISTER 2
ARITHMETIC
LOGIC UNIT
DECIMAL ADJUST
INSTRUCTION REGISTER AND DECODER
CONDITIONAL BRANCH LOGIC
T1
CE/T0
TIMER FLAG
CARRY
ACC
ACC BIT TEST
RAM ADDRESS REGISTER
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
DECODE
RESIDENT RAM ARRAY 128 bytes
STOP
IDLE
CONTROL AND TIMING
CE/T0
RESET
XTAL1
XTAL2
INTERRUPT
INITIALIZE
OSCILLATOR
MGB836

Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

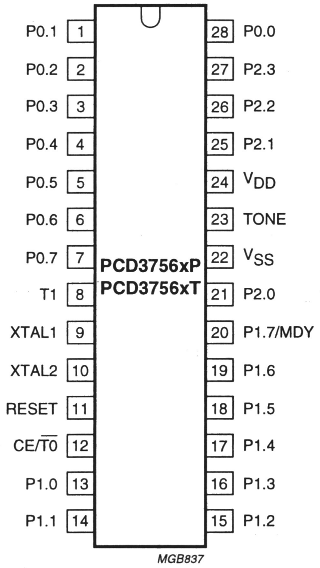

P0.1 1
P0.2 2
P0.3 3
P0.4 4
P0.5 5
P0.6 6
P0.7 7
T1 8
XTAL1 9
XTAL2 10
RESET 11
CE/$\overline{T0}$ 12
P1.0 13
P1.1 14
28 P0.0
27 P2.3
26 P2.2
25 P2.1
24 V$_{DD}$
23 TONE
22 V$_{SS}$
21 P2.0
20 P1.7/MDY
19 P1.6
18 P1.5
17 P1.4
16 P1.3
15 P1.2
PCD3756xP
PCD3756xT
MGB837

Fig.2 Pin configuration (SOT117-1 and SOT136-1).

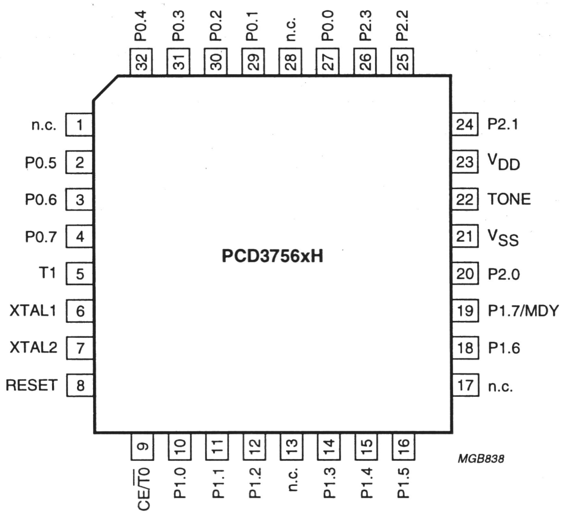

P0.4 32
P0.3 31
P0.2 30
P0.1 29
n.c. 28
P0.0 27
P2.3 26
P2.2 25
n.c. 1
P0.5 2
P0.6 3
P0.7 4
T1 5
XTAL1 6
XTAL2 7
RESET 8
24 P2.1
23 V$_{DD}$
22 TONE
21 V$_{SS}$
20 P2.0
19 P1.7/MDY
18 P1.6
17 n.c.
9 CE/$\overline{T0}$
10 P1.0
11 P1.1
12 P1.2
13 n.c.
14 P1.3
15 P1.4
16 P1.5
PCD3756xH
MGB838

Fig.3 Pin configuration (SOT358-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines or wake-up interrupts
T1	8	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{\text{T0}}$	12	Chip Enable or Test 0
P1.0 to P1.6	13 to 19	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	20	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	21, 25 to 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

Table 2 SOT358-1 package (for information on parallel I/O ports, see Chapter 14)

SYMBOL	PIN	DESCRIPTION
T1	5	Test 1 or count input of 8-bit Timer/event counter 1
XTAL1	6	crystal oscillator or external clock input
XTAL2	7	crystal oscillator output
RESET	8	reset input
CE/$\overline{\text{T0}}$	9	Chip Enable or Test 0
P1.0 to P1.6	10 to 12, 14 to 16, 18	Port 1: 7 quasi-bidirectional I/O lines
P1.7/MDY	19	Port 1: quasi-bidirectional I/O line or melody output
P2.0 to P2.3	20, 24 to 26	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	21	ground
TONE	22	DTMF output
V_{DD}	23	positive supply voltage
P0.0 to P0.7	27, 29 to 32, 2 to 4	Port 0: 8 quasi-bidirectional I/O lines or wake-up interrupts
n.c.	1, 13, 17, 28	not connected

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.4). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.Their frequencies are provided in purely sinusoidal form on the TONE output or as square waves on the P1.7/MDY output.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

In case no tones are generated, or the melody function is used, the TONE output is in tri-state mode.

6.1 Frequency generator derivative registers

6.1.1 HIGH AND LOW GROUP FREQUENCY REGISTERS

Table 3 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers HGF (High Group Frequency) and LGF (Low Group Frequency); access type W.

Table 3 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
11H	HGF	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 MELODY AND PORT INTERRUPT CONTROL REGISTER (MDYCON)

The Melody and Port Interrupt Control Register has two functions: bit 0 defines the behaviour of the melody output; bits 4 to 7 individually enable/disable specific pairs of Port 0 interrupts. MDYCON is a R/W register.

Table 4 Melody and Port Interrupt Control Register (address 13H)

7	6	5	4	3	2	1	0
EPI3	EPI2	EPI1	EPI0	0	0	0	EMO

Table 5 Description of MDYCON bits

BIT	SYMBOL	DESCRIPTION
7 to 4	EPI3 to EPI0	Enable Port 0 interrupts. Bits 7 to 4 individually enable/disable specific pairs of Port 0 interrupts; see Table 6 and Section 8.2 for details.
3 to 1	–	These bits are set to a logic 0.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line and the TONE output is enabled. If bit EMO = 1, then P1.7/MDY is the melody output and the TONE output is disabled (tri-state). EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the logic HIGH state.

Table 6 Port 0 Interrupts control bits

BIT	STATE	INTERRUPTS			
		P0.0 AND P0.1	**P0.2 AND P0.3**	**P0.4 AND P0.5**	**P0.6 AND P0.7**
EPI0	1	enabled	–	–	–
	0	disabled	–	–	–
EPI1	1	–	enabled	–	–
	0	–	disabled	–	–
EPI2	1	–	–	enabled	–
	0	–	–	disabled	–
EPI3	1	–	–	–	enabled
	0	–	–	–	disabled

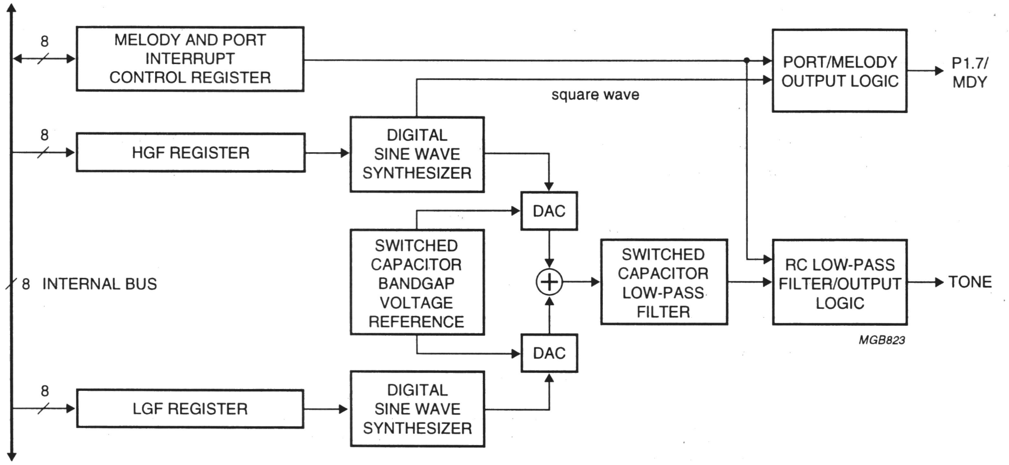

8
MELODY AND PORT INTERRUPT CONTROL REGISTER
PORT/MELODY OUTPUT LOGIC
P1.7/ MDY
square wave
8
HGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER
DAC
SWITCHED CAPACITOR BANDGAP VOLTAGE REFERENCE
8 INTERNAL BUS
SWITCHED CAPACITOR LOW-PASS FILTER
RC LOW-PASS FILTER/OUTPUT LOGIC
TONE
MGB823
DAC
8
LGF REGISTER
DIGITAL SINE WAVE SYNTHESIZER

Fig.4 Block diagram of the frequency generator and melody output (P1.7/MDY) section.

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

If bit EMO = 1 in the Melody and Port Interrupt Control Register the TONE output is disabled (tri-state) and a square wave with the frequency defined by the HGF contents is output on line P1.7/MDY. The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the limitation $60 \leq x \leq 255$ is relaxed to $2 \leq x \leq 255$ in this application; x = decimal value of the HGF register contents. Due to the low-pass filters, the simultaneous signal on the TONE output is not useful for $x < 60$.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY; see Chapter 14, Table 25.

6.3 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature.

The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave. The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value ‘x’ held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x+2)]};\ \text{where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.4 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 7.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 8.

Table 7 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 8 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.5 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 9 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low Group Frequency generation.

Table 9 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980(1)	978.82	−0.12	−1.18
82	1180(1)	1179.03	−0.08	−0.97
8F	1070(2)	1073.33	0.31	3.33
79	1270(2)	1265.30	−0.37	−4.70
80	1200(3)	1197.17	−0.24	−2.83
45	2200(3)	2192.01	−0.36	−7.99
76	1300(4)	1296.94	−0.24	−3.06
48	2100(4)	2103.14	0.15	3.14
5C	1650(1)	1655.66	0.34	5.66
52	1850(1)	1852.77	0.15	2.77
4B	2025(2)	2021.20	−0.19	−3.80
44	2225(2)	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.6 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 10). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low Group Frequency generation.

Table 10 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD(1)	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 EEPROM AND TIMER 2 ORGANIZATION

The PCD3756x types have 128 bytes of Electrically Erasable Programmable Read-Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM relies on the fact that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase access complements the read and write accesses in an EEPROM.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses take 5 ms each. To make these operations more efficient, several provisions are available in the PCD3756x.

First, the EEPROM array is structured into 32 four-byte pages (see Fig.5) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes. Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. Besides for EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.

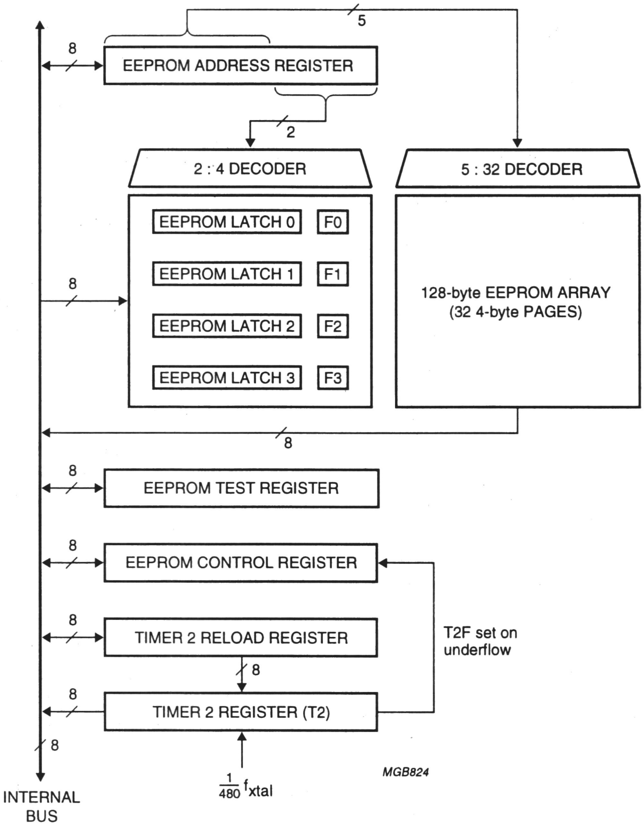

5
8
EEPROM ADDRESS REGISTER
2
2 : 4 DECODER
5 : 32 DECODER
EEPROM LATCH 0
F0
EEPROM LATCH 1
F1
8
EEPROM LATCH 2
F2
EEPROM LATCH 3
F3
128-byte EEPROM ARRAY
(32 4-byte PAGES)
8
8
EEPROM TEST REGISTER
8
EEPROM CONTROL REGISTER
8
TIMER 2 RELOAD REGISTER
T2F set on underflow
8
8
TIMER 2 REGISTER (T2)
8
MGB824
$\frac{1}{480}$ fxtal
INTERNAL BUS

Fig.5 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. The register access type is R/W.

Table 11 EEPROM Control Register (address 04H)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 12 Description of EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 13.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 13 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

7.1.2 EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed. The register access type is R/W.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 14 EEPROM Address Register (address 01H)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 15 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 13) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3 EEPROM DATA REGISTER (DATR)

Table 16 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 17 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.5) defined by bits AD0 and AD1 of ADDR.

7.1.4 EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2 EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.5) cannot be read by user software. Due to their construction, the latches can only be preset, but not cleared. Successive write operations through DATR to the EEPROM latches actually perform a logical OR with the previously stored data in EEPROM. The EEPROM latches are reset at the conclusion of any EEPROM cycle.

7.3 EEPROM flags

The four EEPROM flags (F0 to F3; Fig.5) cannot be directly accessed by user software. An EEPROM flag is set as a side-effect when the corresponding EEPROM latch is written through DATR. The EEPROM flags are reset at the conclusion of any EEPROM cycle.

7.4 EEPROM macros

The instruction sequence used in an EEPROM access should be treated as an indivisible entity. Erroneous programs result if ADDR, DATR, RELR or EPCR are inadvertently changed during an EEPROM cycle or its setup. Special care should be taken if the program may asynchronously divert due to an interrupt. Particularly, a new access to the EEPROM may only be initiated when no write, erase or erase/write cycles are in progress. This can be verified by reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that the Timer 2 Reload Register (RELR) has been loaded with the appropriate value for a 5 ms delay, which depends on f_{xtal} (see Table 24). The end of a write, erase or erase/write cycle will be signalled by a cleared EWP and by a Timer 2 interrupt provided that ET2I = 1 and that the SIO/derivative interrupt is enabled.

7.5 EEPROM access

One read, one write, one erase/write and one erase access are defined by bits EWP and MC1 to MC3 in the EPCR register; see Table 11.

Read byte retrieves the EEPROM byte addressed by ADDR when DATR is read. Read cycles are instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is a combination of an erase and a subsequent write cycle, consequently taking 10 ms.

As their names imply, **write page, erase page and erase/write page** are applied to a whole EEPROM page. Therefore, bits AD0 and AD1 of register ADDR (see Table 14), defining the byte location within an EEPROM page, are irrelevant during write and erase cycles. However, write and erase cycles need not affect all bytes of the page. The EEPROM flags F0 to F3 (see Fig.5) determine which bytes within the EEPROM page are affected by the erase and/or write cycles. A byte whose corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding EEPROM flag is set. With write page, data in EEPROM Latch 0 to 3 (Fig.5) are ORed to the individual page bytes if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes are erased and ORed with the corresponding EEPROM latches.

ORing, in this event, means that the EEPROM latches are copied to the selected page bytes.

The described page-wise organization of erase and write cycles allows up to four bytes to be individually erased or written within 5 ms. This advantage necessitates a preparation step, called **page setup**, before the actual erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1 PAGE SETUP

Page setup is a preparation step required before write page, erase page and erase/write page cycles.
As previously described, these page operations include single-byte write, erase and erase/write as a special event. EEPROM flags F0 to F3 determine which page bytes will be affected by the mentioned page operations. EEPROM Latch 0 to 3 must be preset through DATR to specify the write cycle data to EEPROM and to set the EEPROM flags as a side-effect. Obviously, the actual preset value of the EEPROM latches is irrelevant for erase page. Preset of one, two, three or all four EEPROM latches and the corresponding EEPROM flags can be performed by repeatedly defining ADDR and writing to DATR (see Table 18).

If more than one EEPROM latch must be preset, the subcounter consisting of AD0 and AD1 can be induced to auto-increment after every write to DATR, thus stepping through all EEPROM latches. For this purpose, increment mode (Table 13) must be selected. Auto-incrementing stops at EEPROM Latch 3. It is not mandatory to start at EEPROM Latch 0 as in shown in Table 19.

Note that AD2 to AD6 are irrelevant during page setup. They will usually specify the intended EEPROM page, anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will contain the intended EEPROM page address after page setup.

Table 18 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 19 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2 READ BYTE

Since ADDR auto-increments after a read cycle regardless of the page boundary, successive bytes can efficiently be read by repeating the last instruction.

Table 20 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3 WRITE PAGE

The write cycle performs a logical OR between the data in the EEPROM latches and that in the addressed EEPROM page. To actually copy the data from the EEPROM latches, the corresponding bytes in the page should previously have been erased.

The EEPROM latches are preset as described in Section 7.5.1. The actual transfer to the EEPROM is then performed as shown in Table 21.

The last instruction also starts Timer 2. The data in the EEPROM latches are ORed with that in the corresponding page bytes within 5 ms. A single-byte write is simply a special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM Latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by bits AD2 to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1). This allows efficient coding of multi-page write operations.

Table 21 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4 ERASE/WRITE PAGE

The EEPROM latches are preset as described in Section 7.5.1. The page byte corresponding to the asserted flags (among F0 to F3) are erased and re-written with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes 5 ms upon which Timer Register T2 reloads for another 5 ms cycle for writing. The top cycles together take 10 ms. A single-byte erase/write is simply a special event of 'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and AD1 addressed EEPROM latch 3 prior to the write cycle, ADDR will point to the next EEPROM page (by AD2 to AD6) and to EEPROM latch 0 (by AD0 and AD1). This allows efficient coding of multi-page erase/write operations.

Table 22 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5 ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1. The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes 5 ms. A single-byte erase is simply a special case of 'erase page'.

Note that ADDR does not auto-increment after an erase cycle.

Table 23 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6 Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of $\frac{1}{480} \times f_{xtal}$. It may be used either for EEPROM timing or as a general purpose timer. Conflicts between the two applications should be carefully avoided.

7.6.1 TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to generate the 5 ms intervals needed for erasing or writing the EEPROM. At the decrement rate of $\frac{1}{480} \times f_{xtal}$, the reload value for a 5 ms interval is a function of f_{xtal}. Table 24 summarizes the required reload values for a number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR. The Timer Register T2 is loaded with the reload value from RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end of the erase operation. Therefore, Timer Register T2 is reloaded from RELR for another 5 ms interval during which the flagged EEPROM latches are copied to the corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first underflow of write page and erase page conclude the corresponding EEPROM cycle. Timer 2 is stopped, T2F is set whereas EWP and MC1 to MC3 are cleared.

Table 24 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE(1) (HEX)
1	0A
2	14
3.58	25
6	3E
10	68
16	A6

Note

1. The reload value is $(5 \times 10^{-3} \times \frac{1}{480} \times f_{xtal}) - 1$; f_{xtal} in MHz.

7.6.2 TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing, Timer 2 is started by setting STT2. The Timer Register T2 (see Table 27) is loaded with the reload value from RELR. T2 decrements to zero. On underflow, T2 is reloaded from RELR, T2F is set and T2 continues to decrement.

Timer 2 can be stopped at any time by clearing STT2. The value of T2 is then held and can be read out. After setting STT2 again, Timer 2 decrements from the reload value. Alternatively, it is possible to read T2 'on the fly' i.e. while Timer 2 is operating.

8 INTERRUPTS

8.1 Derivative interrupt

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 11 and 12).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

8.2 Port 0 Wake-up interrupts

In addition to the external interrupt CE, the PCD3756x contains 8 level-sensitive external interrupt sources on Port 0. This function generates an interrupt request if any of the enabled lines of Port 0 (P0.0 to P0.7) is pulled LOW. Like the external interrupt (and contrary to the derivative interrupt) the Port 0 interrupt operates also in Stop mode and forces the CPU to exit the Stop mode.

The Port 0 Wake-up interrupts are controlled by the Enable Port 0 Interrupt bits EPI3 to EPI0 in the Melody and Port Interrupt Control Register MDYCON. Pairs of Port 0 interrupts are individually enabled/disabled via bits 4, 5, 6 and 7. For details see Section 6.1.2. As the Port 0 interrupt is directly linked to the external interrupt, it uses the same flag (EIF), enable instructions (EN I, DIS I) and interrupt vector.

A Port 0 Wake-up interrupt is serviced if:

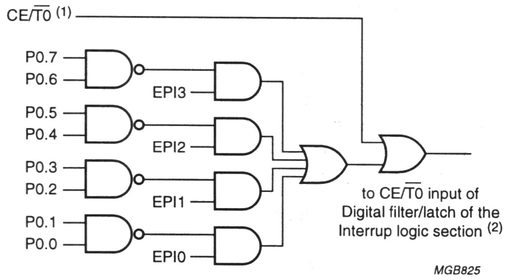
- No interrupt routine is in progress
- The external interrupt is enabled
- It's corresponding enable bit in register MDYCON is set to a logic 1.

If a Port 0 interrupt is to be used, the port flip-flop must first be set to a logic 1 (set to input mode) before it's corresponding EPIn bit is set.

If only a portion of the Port 0 interrupts are used, the remaining port lines may still be used as normal I/O.

In order to configure an I/O as an input, a logic 1 must first be written to it. If a logic 0 is written to one of these port lines (e.g. ANL P0, 00H) while it's corresponding interrupt is enabled, a Port 0 interrupt will be generated.

For more details see data sheet *"PCD33XXA Family; Section External Interrupt"*.


CE/$\overline{\text{T0}}$ (1)
P0.7
P0.6
EPI3
P0.5
P0.4
EPI2
P0.3
P0.2
EPI1
P0.1
P0.0
EPI0
to CE/$\overline{\text{T0}}$ input of
Digital filter/latch of the
Interrup logic section (2)
MGB825

(1) From pin CE/$\overline{\text{T0}}$.

(2) See the *"PCD33XXA Family"* data sheet.

Fig.6 Simplified External/Port 0 interrupt structure.

9 TIMING

Although the PCD3756x types operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33XXA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering Stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{\text{T0}}$, Timer 2 proceeds from the held state.

The Port 0 Wake-up interrupt function remains operative during Stop mode (depending only on the EPIn bits in register MDYCON). In addition to the description in the *"PCD33XXA Family"* data sheet, Stop mode may be left by a Port 0 Wake-up interrupt event (see Section 8.2).

13 INSTRUCTION SET RESTRICTIONS

RAM space is restricted to 128 bytes, care should be taken to avoid accesses to non-existing RAM locations.

14 OVERVIEW OF FAMILY MEMBERS

Table 25 Port and Power-on-reset configuration
See notes 1 and 2.

TYPE	PORT 0								PORT 1								PORT 2				V_{POR}
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
PCD3756A	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1S	1R	1R(3)	2S	2S	2S	2S	1.3 V

Notes

1. Port output drive:1 = standard I/O; 2 = open-drain I/O, see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).
3. The melody output drive type is push-pull.

15 OTP PROGRAMMING

The programming of the PCD3755x and PCD3756x OTPs is based on the OM4260 programmer (Ceibo MP-51), available from Philips. The OM4260 works in conjunction with various adapters supporting the different package types available as listed in Table 26.

The low-voltage OTP program memory used is of Anti-Fuse-PROM type and can not be erased after programming.

Thus, the complete OTP memory cannot be tested by the factory, but only partially via a special test array.
The average expected yield is 97%.

Detailed information on the OTP programming is available in the *"PCD3755x Application Note"*, being available via your Philips Sales office.

Table 26 OTP programming overview

DEVICE	PHILIPS TYPE NUMBER	CEIBO TYPE NUMBER	SUPPORTED PACKAGE
Ceibo MP-51	OM4260	MP-51 programmer base	–
PCD3755x/56x	OM5007	PCD3755A/56A adapter DIP	DIP28
PCD3755x/56x	OM5030	PCD3755A/56A adapter SO	SO28
PCD3755x/56x	OM5037(1)	PCD3755A/56A adapter QFP32	LQFP32

Note

1. As the OM5037 is only a socket converter, the OM5007 is also needed to program the PCD3755x/56x in the LQFP32 package.

16 SUMMARY OF DERIVATIVE REGISTERS

Table 27 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Melody Control Register (MDYCON)	0	0	0	0	0	0	0	EMO	R/W
14 to FF	not used									

17 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+7.0	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{SS}	ground supply current	–50	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_j	operating junction temperature	–	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

18 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

19 DC CHARACTERISTICS

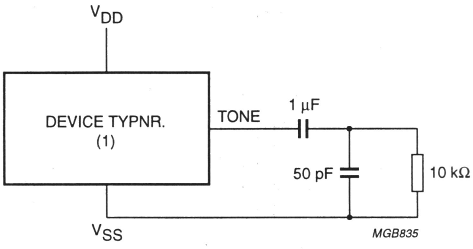
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 8 to 12)						
V_{DD}	supply voltage					
	operating; note 1		1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.8	1.6	mA
		V_{DD} = 3 V	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.5	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	2.4	6.0	mA
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	–	0.7	1.4	mA
		V_{DD} = 3 V	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz	–	1.1	3.4	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 3	–	1.0	5.5	μA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 3	–	–	10	μA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	1	μA
Port outputs (see Figs 13 to 15)						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	V_{DD} = 3 V; V_O = 2.7 V	–10	–30	–	μA
		V_{DD} = 3 V; V_O = 0 V	–	–140	–300	μA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–3.5	–	mA
TONE output (see Fig.7; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\lvert Z_O \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EEPROM (notes 1 and 6)						
$CY_{t/w}$	endurance (erase/write cycles)	note 7	10^5	–	–	
t_{ret}	data retention time		10	–	–	years
Power-on-reset						
V_{POR}	Power-on-reset level PCD3756A		0.8	1.3	1.8	V

Notes

1. TONE output, EEPROM erase and write require $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
    a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.
    b) Typical values: 25 °C; crystal connected between XTAL1 and XTAL2.
3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{T0}$ at V_{SS}.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low Group Frequency (LGF) component (CEPT).
6. After final testing the value of each EEPROM bit is a logic 1, but this cannot be guaranteed after board assembly.
7. Verified on sampling basis.



(1) Device typenr.: PCD3756x.

Fig.7 TONE output test circuit.

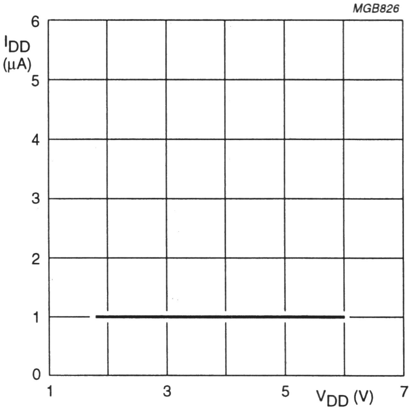
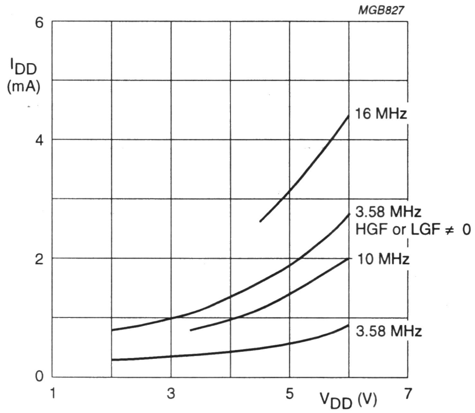
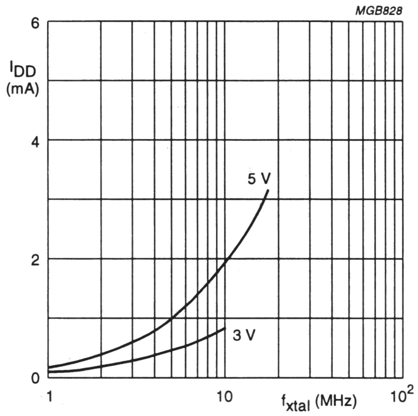


Fig.8 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



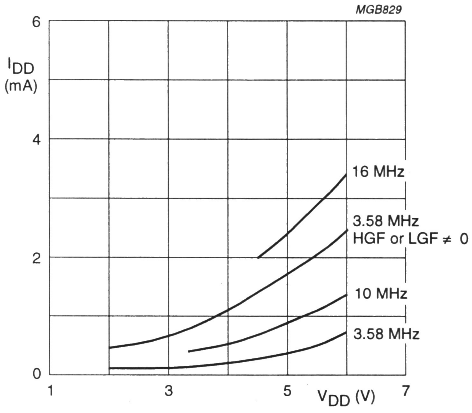
Measured with crystal between XTAL1 and XTAL2.

Fig.9 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



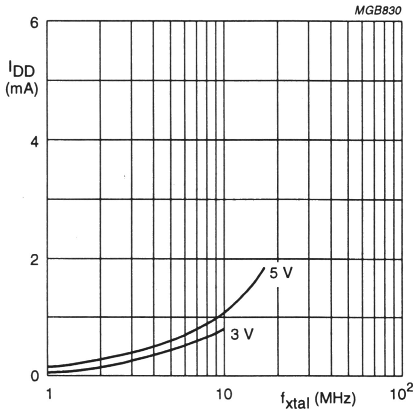
Measured with function generator on XTAL1.

Fig.10 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



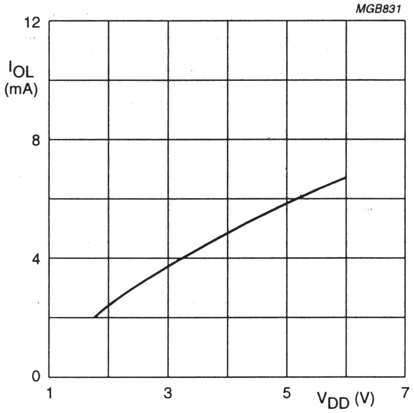
Measured with crystal between XTAL1 and XTAL2.

Fig.11 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.12 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



$V_O = 0.4$ V.

Fig.13 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

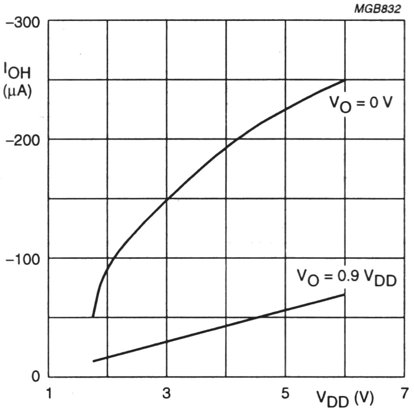
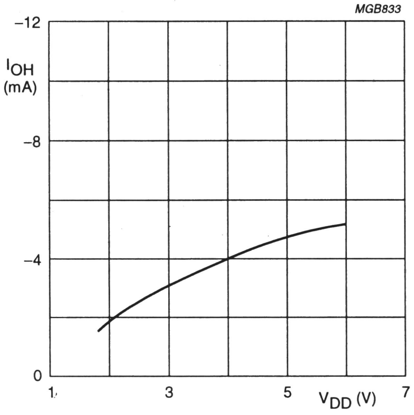


Fig.14 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.15 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

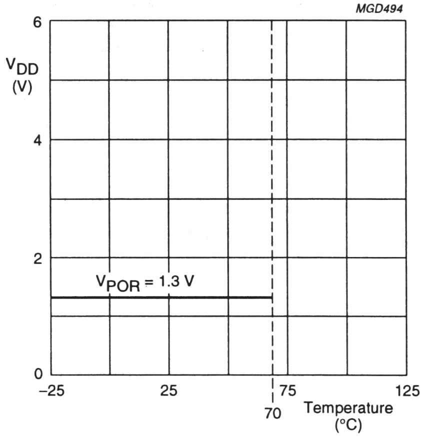


Fig.16 Typical Power-on-reset level (V_{POR}) as function of temperature.

20 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.17	1	–	16	MHz
Oscillator (see Fig.18)						
g_m	transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

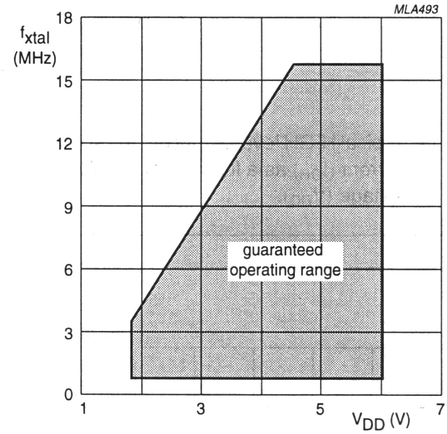


Fig.17 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

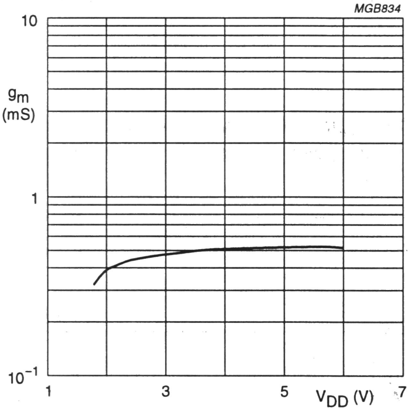


Fig.18 Typical transconductance as a function of supply voltage (V_{DD}).

Analog Voice Scrambler/Descrambler

PCD4440T

FEATURES

- Scrambler or descrambler function
- Scrambling in frequency domain
- Selectable split frequency (up to 10 selections per second)
- Telephony-band filtering included
- No increase in bandwidth
- No external components required
- Small signal delay
- Insensitive to distortion and group delay of transmission channel
- Control via serial (I²C) bus
- Low transfer loss of speech
- Mute option
- Transparent mode
- High signal input impedance
- Low signal output impedance
- Low power consumption

APPLICATIONS

- Cordless telephones
- Security telephones
- Portable phones
- PMR

GENERAL DESCRIPTION

The PCD4440 is a silicon gate CMOS integrated circuit intended to be used in radio, mobile- and line powered telecommunications products utilizing a microcontroller for the control functions. Analog scrambling/descrambling is based on the split frequency method realized in a sophisticated switched-capacitor technology. The PCD4440 is compatible with most microcontrollers and communicates via a two line bidirectional bus (I²C).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD4440T	8	mini-pack	plastic	SOT176C

BLOCK DIAGRAM

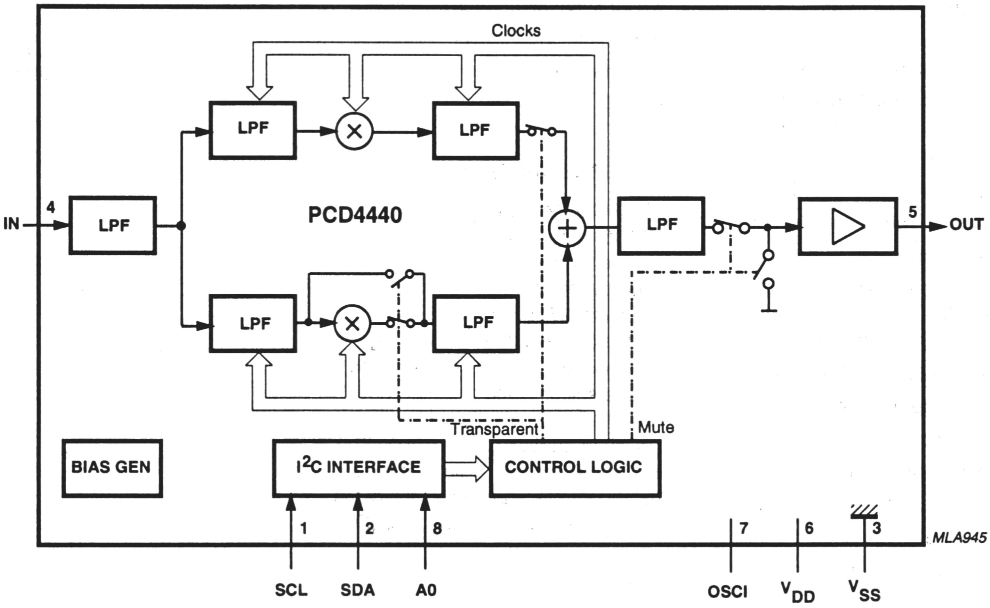

Clocks
LPF
LPF
LPF
LPF
LPF
LPF
PCD4440
IN
4
5
OUT
Transparent
Mute
BIAS GEN
I²C INTERFACE
CONTROL LOGIC
1
2
8
SCL
SDA
A0
7
6
3
OSCI
VDD
VSS
MLA945

Fig.1 Block diagram.

PINNING

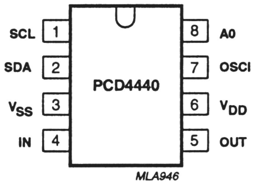


Fig.2 Pin configuration.

Pin Description

SYMBOL	PIN	FUNCTION
SCL	1	serial clock line (I^{2}C)
SDA	2	serial data line (I^{2}C)
V_{SS}	3	negative Supply
IN	4	signal input
OUT	5	signal output
V_{DD}	6	positive supply
OSCI	7	oscillator input
A0	8	slave address input (I^{2}C)

FUNCTIONAL DESCRIPTION

To provide privacy for the end user of a cordless telephone set, the radio-link audio signal must be scrambled. In the microphone and the incoming telephone line audio path a scrambler circuit has to be implemented. Consequently the audio signal to the telephone line and to the earpiece must be descrambled. Both functions can be fulfilled by the PCD4440 by simply inserting it in the audio path.

The PCD4440 accomplishes this task by first filtering the incoming signal, limiting the bandwidth to 3500 Hz. Then the signal is split into a high (> f_S) and a low (< f_S) frequency band. Both frequency bands are inverted and added again to provide a single output signal.

Values for 9 split frequencies f_S can be controlled by a scramble code table in the microcontroller. Control of these split frequencies is accomplished via the serial two wire I^{2}C-bus. In addition to the split frequencies (fs), a transparent mode and mute instruction can be selected.

In Fig.3, the signal path for both bands is drawn. The lower band path (on the left side of the diagram) operates on frequencies $f \leq f_S$ (Split Frequency), the upper band path (on the right side) on frequencies $f \geq f_S$.

The input signal contains frequencies from f_1 up to f_2. The output signal is band limited (only in scrambling mode) from f_l (300 Hz) to f_h (3500 Hz). In the left path, the input signal is first limited to f_S. The following modulator inverts the lower band. f_l is folded up to f_S, f_S down to f_l. In general, an input frequency f_{in} is folded to $f_{out} = f_S + f_l - f_{in}$. Finally the folded signal is band limited to f_S again.

In the right path, the input signal is first limited to f_h. The following modulator inverts the upper band. f_S is folded up to f_h, f_h down to f_S. In general, an input frequency f_{in} is folded to $f_{out} = f_S + f_h - f_{in}$. Finally, the folded signal is band limited to f_h again. In the last step, the bands are added and buffered.

In the transparent mode, the input signal is band limited to 3500 Hz. Frequencies form 0 - 300 Hz are not filtered out.

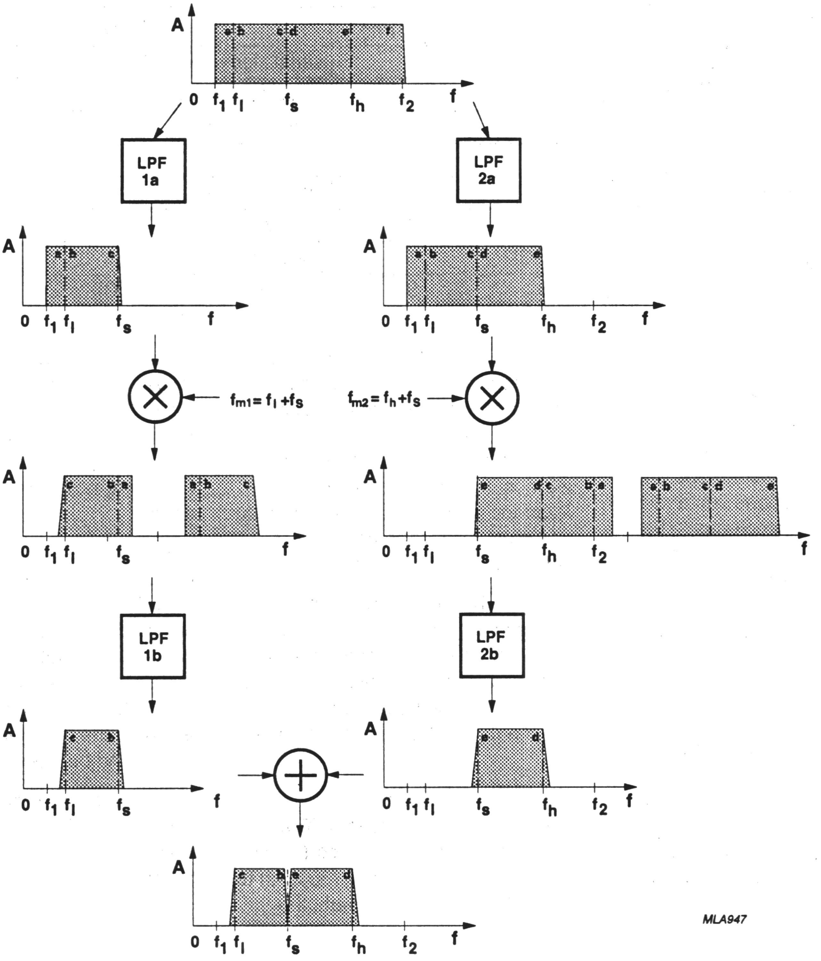

A
a b c d e f
0 f_1 f_l f_s f_h f_2 f
LPF 1a
LPF 2a
$f_{m1} = f_l + f_s$
$f_{m2} = f_h + f_s$
LPF 1b
LPF 2b
MLA947

Fig.3 Scrambler signal path.

APPLICATIONS

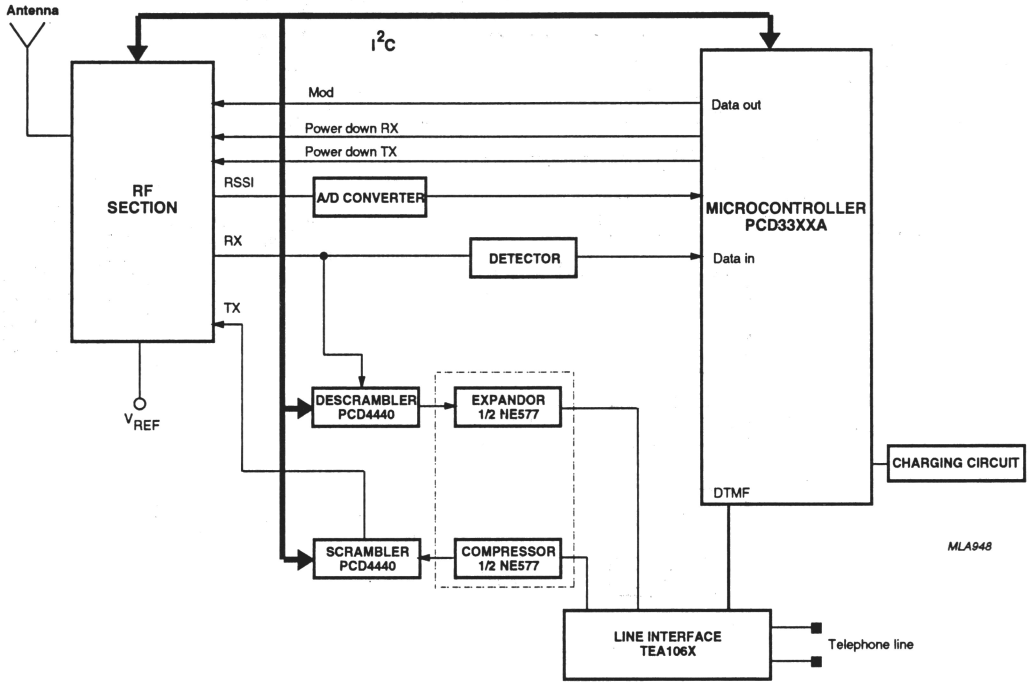

Antenna
I²C
RF SECTION
Mod
Power down RX
Power down TX
RSSI
A/D CONVERTER
RX
DETECTOR
TX
Data out
MICROCONTROLLER PCD33XXA
Data in
V_REF
DESCRAMBLER PCD4440
EXPANDOR 1/2 NE577
SCRAMBLER PCD4440
COMPRESSOR 1/2 NE577
CHARGING CIRCUIT
DTMF
MLA948
LINE INTERFACE TEA106X
Telephone line

Fig.4 CT0 handset with direct (Manchester code) data system.

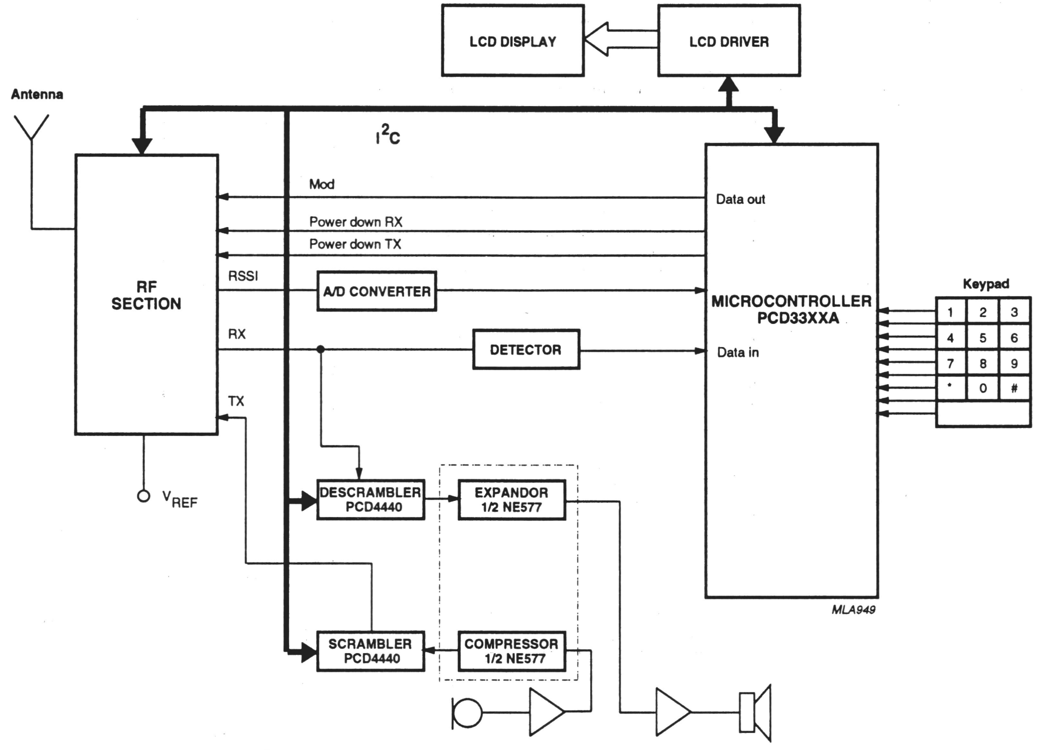

LCD DISPLAY
LCD DRIVER
Antenna
I^2C
Mod
Data out
Power down RX
Power down TX
RF SECTION
RSSI
A/D CONVERTER
MICROCONTROLLER PCD33XXA
Keypad
1
2
3
4
5
6
7
8
9
*
0
#
RX
DETECTOR
Data in
TX
V_{REF}
DESCRAMBLER PCD4440
EXPANDOR 1/2 NE577
SCRAMBLER PCD4440
COMPRESSOR 1/2 NE577
MLA949

Fig.5 CT0 Base unit with direct (Manchester code) data system.

HANDLING

Handling MOS devices

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

LCD controller/drivers PCF2104 family

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - – generation of intermediate LCD bias voltages
  - – oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I^{2}C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2104 integrated circuit is similar to the PCF2114 but does not contain the high voltage generator. It is optimized for chip-on-glass applications. The letter X in PCF2104X specifies the character set in the Character Generator ROM (CGROM). The different character sets currently available are specified by the letters C and L. Other character sets are available on request.

The PCF2104 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with a 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages which results in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2104 interfaces to most microcontrollers via a 4 or 8-bit bus or, via the 2-wire I^{2}C-bus.

Packages

- PCF2104XU/12; chip with bumps on Flexible Film Carrier (FFC)
- Pin grid array PGA144 (samples only).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

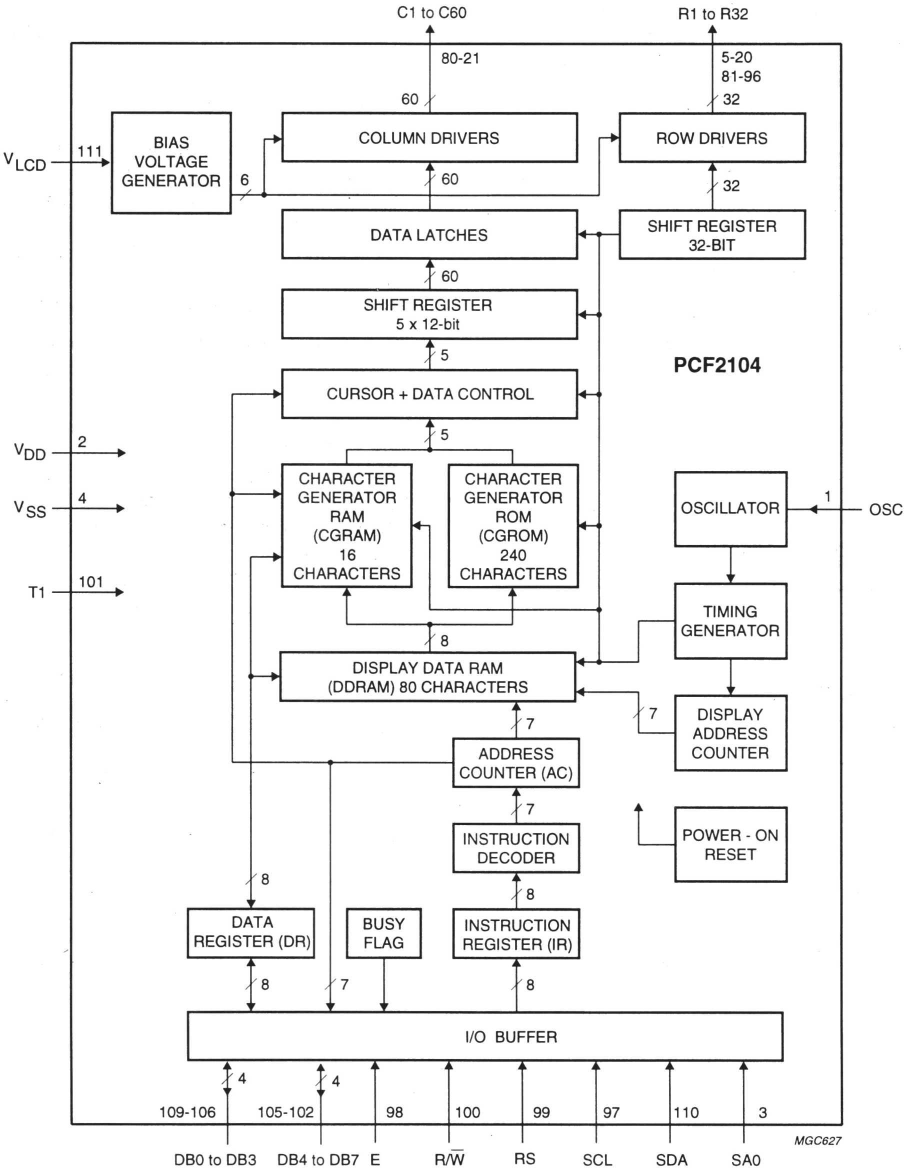

C1 to C60
80-21
60
R1 to R32
5-20
81-96
32
BIAS VOLTAGE GENERATOR
COLUMN DRIVERS
ROW DRIVERS
V_LCD
111
6
60
32
DATA LATCHES
SHIFT REGISTER 32-BIT
60
SHIFT REGISTER 5 x 12-bit
5
CURSOR + DATA CONTROL
PCF2104
5
V_DD
2
V_SS
4
T1
101
CHARACTER GENERATOR RAM (CGRAM) 16 CHARACTERS
CHARACTER GENERATOR ROM (CGROM) 240 CHARACTERS
OSCILLATOR
1
OSC
TIMING GENERATOR
8
DISPLAY DATA RAM (DDRAM) 80 CHARACTERS
7
DISPLAY ADDRESS COUNTER
7
ADDRESS COUNTER (AC)
7
INSTRUCTION DECODER
POWER - ON RESET
8
8
DATA REGISTER (DR)
BUSY FLAG
INSTRUCTION REGISTER (IR)
8
7
8
I/O BUFFER
4
4
109-106
105-102
98
100
99
97
110
3
DB0 to DB3
DB4 to DB7
E
R/W̄
RS
SCL
SDA
SA0
MGC627

Fig.1 Block diagram.

PINNING

SYMBOL	FFC PAD	DESCRIPTION
OSC	1	oscillator/external clock input
V_{DD}	2	logic supply voltage
SA0	3	I²C-bus address pin input
V_{SS}	4	ground
R8 to R5	5 to 8	LCD row driver outputs
R32 to R29	9 to12	LCD row driver outputs
R24 to R17	13 to 20	LCD row driver outputs
C60 to C1	21 to 80	LCD column driver outputs
R9 to R16	81 to 88	LCD row driver outputs
R25 to R28	89 to 92	LCD row driver outputs
R1 to R4	93 to 96	LCD row driver outputs
SCL	97	I²C-bus serial clock input
E	98	data bus clock input
RS	99	register select input
R/$\overline{W}$	100	read/write input
T1	101	test pad input
DB7 to DB0	102 to 109	bidirectional data bus input/output
SDA	110	I²C-bus serial data input/output
V_{LCD}	111	LCD supply voltage input

LCD controller/drivers

PCF2116 family (PCF2114X; PCF2116X)

FEATURES

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese syllabary) and user defined symbols
- On-chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I^{2}C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1 : 32 and 1 : 16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V
- Low power consumption.

APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

GENERAL DESCRIPTION

The PCF2116 family of LCD controller/drivers consists of 2 similar members: PCF2116X and PCF2114X, later referred to as PCF2116. The letter X in PCF2116X or PCF2114X specifies the character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, G and J. Set 'A' in PCF2116A characterises the built-in standard character set. Other character sets are available on request.

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana characters. The PCF2116 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I^{2}C-bus.

Packages

- PCF2116XU/10; chip on FFC
- PCF2114XU/10; chip on FFC
- PCF2116XU/12; chip with bumps on FFC
- PCF2114XU/12; chip with bumps on FFC
- PCF2116XH; SQFP128 (14 × 20 mm)
- Pin grid array PGA144 (samples only).

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF2114XH	128	SQFP128	plastic	SOT387-1
PCF2116XH	128	SQFP128	plastic	SOT387-1
PCF2114XU	116	FFC116	–	–
PCF2116XU	116	FFC116	–	–

BLOCK DIAGRAM

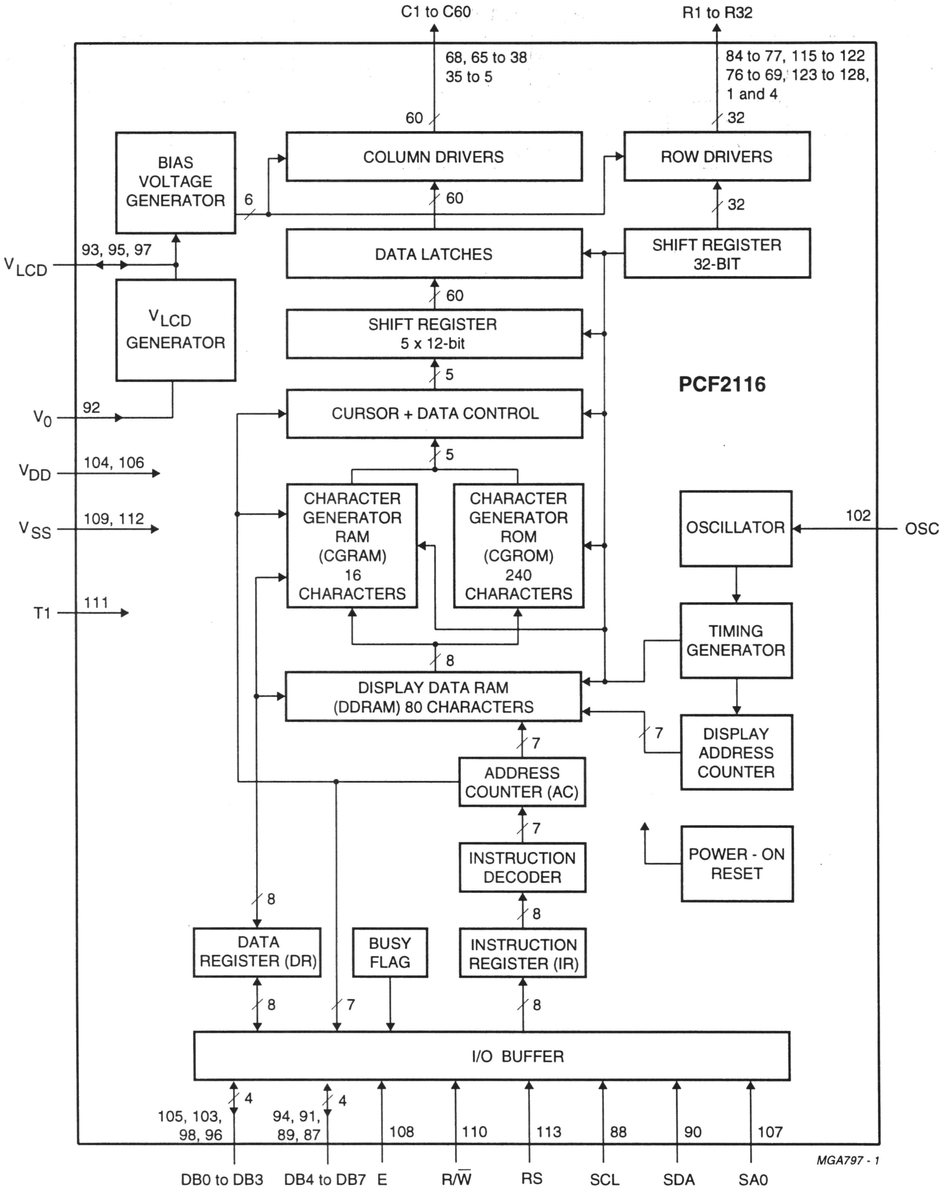

C1 to C60
R1 to R32
68, 65 to 38
35 to 5
84 to 77, 115 to 122
76 to 69, 123 to 128,
1 and 4
60
32
BIAS VOLTAGE GENERATOR
COLUMN DRIVERS
ROW DRIVERS
6
60
32
DATA LATCHES
SHIFT REGISTER 32-BIT
V_{LCD}
93, 95, 97
60
V_{LCD} GENERATOR
SHIFT REGISTER 5 x 12-bit
5
PCF2116
V_0
92
CURSOR + DATA CONTROL
5
V_{DD}
104, 106
V_{SS}
109, 112
CHARACTER GENERATOR RAM (CGRAM) 16 CHARACTERS
CHARACTER GENERATOR ROM (CGROM) 240 CHARACTERS
OSCILLATOR
102
OSC
T1
111
TIMING GENERATOR
8
DISPLAY DATA RAM (DDRAM) 80 CHARACTERS
7
7
DISPLAY ADDRESS COUNTER
ADDRESS COUNTER (AC)
7
INSTRUCTION DECODER
POWER - ON RESET
8
8
DATA REGISTER (DR)
BUSY FLAG
INSTRUCTION REGISTER (IR)
8
7
8
I/O BUFFER
4
4
105, 103, 98, 96
94, 91, 89, 87
108
110
113
88
90
107
DB0 to DB3
DB4 to DB7
E
R/$\overline{W}$
RS
SCL
SDA
SA0
MGA797 - 1

Fig.1 Block diagram (SQFP128).

PINNING

SYMBOL	SQFP128 PIN	FFC PAD	DESCRIPTION
R31	1	27	LCD row driver output
n.c.	2 and 3	–	not connected
R32	4	28	LCD row driver output
C60 to C30	5 to 35	29 to 59	LCD column driver outputs 60 to 30
n.c.	36 and 37	–	not connected
C29 to C2	38 to 65	60 to 87	LCD column driver outputs 29 to 2
n.c.	66 and 67	–	not connected
C1	68	88	LCD column driver output 1
R24 to R17	69 to 76	89 to 96	LCD row driver outputs
R8 to R1	77 to 84	97 to 104	LCD row driver outputs
n.c.	85 and 86	–	not connected
DB7	87	105	bidirectional data bus
SCL	88	106	I^{2}C serial clock input
DB6	89	107	bidirectional data bus
SDA	90	108	I^{2}C serial data input/output
DB5	91	109	bidirectional data bus
V_0	92	110	control input for V_{LCD}
V_{LCD1}	93	111	LCD supply voltage
DB4	94	112	bidirectional data bus
V_{LCD2}	95	113	LCD supply voltage
DB3	96	114	bidirectional data bus
V_{LCD3}	97	115	LCD supply voltage
DB2	98	116	bidirectional data bus
n.c.	99 to 101	–	not connected
OSC	102	1	oscillator/external clock input
DB1	103	2	bidirectional data bus
V_{DD2}	104	3	supply voltage
DB0	105	4	bidirectional data bus
V_{DD1}	106	5	supply voltage
SA0	107	6	I^{2}C address pin
E	108	7	data bus clock
V_{SS1}	109	8	ground (logic)
$R/\overline{W}$	110	9	read/write
T1	111	10	test pad (connect to V_{SS})
V_{SS2}	112	11	ground (logic)
RS	113	12	register select
n.c.	114	–	not connected
R9 to R16	115 to 122	13 to 20	LCD row driver outputs
R25 to R30	123 to 128	21 to 26	LCD row driver outputs

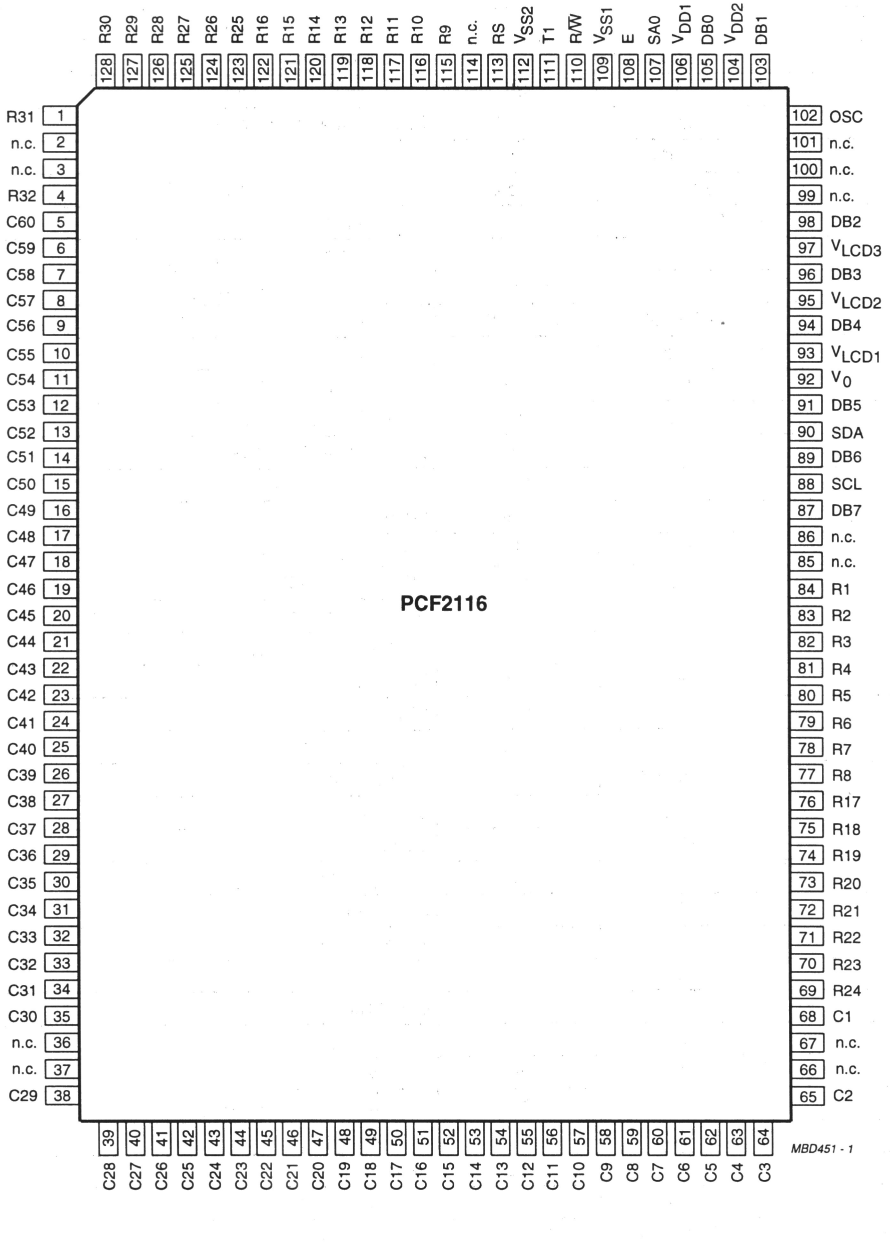

128 R30
127 R29
126 R28
125 R27
124 R26
123 R25
122 R16
121 R15
120 R14
119 R13
118 R12
117 R11
116 R10
115 R9
114 n.c.
113 RS
112 V_SS2
111 T1
110 R/W
109 V_SS1
108 E
107 SA0
106 V_DD1
105 DB0
104 V_DD2
103 DB1
R31 1
n.c. 2
n.c. 3
R32 4
C60 5
C59 6
C58 7
C57 8
C56 9
C55 10
C54 11
C53 12
C52 13
C51 14
C50 15
C49 16
C48 17
C47 18
C46 19
C45 20
C44 21
C43 22
C42 23
C41 24
C40 25
C39 26
C38 27
C37 28
C36 29
C35 30
C34 31
C33 32
C32 33
C31 34
C30 35
n.c. 36
n.c. 37
C29 38
102 OSC
101 n.c.
100 n.c.
99 n.c.
98 DB2
97 V_LCD3
96 DB3
95 V_LCD2
94 DB4
93 V_LCD1
92 V_0
91 DB5
90 SDA
89 DB6
88 SCL
87 DB7
86 n.c.
85 n.c.
84 R1
83 R2
82 R3
81 R4
80 R5
79 R6
78 R7
77 R8
76 R17
75 R18
74 R19
73 R20
72 R21
71 R22
70 R23
69 R24
68 C1
67 n.c.
66 n.c.
65 C2
PCF2116
39 C28
40 C27
41 C26
42 C25
43 C24
44 C23
45 C22
46 C21
47 C20
48 C19
49 C18
50 C17
51 C16
52 C15
53 C14
54 C13
55 C12
56 C11
57 C10
58 C9
59 C8
60 C7
61 C6
62 C5
63 C4
64 C3
MBD451 - 1

Fig.2 Pin configuration (SQFP128).

8-bit microcontrollers

PCF84C12A; PCF84C22A; PCF84C42A

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 INSTRUCTION SET
7 SUMMARY OF MASK OPTIONS
8 HANDLING MOS DEVICES
9 LIMITING VALUES
10 DC CHARACTERISTICS
11 AC CHARACTERISTICS
12 PACKAGE OUTLINES
13 SOLDERING
13.1 Introduction
13.2 DIP
13.3 SO
14 DEFINITIONS
15 LIFE SUPPORT APPLICATIONS

8-bit microcontrollers

PCF84C12A; PCF84C22A; PCF84C42A

1 FEATURES

- Manufactured in silicon gate CMOS process
- 8-bit CPU, ROM, RAM, I/O in a 20-lead package
- 1 kbyte ROM (PCF84C12A)
- 2 kbyte ROM (PCF84C22A)
- 4 kbyte ROM (PCF84C42A)
- 64 byte RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 13 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Supply voltage: 2.5 to 5.5 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C12A, PCF84C22A and PCF84C42A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the *"PCF84CXXXA family data sheet"* which should be read in conjunction with this publication.

The PCF84C12A, PCF84C22A and PCF84C42A are general purpose CMOS microcontrollers with 1 kbyte, 2 kbytes and 4 kbytes of program memory, respectively. They include 64 bytes of RAM and 13 I/O port lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF84C12AP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
PCF84C22AP			
PCF84C42AP			
PCF84C12AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCF84C22AT			
PCF84C42AT			

4 BLOCK DIAGRAM

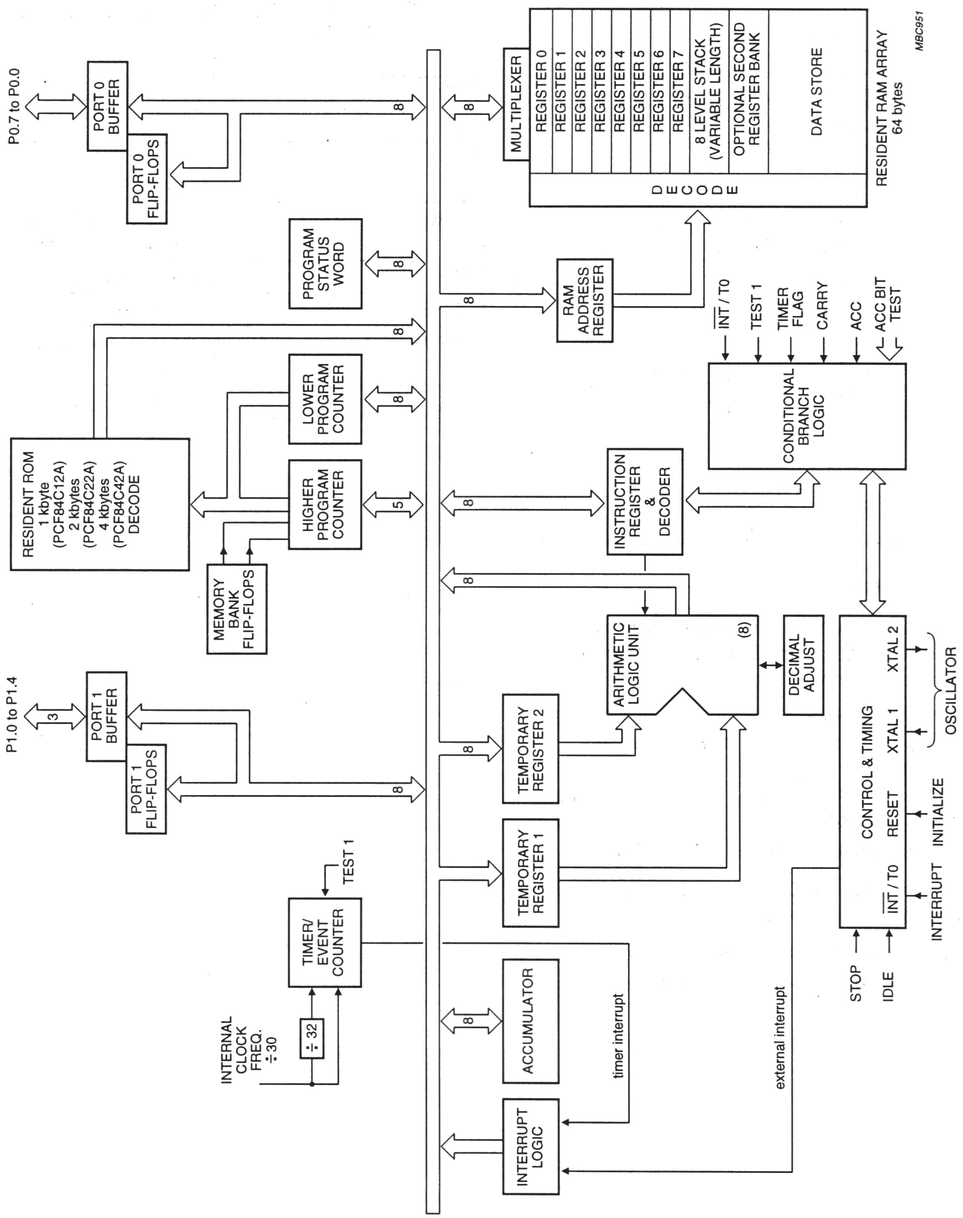

P0.7 to P0.0
PORT 0 BUFFER
PORT 0 FLIP-FLOPS
8
8
MULTIPLEXER
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
8 LEVEL STACK (VARIABLE LENGTH)
OPTIONAL SECOND REGISTER BANK
DATA STORE
DECODE
RESIDENT RAM ARRAY 64 bytes
MBC951
PROGRAM STATUS WORD
8
8
RAM ADDRESS REGISTER
INT / T0
TEST 1
TIMER FLAG
CARRY
ACC
ACC BIT TEST
8
LOWER PROGRAM COUNTER
8
CONDITIONAL BRANCH LOGIC
RESIDENT ROM 1 kbyte (PCF84C12A) 2 kbytes (PCF84C22A) 4 kbytes (PCF84C42A) DECODE
HIGHER PROGRAM COUNTER
5
8
INSTRUCTION REGISTER & DECODER
MEMORY BANK FLIP-FLOPS
8
ARITHMETIC LOGIC UNIT
(8)
DECIMAL ADJUST
CONTROL & TIMING
XTAL 2
XTAL 1
OSCILLATOR
RESET
INITIALIZE
INT / T0
INTERRUPT
STOP
IDLE
P1.0 to P1.4
3
PORT 1 BUFFER
PORT 1 FLIP-FLOPS
8
8
TEMPORARY REGISTER 2
8
TEMPORARY REGISTER 1
TEST 1
TIMER/ EVENT COUNTER
INTERNAL CLOCK FREQ. ÷ 30
÷ 32
8
ACCUMULATOR
timer interrupt
external interrupt
INTERRUPT LOGIC

Fig.1 Block diagram of PCF84C12A; PCF84C22A and PCF84C42A.

5 PINNING INFORMATION

5.1 Pinning

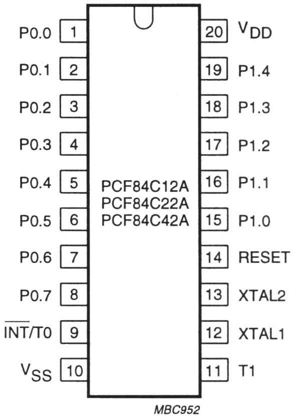

P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
INT/T0
VSS
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
VDD
P1.4
P1.3
P1.2
P1.1
P1.0
RESET
XTAL2
XTAL1
T1
PCF84C12A
PCF84C22A
PCF84C42A
MBC952

Fig.2 Pin configuration.

6 INSTRUCTION SET

Since the serial I/O interface, Port 2 and derivative logic are not provided, instructions associated with these functions are not available.

ROM space is restricted to 1 kbyte for the PCF84C12A, 2 kbytes for the PCF84C22A and 4 kbytes for the PCF84C42A. Therefore, the instructions SEL MB1/2/3 for the PCF84C12A and PCF84C22A, and the instructions SEL MB2/3 for PCF84C42A should be avoided as they would define non-existing program memory banks.

As RAM space is limited to 64 bytes, care should be taken to avoid accesses to non-existing RAM locations.

Refer to the *"PCF84CXXXA Family data sheet"* for a complete description of the instruction set.

5.2 Pin description

Table 1 DIP20 and SO20 packages

SYMBOL	PIN	FUNCTION
P0.0 to P0.7	1 to 8	Port 0: quasi-bidirectional I/O lines
$\overline{\text{INT}}$/T0	9	Interrupt/Test 0
V_{SS}	10	ground
T1	11	Test 1/count input of 8-bit timer/event counter 1
XTAL1	12	crystal oscillator input or external clock input
XTAL2	13	crystal oscillator output
RESET	14	Reset input
P1.0 to P1.4	15 to 19	Port 1: quasi-bidirectional I/O lines
V_{DD}	20	positive supply

7 SUMMARY OF MASK OPTIONS

Table 2 Mask options

ROM CODE	OPTION		
Program/data	Any mix of instructions and data up to ROM size of 1 kbyte for the PCF84C12A, 2 kbytes for the PCF84C22A and 4 kbytes for the PCF84C42A.		
Port Output Options			
P0.0 to P0.7	option 1	option 2	option 3
P1.0 to P1.4	option 1	option 2	option 3
Port State after reset			
P0.0 to P0.7	set	reset	–
P1.0 to P1.4	set	reset	–
Oscillator			
Transconductance	LOW (g_{mL})	MEDIUM (g_{mM})	HIGH (g_{mH})

8 HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

9 LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltages	–0.5	+7	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
I_{DD}	positive supply current	–50	+50	mA
I_{SS}	ground supply current	–100	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_j	operating junction temperature	–	90	°C

10 DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified. See Figs 3 to 12.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating	see Fig.3	2.5	–	5.5	V
I_{DD}	supply current operating	V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL}); see note 1	–	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); see note 1	–	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); see note 1	–	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); see note 1	–	2.5	6.0	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 3 V; f_{xtal} = 3.58 MHz (g_{mL}); see note 1	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL}); see note 1	–	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM}); see note 1	–	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); see note 1	–	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 2.5 V; T_{amb} = 25 °C; see note 2	–	1.2	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Port outputs						
I_{OL}	LOW level output current	V_{DD} = 5 V; V_O = 0.4 V; see Fig.9	–1.6	–12	–	mA
I_{OH}	HIGH level pull-up output source current HIGH	V_{DD} = 5 V; V_O = 3.5 V; see Fig.10	40	100	–	µA
		V_{DD} = 5 V; V_O = 0 V; see Fig.10	–	140	400	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 5 V; V_O = 4.6 V; see Fig.11	1.6	7	–	mA
Oscillator transconductance						
g_{mL}	option LOW	V_{DD} = 5 V	0.2	0.4	1.0	S
g_{mM}	option MEDIUM	V_{DD} = 5 V	0.9	1.6	3.2	S
g_{mH}	option HIGH	V_{DD} = 5 V	3.0	4.5	9.0	S
R_F	feedback resistor		0.3	1.0	3.0	MΩ

Notes

1. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs, including XTAL2, open (typical values at 25 °C with crystal connected between XTAL1 and XTAL2).
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET and T1 at V_{SS}; $\overline{INT}$/T0 at V_{DD}; crystal connected between XTAL1 and XTAL2; open drain outputs connected to V_{SS}; all other outputs open.

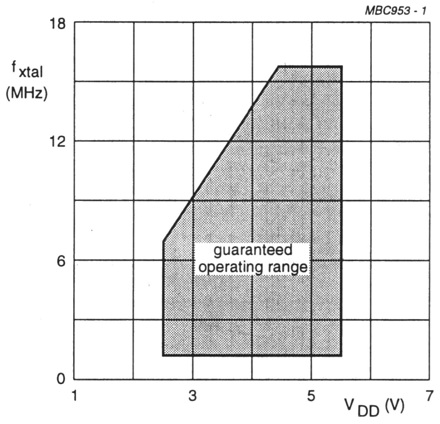


Fig.3 Maximum clock frequency as a function of supply voltage (V_{DD}).

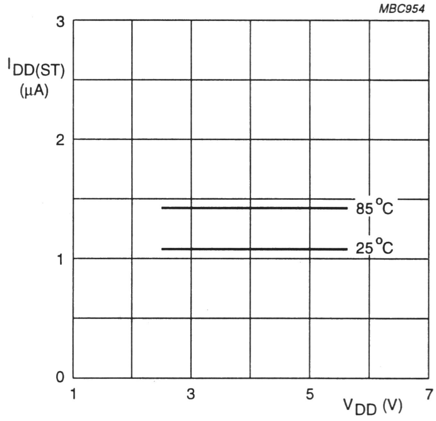


Fig.4 Typical supply current ($I_{DD(ST)}$) in Stop mode as a function of supply voltage (V_{DD}).

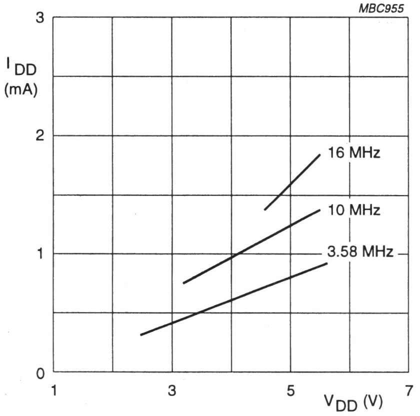


Fig.5 Typical supply current (I_{DD}) as a function of supply voltage (V_{DD}).

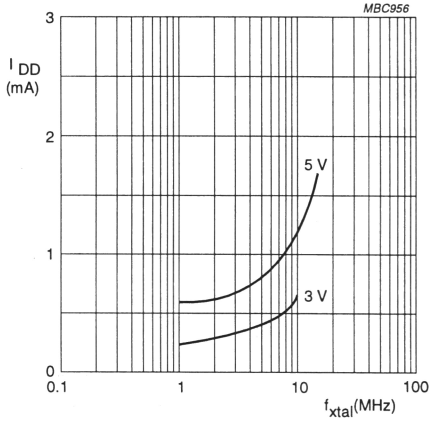


Fig.6 Typical supply current (I_{DD}) as a function of frequency (f_{xtal}).

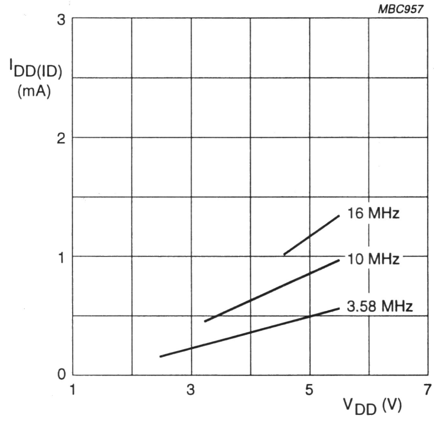


Fig.7 Typical supply current ($I_{DD(ID)}$) in Idle mode as a function of supply voltage (V_{DD}).

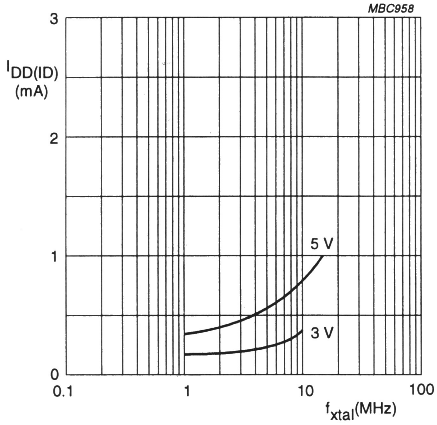
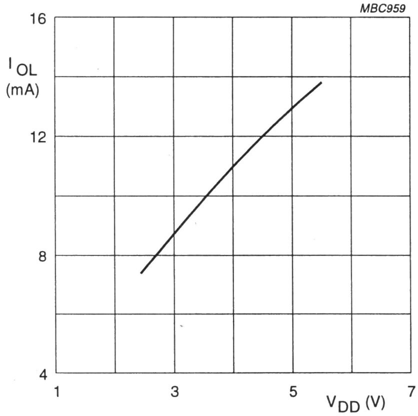


Fig.8 Typical supply current ($I_{DD(ID)}$) in Idle mode as a function of frequency (f_{xtal}).



V_O = 0.4 V.

Fig.9 Typical port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

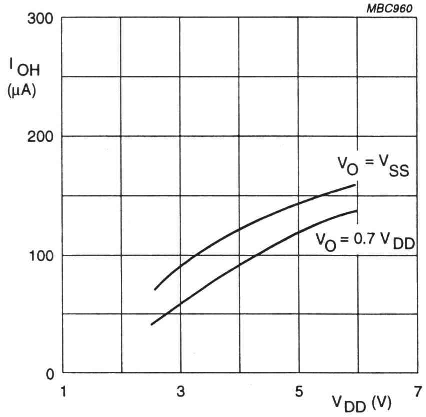
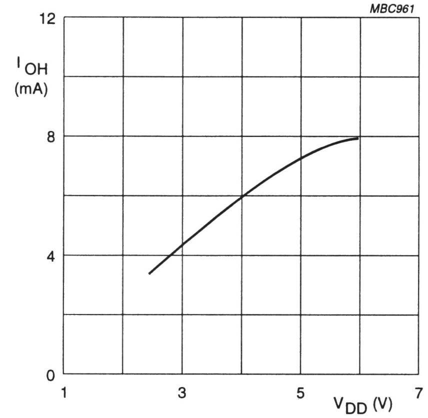


Fig.10 Typical output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.11 Typical push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

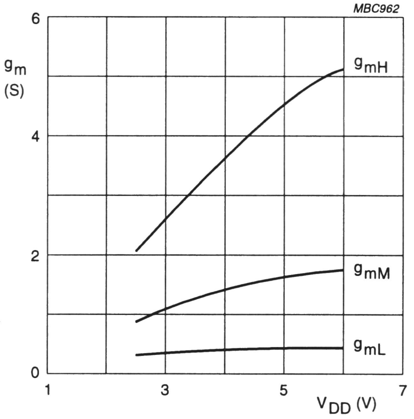


Fig.12 Typical transconductance values as a function of supply voltage (V_{DD}).

11 AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs; see note 1	–	30	–	ns
t_f	fall time all outputs; see note 1	–	30	–	ns
f_{xtal}	clock frequency; see Fig.3	1	–	16	MHz

Note

1. V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

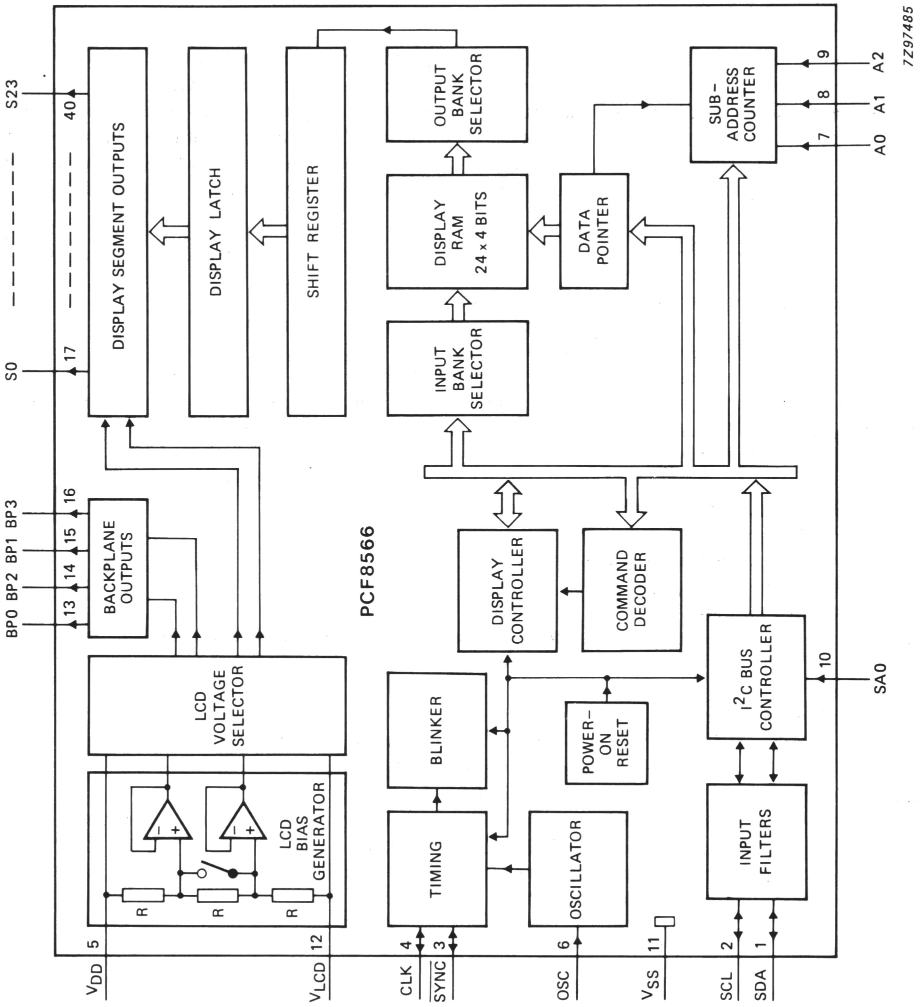

PCF8566
DISPLAY SEGMENT OUTPUTS
DISPLAY LATCH
SHIFT REGISTER
OUTPUT BANK SELECTOR
DISPLAY RAM 24 x 4 BITS
INPUT BANK SELECTOR
DATA POINTER
SUB-ADDRESS COUNTER
BACKPLANE OUTPUTS
LCD VOLTAGE SELECTOR
LCD BIAS GENERATOR
R
R
R
BLINKER
TIMING
OSCILLATOR
DISPLAY CONTROLLER
COMMAND DECODER
POWER-ON RESET
I²C BUS CONTROLLER
INPUT FILTERS
S0
17
S23
40
BP0
BP2
BP1
BP3
13
14
15
16
A0
A1
A2
7
8
9
SA0
10
V_DD
5
V_LCD
12
CLK
4
SYNC
3
OSC
6
V_SS
11
SCL
2
SDA
1
7Z97485

Fig. 1 Block diagram.

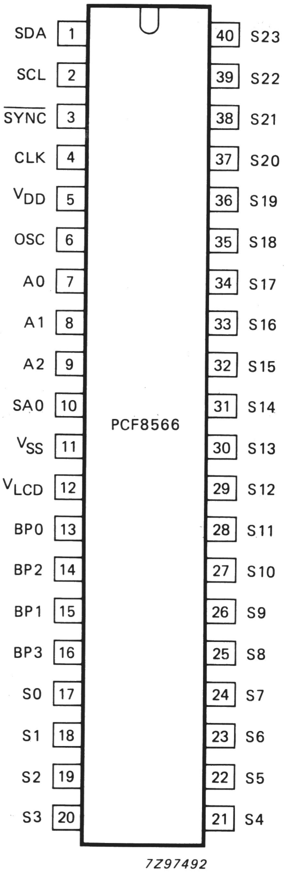

SDA 1
SCL 2
$\overline{\text{SYNC}}$ 3
CLK 4
V_{DD} 5
OSC 6
A0 7
A1 8
A2 9
SA0 10
V_{SS} 11
V_{LCD} 12
BP0 13
BP2 14
BP1 15
BP3 16
S0 17
S1 18
S2 19
S3 20
S4 21
S5 22
S6 23
S7 24
S8 25
S9 26
S10 27
S11 28
S12 29
S13 30
S14 31
S15 32
S16 33
S17 34
S18 35
S19 36
S20 37
S21 38
S22 39
S23 40
PCF8566
7Z97492

Fig. 2 Pinning diagram.

PINNING

1	SDA	I²C bus data input/output
2	SCL	I²C bus clock input/output
3	$\overline{\text{SYNC}}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7 8 9	A0 A1 A2	I²C bus subaddress inputs
10	SA0	I²C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13 14 15 16	BP0 BP2 BP1 BP3	LCD backplane outputs
17 to 40	S0 to S23	LCD segment outputs

Remote 8-bit I/O expander for I^{2}C-bus PCF8574

FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10 µA maximum
- I^{2}C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I^{2}C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, space-saving SO16 or SSOP20 package.

GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I^{2}C).

The device consists of an 8-bit quasi-bidirectional Port and an I^{2}C interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line ($\overline{\text{INT}}$) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^{2}C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and PCF8574A versions differ only in their slave address.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

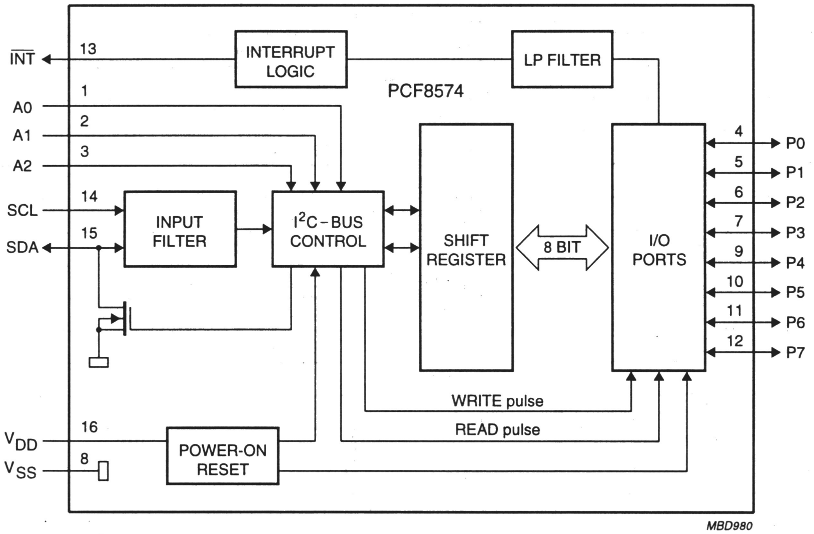

INT
13
INTERRUPT LOGIC
LP FILTER
1
A0
2
A1
3
A2
PCF8574
14
SCL
15
SDA
INPUT FILTER
I2C-BUS CONTROL
SHIFT REGISTER
8 BIT
I/O PORTS
4 P0
5 P1
6 P2
7 P3
9 P4
10 P5
11 P6
12 P7
WRITE pulse
READ pulse
16
VDD
8
VSS
POWER-ON RESET
MBD980

Fig.1 Block diagram (SOT38-1 and SOT162-1).

PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O Port 0
P1	5	11	quasi-bidirectional I/O Port 1
P2	6	12	quasi-bidirectional I/O Port 2
P3	7	14	quasi-bidirectional I/O Port 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O Port 4
P5	10	17	quasi-bidirectional I/O Port 5
P6	11	19	quasi-bidirectional I/O Port 6
P7	12	20	quasi-bidirectional I/O Port 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

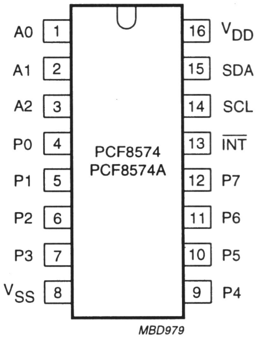

A0 1
A1 2
A2 3
P0 4
P1 5
P2 6
P3 7
VSS 8
16 VDD
15 SDA
14 SCL
13 INT
12 P7
11 P6
10 P5
9 P4
PCF8574
PCF8574A
MBD979

Fig.2 Pin configuration (DIP16; SO16).

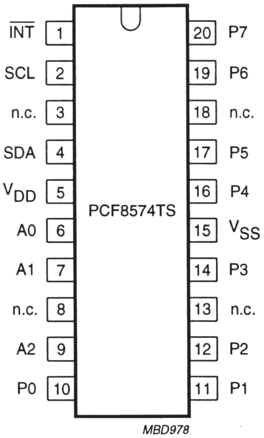

INT 1
SCL 2
n.c. 3
SDA 4
VDD 5
A0 6
A1 7
n.c. 8
A2 9
P0 10
20 P7
19 P6
18 n.c.
17 P5
16 P4
15 VSS
14 P3
13 n.c.
12 P2
11 P1
PCF8574TS
MBD978

Fig.3 Pin configuration (SSOP20).

Universal LCD driver for low multiplex rates PCF8576C

FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^{2}C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
- No external components
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I^{2}C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576CT	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576CU	–	uncased chip in tray	–
PCF8576CU/10	FFC	chip-on-film frame carrier	–
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

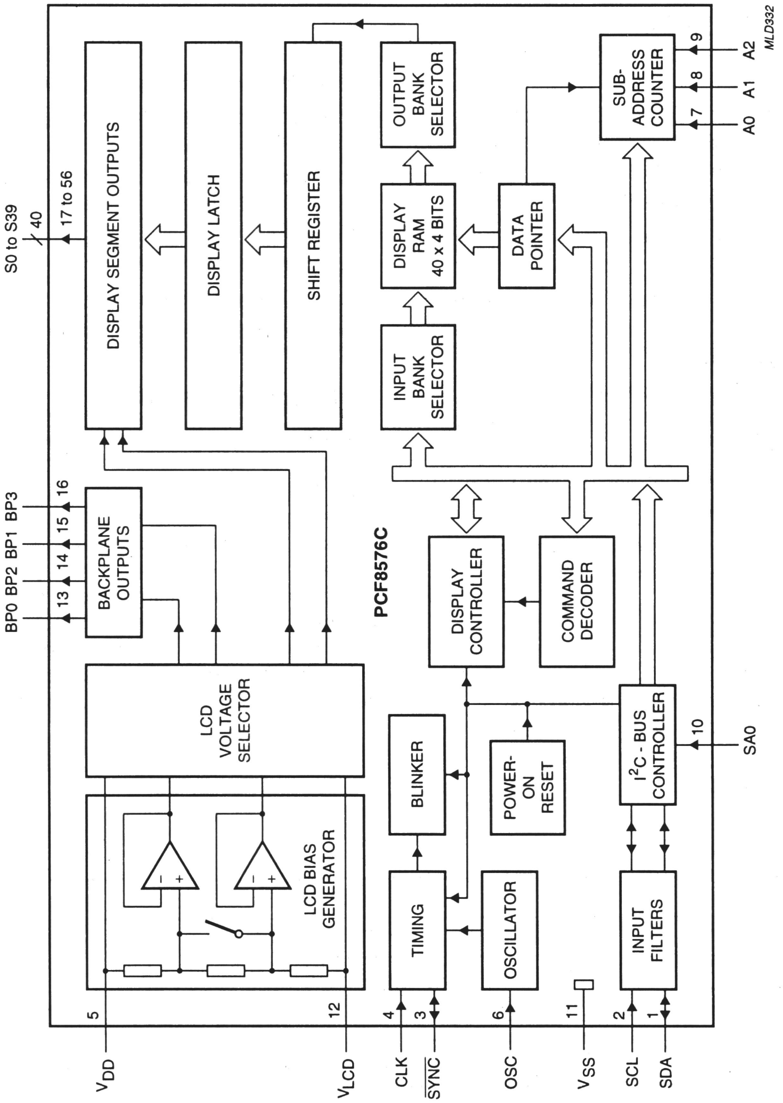

S0 to S39
40
17 to 56
DISPLAY SEGMENT OUTPUTS
DISPLAY LATCH
SHIFT REGISTER
OUTPUT BANK SELECTOR
DISPLAY RAM 40 x 4 BITS
INPUT BANK SELECTOR
DATA POINTER
SUB-ADDRESS COUNTER
MLD332
9
8
7
A2
A1
A0
BP0 BP2 BP1 BP3
13
14
15
16
BACKPLANE OUTPUTS
PCF8576C
DISPLAY CONTROLLER
COMMAND DECODER
LCD VOLTAGE SELECTOR
BLINKER
POWER-ON RESET
I^2C - BUS CONTROLLER
10
SA0
LCD BIAS GENERATOR
TIMING
OSCILLATOR
INPUT FILTERS
5
12
4
3
6
11
2
1
V_{DD}
V_{LCD}
CLK
$\overline{SYNC}$
OSC
V_{SS}
SCL
SDA

Fig.1 Block diagram; VSO56.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT190	SOT314	
SDA	1	10	I²C-bus serial data input/output
SCL	2	11	I²C-bus serial clock input
$\overline{\text{SYNC}}$	3	12	cascade synchronization input/output
CLK	4	13	external clock input
V_{DD}	5	14	supply voltage
OSC	6	15	oscillator input
A0 to A2	7 to 9	16 to 18	I²C-bus subaddress inputs
SA0	10	19	I²C-bus slave address input; bit 0
V_{SS}	11	20	logic ground
V_{LCD}	12	21	LCD supply voltage
BP0, BP2, BP1, BP3	13 to 16	25 to 28	LCD backplane outputs
S0 to S39	17 to 56	29 to 32, 34 to 47, 49 to 64, 2 to 7	LCD segment outputs
n.c.	–	1, 8, 9, 22 to 24, 33 and 48	not connected

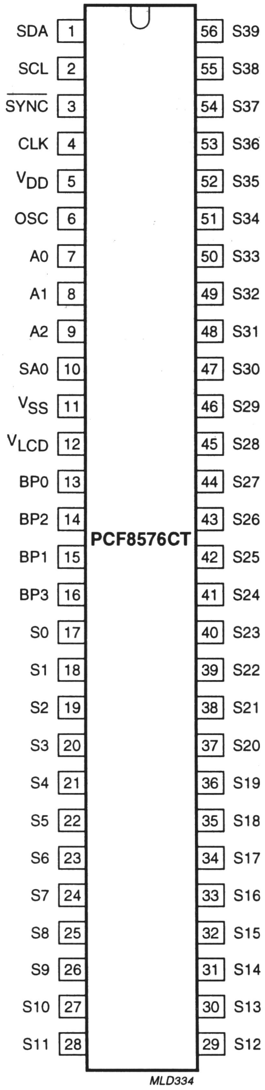

SDA 1
SCL 2
$\overline{\text{SYNC}}$ 3
CLK 4
V_{DD} 5
OSC 6
A0 7
A1 8
A2 9
SA0 10
V_{SS} 11
V_{LCD} 12
BP0 13
BP2 14
BP1 15
BP3 16
S0 17
S1 18
S2 19
S3 20
S4 21
S5 22
S6 23
S7 24
S8 25
S9 26
S10 27
S11 28
56 S39
55 S38
54 S37
53 S36
52 S35
51 S34
50 S33
49 S32
48 S31
47 S30
46 S29
45 S28
44 S27
43 S26
42 S25
41 S24
40 S23
39 S22
38 S21
37 S20
36 S19
35 S18
34 S17
33 S16
32 S15
31 S14
30 S13
29 S12
PCF8576CT
MLD334

Fig.2 Pin configuration; VSO56.

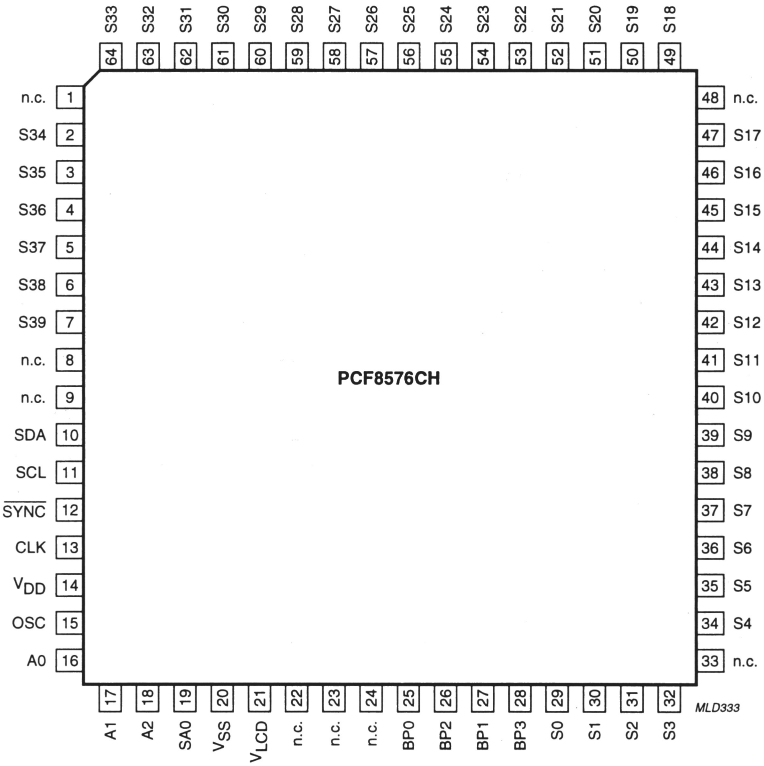

PCF8576CH
n.c. 1
S34 2
S35 3
S36 4
S37 5
S38 6
S39 7
n.c. 8
n.c. 9
SDA 10
SCL 11
$\overline{\text{SYNC}}$ 12
CLK 13
V_{DD} 14
OSC 15
A0 16
A1 17
A2 18
SA0 19
V_{SS} 20
V_{LCD} 21
n.c. 22
n.c. 23
n.c. 24
BP0 25
BP2 26
BP1 27
BP3 28
S0 29
S1 30
S2 31
S3 32
n.c. 33
S4 34
S5 35
S6 36
S7 37
S8 38
S9 39
S10 40
S11 41
S12 42
S13 43
S14 44
S15 45
S16 46
S17 47
n.c. 48
S18 49
S19 50
S20 51
S21 52
S22 53
S23 54
S24 55
S25 56
S26 57
S27 58
S28 59
S29 60
S30 61
S31 62
S32 63
S33 64
MLD333

Fig.3 Pin configuration; LQFP64.

LCD row/column driver for dot matrix graphic displays

PCF8578

FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as ${}^{32}/_{8}$, ${}^{24}/_{16}$, ${}^{16}/_{24}$ or ${}^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^{2}C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

GENERAL DESCRIPTION

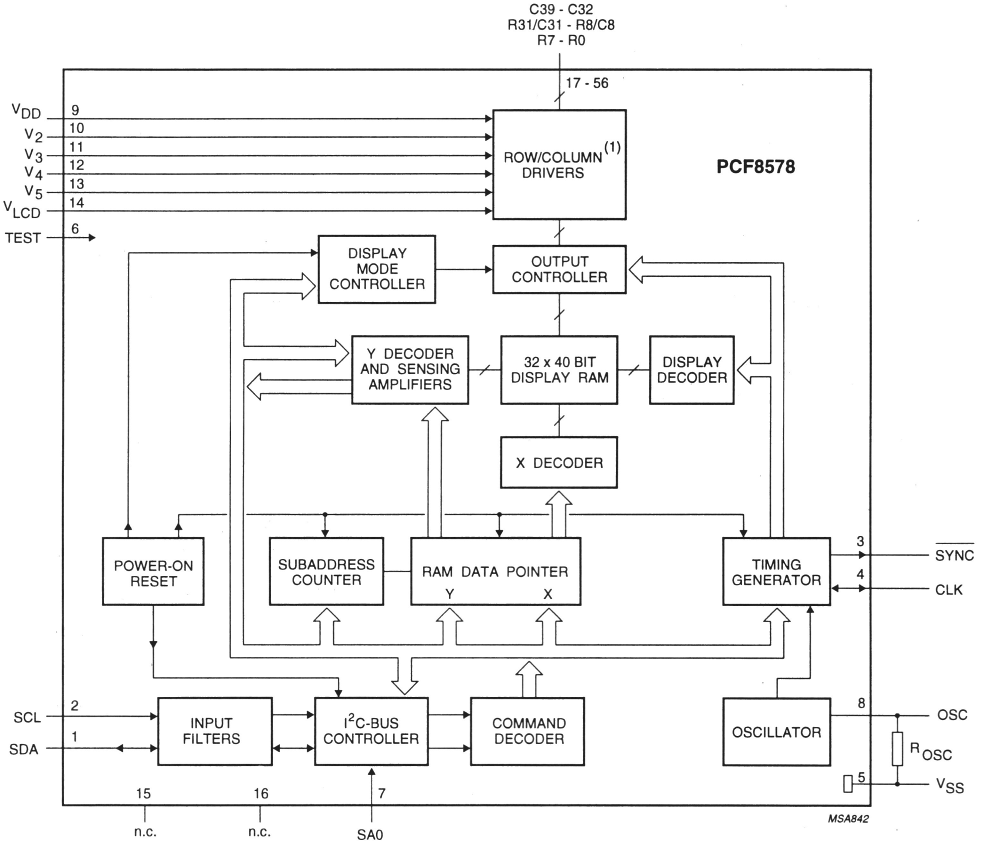
The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as ${}^{32}/_{8}$, ${}^{24}/_{16}$, ${}^{16}/_{24}$ or ${}^{8}/_{32}$ rows/columns.
The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^{2}C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8578T	56	VSO56	plastic	SOT190
PCF8578U7	–	chip with bumps on-tape	–	–

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM


C39 - C32
R31/C31 - R8/C8
R7 - R0
17 - 56
PCF8578
V_{DD} 9
V_2 10
V_3 11
V_4 12
V_5 13
V_{LCD} 14
TEST 6
ROW/COLUMN DRIVERS (1)
DISPLAY MODE CONTROLLER
OUTPUT CONTROLLER
Y DECODER AND SENSING AMPLIFIERS
32 x 40 BIT DISPLAY RAM
DISPLAY DECODER
X DECODER
POWER-ON RESET
SUBADDRESS COUNTER
RAM DATA POINTER
Y
X
TIMING GENERATOR
3 SYNC
4 CLK
SCL 2
SDA 1
INPUT FILTERS
I²C-BUS CONTROLLER
COMMAND DECODER
OSCILLATOR
8 OSC
R_{OSC}
5 V_{SS}
15 n.c.
16 n.c.
7 SA0
MSA842

(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I^{2}C-bus serial data line
SCL	2	I^{2}C-bus serial clock line
$\overline{\text{SYNC}}$	3	cascade synchronization output
CLK	4	external clock input/output
V_{SS}	5	ground (logic)
TEST	6	test pin (connect to V_{SS})
SA0	7	I^{2}C-bus slave address input (bit 0)
OSC	8	oscillator input
V_{DD}	9	positive supply voltage
V_2 to V_5	10 to 13	LCD bias voltage inputs
V_{LCD}	14	LCD supply voltage
n.c.	15, 16	not connected
C39 to C32	17 to 24	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	LCD row/column driver outputs
R7 to R0	49 to 56	LCD row driver outputs

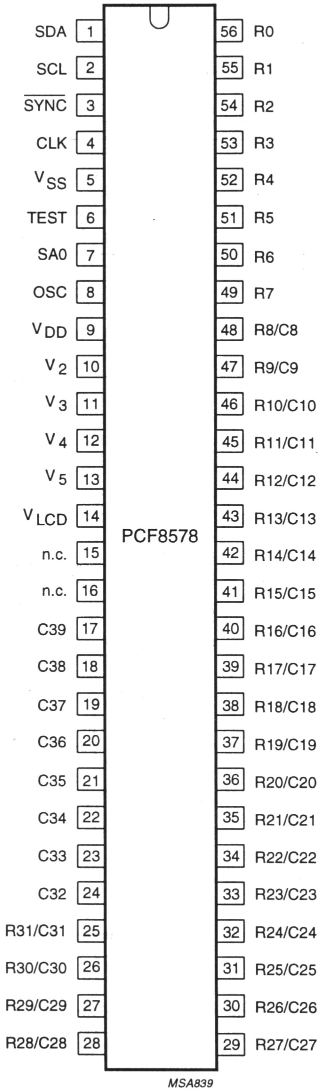

SDA 1
SCL 2
SYNC 3
CLK 4
VSS 5
TEST 6
SA0 7
OSC 8
VDD 9
V2 10
V3 11
V4 12
V5 13
VLCD 14
n.c. 15
n.c. 16
C39 17
C38 18
C37 19
C36 20
C35 21
C34 22
C33 23
C32 24
R31/C31 25
R30/C30 26
R29/C29 27
R28/C28 28
56 R0
55 R1
54 R2
53 R3
52 R4
51 R5
50 R6
49 R7
48 R8/C8
47 R9/C9
46 R10/C10
45 R11/C11
44 R12/C12
43 R13/C13
42 R14/C14
41 R15/C15
40 R16/C16
39 R17/C17
38 R18/C18
37 R19/C19
36 R20/C20
35 R21/C21
34 R22/C22
33 R23/C23
32 R24/C24
31 R25/C25
30 R26/C26
29 R27/C27
PCF8578
MSA839

Fig.2 Pin configuration.

Low power clock calendar PCF8593

FEATURES

- I^2C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{RESET}$ input pin
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 μA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I^2C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package
- Slave address:
  - READ A3H
  - WRITE A2H.

GENERAL DESCRIPTION

The PCF8593 is a CMOS Real-time clock/calendar optimized for low power consumption. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C-bus). The built-in word address register is incremented automatically after each written or read data byte. The built-in 32.768 kHz oscillator circuit and the first 8 registers are used for the clock/calendar and counter functions. The next 8 registers may be programmed as alarm registers or used as free RAM space.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I^2C-bus active	2.5	6.0	V
		I^2C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	200	μA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	4.0	15.0	μA
		f_{scl} = 0 Hz; V_{DD} = 2 V	1.0	8.0	μA
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8593P	8	DIL	plastic	SOT97-1
PCF8593T	8	SO8	plastic	SOT96-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATA SHEET

BLOCK DIAGRAM

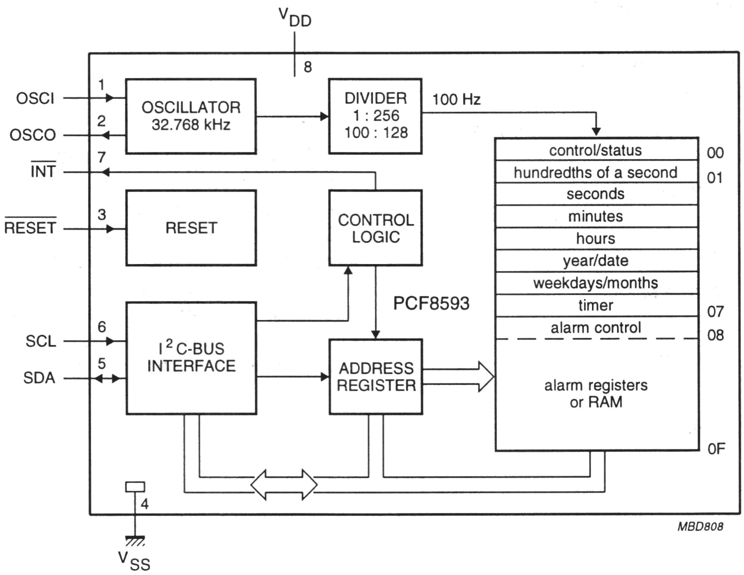

V_DD
8
OSCI
1
OSCO
2
INT
7
RESET
3
SCL
6
SDA
5
OSCILLATOR
32.768 kHz
DIVIDER
1 : 256
100 : 128
100 Hz
RESET
CONTROL
LOGIC
PCF8593
I²C-BUS
INTERFACE
ADDRESS
REGISTER
control/status
hundredths of a second
seconds
minutes
hours
year/date
weekdays/months
timer
alarm control
alarm registers
or RAM
00
01
07
08
0F
4
V_SS
MBD808

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

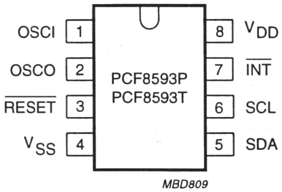

OSCI 1
OSCO 2
RESET 3
V_SS 4
8 V_DD
7 INT
6 SCL
5 SDA
PCF8593P
PCF8593T
MBD809

Fig.2 Pin configuration.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

PMBF107
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	100	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	28	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	2.4	V

PIN CONFIGURATION

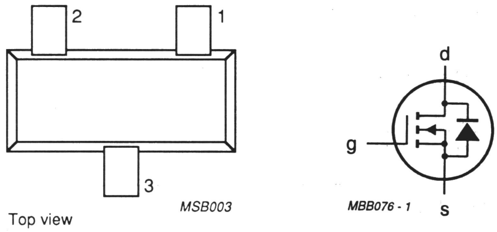


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	2.5 5.0	Ω Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs}\rvert$	min. typ.	100 200	mS mS

MECHANICAL DATA

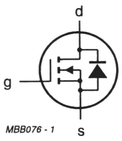
Dimensions in mm

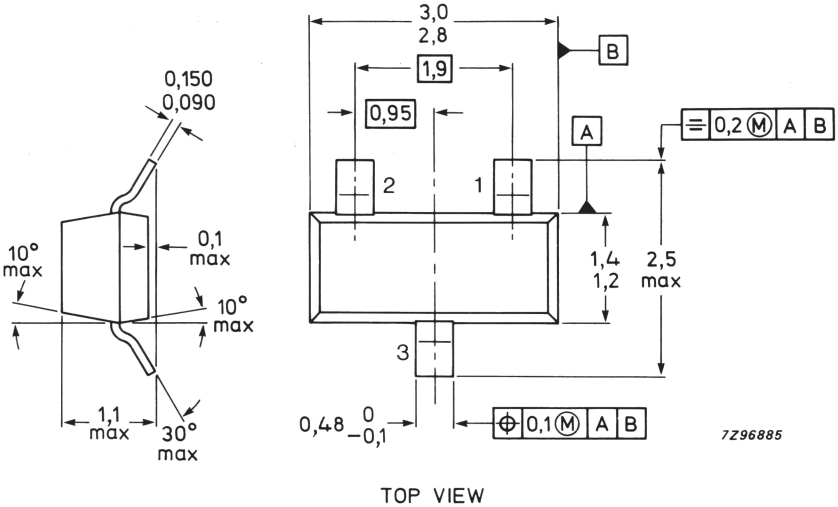
Fig.1 SOT23.

Marking code:
PMBF170 = pKX

Pinning

1 = gate
2 = source
3 = drain


d
g
s
MBB076 - 1


0,150
0,090
0,1
max
10°
max
10°
max
1,1
max
30°
max
3,0
2,8
1,9
0,95
B
A
≡ 0,2 Ⓜ A B
2
1
3
1,4
1,2
2,5
max
0,48 0 −0,1
⌖ 0,1 Ⓜ A B
7Z96885
TOP VIEW

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON EPITAXIAL TRANSISTORS

N-P-N transistors in a microminiature (SMD) plastic package intended for surface mounted applications. They are primarily intended for use in telephony and professional communication equipment.

QUICK REFERENCE DATA

			PMBTA42	PMBTA43	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	200	V
Collector-emitter voltage (open base)	V_{CEO}	max.	300	200	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6		V
Collector current (DC)	I_C	max.	500		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250		mW
Junction temperature	T_j	max.	150		°C
D.C. current gain I_C = 10 mA; V_{CE} = 10 V	h_{FE}	min.	40		
Transition frequency at f = 100 MHz I_C = 10 mA; V_{CE} = 20 V	f_T	min.	50		MHz
Feedback capacitance at f = 1 MHz I_C = 0; V_{CE} = 20 V	C_{re}	max.	3	4	pF

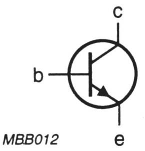
MECHANICAL DATA

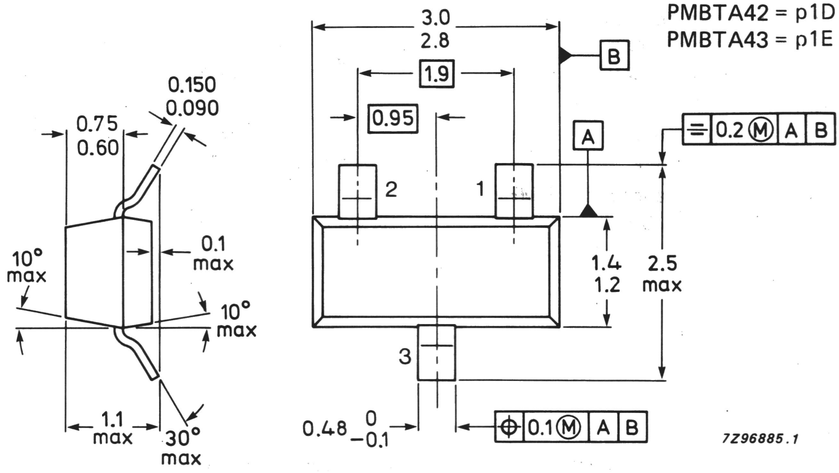
Dimensions in mm

Fig. 1 SOT-23.

Marking code
PMBTA42 = p1D
PMBTA43 = p1E

Pinning:
1 = base
2 = emitter
3 = collector




0.150
0.090
0.75
0.60
0.1
max
10°
max
10°
max
1.1
max
30°
max
3.0
2.8
B
1.9
0.95
A
≡ 0.2 Ⓜ A B
2
1
1.4
1.2
2.5
max
3
0.48 0 −0.1
⊕ 0.1 Ⓜ A B
7Z96885.1

TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PMBTA42	PMBTA43	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	200	V
Collector-emitter voltage (open base)	V_{CEO}	max.	300	200	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6	6	V
Collector current (DC)	I_C	max.	500	500	mA
Total power dissipation (note 1) up to T_{amb} = 25 ^{o}C	P_{tot}	max.	250	250	mW
Storage temperature	T_{stg}		−65 to +150	−65 to +150	^{o}C
Junction temperature	T_j	max.	150	150	^{o}C

THERMAL CHARACTERISTICS

$T_j = P\,(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

Thermal resistance from junction to ambient	$R_{th\ j\text{-}a}$	=	500	K/W

CHARACTERISTICS

T_{amb} = 25 ^{o}C unless otherwise specified

			PMBTA42	PMBTA43	
Collector-emitter breakdown voltage (note 2) I_C = 1 mA; I_B = 0	$V_{(BR)CEO}$	min.	300	200	V
Collector-base breakdown voltage I_C = 100 μA; I_E = 0	$V_{(BR)CBO}$	min.	300	200	V
Emitter-base breakdown voltage I_E = 100 μA; I_C = 0	$V_{(BR)EBO}$	min.	6	6	V
Collector cut-off current I_E = 0; V_{CB} = 200 V	I_{CBO}	max.	0,1	–	μA
I_E = 0; V_{CB} = 160 V		max.	–	0,1	μA
Emitter cut-off current I_C = 0; V_{BE} = 6 V	I_{EBO}	max.	0,1	–	μA
I_C = 0; V_{BE} = 4 V		max.	–	0,1	μA
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 20 V	C_{re}	max.	3	4	pF

Notes

1. Mounted on an FR4 printed-circuit board 8 mm x 10 mm x 0.7 mm.
2. Pulse test conditions: t_p = 300 μs; δ = 0,02.

Saturation voltages				
I_C = 20 mA; I_B = 2 mA	V_{CEsat}	max.	0,5	V
	V_{BEsat}	max.	0,9	V
D.C. current gain				
I_C = 1 mA; V_{CE} = 10 V		min.	25	
I_C = 10 mA; V_{CE} = 10 V	h_{FE}	min.	40	
I_C = 30 mA; V_{CE} = 10 V		min.	40	
Transition frequency at f = 100 MHz				
I_C = 10 mA; V_{CE} = 20 V	f_T	min.	50	MHz

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON EPITAXIAL TRANSISTORS

P-N-P transistors in a microminiature (SMD) plastic package intended for surface mounted applications. They are primarily intended for use in telephony and professional communication equipment.

QUICK REFERENCE DATA

			PMBTA92	PMBTA93	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	300	200	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	300	200	V
Emitter-base voltage (open collector)	$-V_{EBO}$	max.	5		V
Collector current (d.c.)	$-I_C$	max.	500		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250		mW
D.C. current gain $-I_C$ = 10 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	40		
Transition frequency at f = 100 MHz $-I_C$ = 10 mA; $-V_{CE}$ = 20 V	f_T	min.	50		MHz
Collector-base capacitance at f = 1 MHz I_E = 0; $-V_{CB}$ = 20 V	C_c	max.	6	8	pF

MECHANICAL DATA

Dimensions in mm

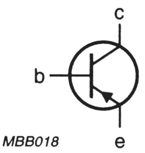
Fig. 1 SOT-23.

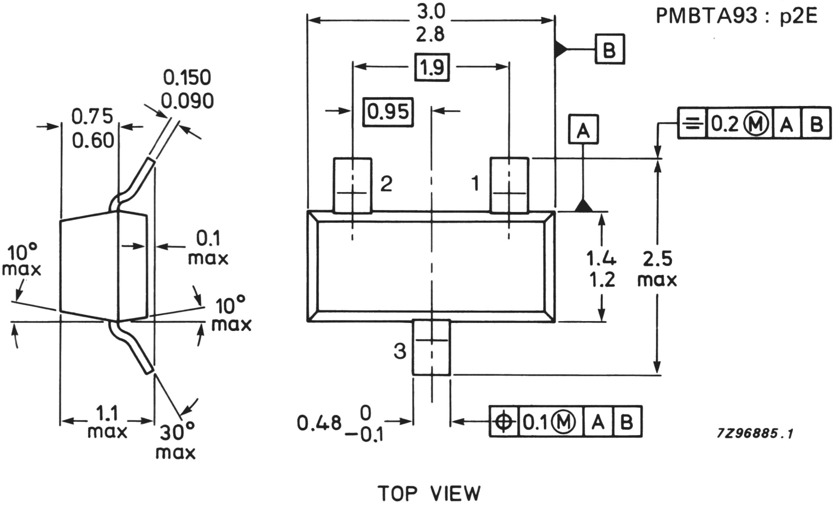
Marking code

PMBTA92 : p2D
PMBTA93 : p2E

Pinning:

1 = base
2 = emitter
3 = collector




0.150
0.090
0.75
0.60
0.1
max
10°
max
10°
max
1.1
max
30°
max
3.0
2.8
B
1.9
0.95
A
0.2 Ⓜ A B
2
1
1.4
1.2
2.5
max
3
0.48 0 −0.1
0.1 Ⓜ A B
7Z96885.1
TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PMBTA92	PMBTA93	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	300	200	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	300	200	V
Emitter-base voltage (open collector)	$-V_{EBO}$	max.	5		V
Collector current (d.c.)	$-I_C$	max.	500		mA
Total power dissipation * up to T_{amb} = 25 °C	P_{tot}	max.	250		mW
Storage temperature	T_{stg}		−65 to +150		°C
Junction temperature	T_j	max.	150		°C

THERMAL CHARACTERISTICS **

$T_j = P\,(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

Thermal resistance from junction to ambient*	$R_{th\ j\text{-}a}$	=	500	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			PMBTA92	PMBTA93	
Collector-emitter breakdown voltage $-I_C$ = 1 mA; I_B = 0	$-V_{(BR)CEO}$	min.	300	200	V
Collector-base breakdown voltage $-I_C$ = 100 μA; I_E = 0	$-V_{(BR)CBO}$	min.	300	200	V
Collector cut-off current $-V_{CB}$ = 200 V; I_E = 0	$-I_{CBO}$	max.	0,25	–	μA
$-V_{CB}$ = 160 V; I_E = 0		max.	–	0,25	μA
Emitter-base breakdown voltage $-I_E$ = 100 μA; I_C = 0	$-V_{(BR)EBO}$	min.	5		V
Emitter cut-off current I_C = 0; $-V_{BE}$ = 3 V	$-I_{EBO}$	max.	0,1		μA
Collector-base capacitance at f = 1 MHz; I_E = 0; $-V_{CB}$ = 20 V	C_c	max.	6	8	pF
Saturation voltages $-I_C$ = 20 mA; $-I_B$ = 2 mA	$-V_{CEsat}$	max.	0,5		V
$-I_C$ = 20 mA; $-I_B$ = 2 mA	$-V_{BEsat}$	max.	0,9		V
D.C. current gain ▲ $-I_C$ = 1 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	25		
$-I_C$ = 10 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	40		
$-I_C$ = 30 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	25		

---

* Mounted on an FR4 printed-circuit board 8 mm x 10 mm x 0.7 mm.

** See Thermal characteristics.

▲ Pulse test conditions: t_p = 300 μs; duty cycle ≤ 2%.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON EPITAXIAL TRANSISTORS

NPN transistors in a microminiature SMD package (SOT-223).
They are primarily intended for use in telephony and professional communication equipment.

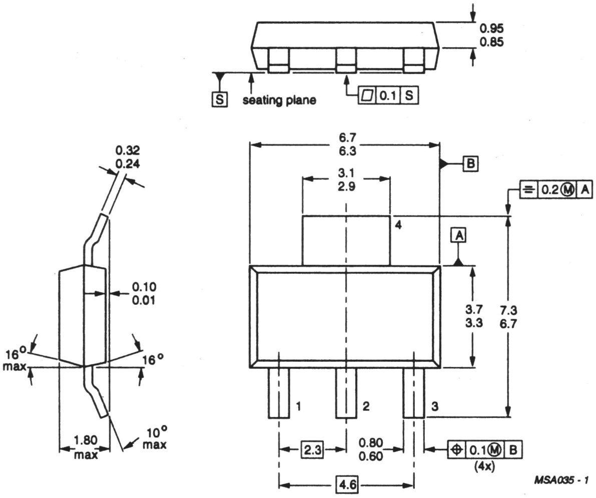
QUICK REFERENCE DATA

			PZTA42	PZTA43	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	200	V
Collector-emitter voltage (open base)	V_{CEO}	max.	300	200	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6		V
Collector current (DC)	I_C	max.	500		mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1,5		W
Junction temperature	T_j	max.	150		^oC
DC current gain $I_C = 10$ mA; $V_{CE} = 10$ V	h_{FE}	>	40		
Transition frequency at f = 100 MHz $I_C = 10$ mA; $V_{CE} = 20$ V	f_T	>	50		MHz
Feedback capacitance at f = 1 MHz $I_C = 0$; $V_{CE} = 20$ V	C_{re}	<	3	4	pF

MECHANICAL DATA

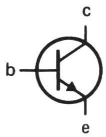
Dimensions in mm

Fig. 1 SOT-223


0.95
0.85
S
seating plane
0.1 S
0.32
0.24
6.7
6.3
B
3.1
2.9
0.2 M A
4
A
0.10
0.01
3.7
3.3
7.3
6.7
16°
max
16°
1
2
3
1.80
max
10°
max
2.3
0.80
0.60
0.1 M B
(4x)
4.6
MSA035 - 1

Pinning

1 = Base
2 = Collector
3 = Emitter
4 = Collector



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PZTA42	PZTA43	
Collector-base voltage (open emitter)	V_{CBO}	max.	300	200	V
Collector-emitter voltage (open base)	V_{CEO}	max.	300	200	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6		V
Collector current (DC)	I_C	max.	500		mA
Total power dissipation* up to T_{amb} = 25 °C	P_{tot}	max.	1,5		W
Storage temperature range	T_{stg}		−65 to +150		°C
Junction temperature	T_j	max.	150		°C

THERMAL CHARACTERISTICS

Thermal resistance from junction to ambient*	$R_{th\,j\text{-}a}$	=	83,3	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			PZTA42	PZTA43	
Collector-emitter breakdown voltage** I_C = 1 mA; I_B = 0	$V_{(BR)CEO}$	>	300	200	V
Collector-base breakdown voltage I_C = 100 μA; I_E = 0	$V_{(BR)CBO}$	>	300	200	V
Emitter-base breakdown voltage I_E = 100 μA; I_C = 0	$V_{(BR)EBO}$	>	6	6	V
Collector cut-off current I_E = 0; V_{CB} = 200 V	I_{CBO}	<	0,1	–	μA
I_E = 0; V_{CB} = 160 V		<	–	0,1	μA
Emitter cut-off current I_C = 0; V_{BE} = 6 V	I_{EBO}	<	0,1	–	μA
I_C = 0; V_{BE} = 4 V		<	–	0,1	μA
Feedback capacitance at f = 1 MHz I_E = 0; V_{CB} = 20 V	C_{re}	<	3	4	pF

---

* Device mounted on an epoxy printed circuit board 40 mm x 40 mm x 1,5 mm; mounting pad for the collector lead min. 6 cm^2.

** Pulse test conditions t_p = 300 μs; δ = 0,02.

Saturation voltages				
I_C = 20 mA; I_B = 2 mA	V_{CEsat}	<	0,5	V
	V_{BEsat}	<	0,9	V
DC current gain				
I_C = 1 mA; V_{CE} = 10 V		>	25	
I_C = 10 mA; V_{CE} = 10 V	h_{FE}	>	40	
I_C = 30 mA; V_{CE} = 10 V		>	40	
Transition frequency at f = 100 MHz				
I_C = 10 mA; V_{CE} = 20 V	f_T	>	50	MHz

NPN high voltage transistor

PZTA44; PZTA45

FEATURES

- High voltage
- High current.

DESCRIPTION

High voltage NPN transistor in a 4-lead SOT223 surface mounting package, especially suitable for use in telecommunications applications.

PINNING - SOT223

PIN	DESCRIPTION
1	base
2	collector
3	emitter
4	collector

PIN CONFIGURATION

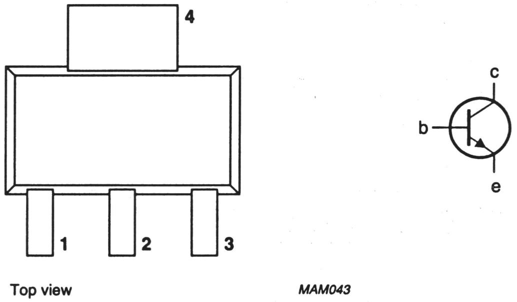


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	PZTA44		–	500	V
	PZTA45		–	400	V
V_{CEO}	collector-emitter voltage	open base			
	PZTA44		–	400	V
	PZTA45		–	350	V
$V_{CE(sat)}$	collector-emitter saturation voltage	$I_C = 50$ mA; $I_B = 5$ mA	–	750	mV
h_{FE}	DC current gain	$I_C = 100$ mA; $V_{CE} = 10$ V;	40	–	
I_C	DC collector current		–	300	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	1.5	W

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	PZTA44		–	500	V
	PZTA45		–	400	V
V_{CEO}	collector-emitter voltage	open base			
	PZTA44		–	400	V
	PZTA45		–	350	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	DC collector current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1) see Fig.2	–	1.5	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature	see Fig.2	–65	150	°C

Note

1. Refer to SOT223 standard mounting conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air (note 1)	max. 83.3 K/W

Note

1. Refer to SOT223 standard mounting conditions.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 100 μA; I_E = 0			
	PZTA44		500	–	V
	PZTA45		400	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 1 mA; I_B = 0 (note 1)			
	PZTA44		400	–	V
	PZTA45		350	–	V
$V_{(BR)CES}$	collector-emitter breakdown voltage	R_{BE} = 0; I_C = 100 μA; V_{BE} = 0			
	PZTA44		500	–	V
	PZTA45		400	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 μA; I_C = 0	6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CE(sat)}$	collector-emitter saturation voltage	I_C = 1 mA; I_B = 0.1 mA	–	0.4	V
		I_C = 10 mA; I_B = 1 mA	–	0.5	V
		I_C = 50 mA; I_B = 5 mA (note 1)	–	750	mV
$V_{BE(sat)}$	base-emitter saturation voltage	I_C = 10 mA; I_B = 1 mA	–	750	mV
I_{CBO}	collector-base cut-off current				
	PZTA44	I_E = 0; V_{CB} = 400 V	–	100	nA
		I_E = 0; V_{CB} = 400 V; T_j = 150 °C	–	10	μA
	PZTA45	I_E = 0; V_{CB} = 320 V	–	100	nA
		I_E = 0; V_{CB} = 320 V; T_j = 150 °C	–	10	μA
I_{EBO}	emitter-base cut-off current	I_C = 0; V_{EB} = 4 V	–	100	nA
I_{CES}	collector-emitter cut-off current				
	PZTA44	V_{BE} = 0; V_{CE} = 400 V	–	500	nA
	PZTA45	V_{BE} = 0; V_{CE} = 320 V	–	500	nA
h_{FE}	DC current gain	I_C = 1 mA; V_{CE} = 10 V	40	–	
		I_C = 10 mA; V_{CE} = 10 V	50	200	
		I_C = 50 mA; V_{CE} = 10 V (note 1)	45	–	
		I_C = 100 mA; V_{CE} = 10 V (note 1)	40	–	
f_T	transition frequency	I_C = 10 mA; V_{CB} = 10 V; f = 100 MHz	20	–	MHz
C_{ob}	output capacitance	I_E = 0; V_{CB} = 20 V; f = 1 MHz	–	7	pF
C_e	input capacitance	I_C = 0; V_{EB} = 0.5 V; f = 1 MHz	–	180	pF

Note

1. Pulse test : $t_p \leq 300$ μs; $\delta \leq 0.02$.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON EPITAXIAL TRANSISTORS

PNP transistors in a microminiature SMD package (SOT-223).
They are primarily intended for use in telephony and professional communication equipment.

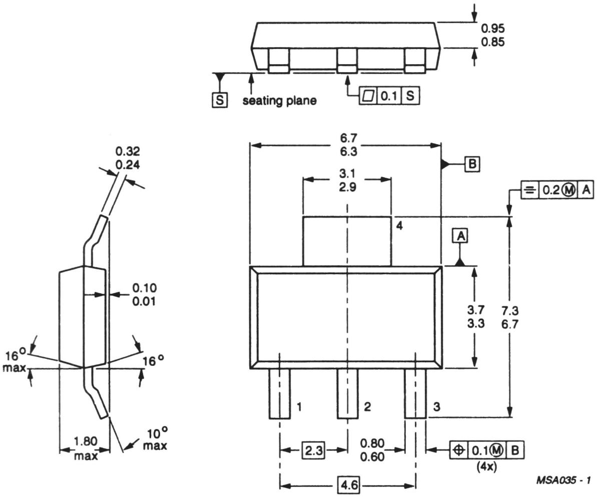
QUICK REFERENCE DATA

			PZTA92	PZTA93	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	300	200	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	300	200	V
Emitter-base voltage (open collector)	$-V_{EBO}$	max.	5		V
Collector current (DC)	$-I_C$	max.	500		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1,5		W
DC current gain $-I_C$ = 10 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	40		
Transition frequency at f = 100 MHz $-I_C$ = 10 mA; $-V_{CE}$ = 20 V	f_T	min.	50		MHz
Collector-base capacitance at f = 1 MHz I_E = 0; $-V_{CB}$ = 20 V	C_c	max.	6	8	pF

MECHANICAL DATA

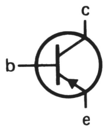
Dimensions in mm

Fig. 1 SOT-223


0.95
0.85
S
seating plane
0.1 S
6.7
6.3
B
3.1
2.9
0.2 M A
4
A
3.7
3.3
7.3
6.7
1
2
3
0.32
0.24
0.10
0.01
16°
max
16°
1.80
max
10°
max
2.3
0.80
0.60
0.1 M B
(4x)
4.6
MSA035 - 1

Pinning

1 = Base
2 = Collector
3 = Emitter
4 = Collector



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PZTA92	PZTA93	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	300	200	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	300	200	V
Emitter-base voltage (open collector)	$-V_{EBO}$	max.	5		V
Collector current (DC)	$-I_C$	max.	500		mA
Total power dissipation * up to T_{amb} = 25 °C	P_{tot}	max.	1,5		W
Storage temperature range	T_{stg}		−65 to +150		°C
Junction temperature	T_j	max.	150		°C

THERMAL CHARACTERISTICS

Thermal resistance from junction to ambient*	$R_{th\ j\text{-}a}$	= 83,3	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			PZTA92	PZTA93	
Collector-emitter breakdown voltage $-I_C$ = 1 mA; I_B = 0	$-V_{(BR)CEO}$	min.	300	200	V
Collector-base breakdown voltage $-I_C$ = 100 μA; I_E = 0	$-V_{(BR)CBO}$	min.	300	200	V
Collector cut-off current $-V_{CB}$ = 200 V; I_E = 0	$-I_{CBO}$	max.	0,25	–	μA
$-V_{CB}$ = 160 V; I_E = 0	$-I_{CBO}$	max.	–	0,25	μA
Emitter-base breakdown voltage $-I_E$ = 100 μA; I_C = 0	$-V_{(BR)EBO}$	min.	5		V
Emitter cut-off current I_C = 0; $-V_{BE}$ = 3 V	$-I_{EBO}$	max.	0,1		μA
Collector-base capacitance at f = 1 MHz; I_E = 0; $-V_{CB}$ = 20 V	C_c	max.	6	8	pF
Saturation voltages $-I_C$ = 20 mA; $-I_B$ = 2 mA	$-V_{CEsat}$	max.	0,5		V
$-I_C$ = 20 mA; $-I_B$ = 2 mA	$-V_{BEsat}$	max.	0,9		V
DC current gain** $-I_C$ = 1 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	25		
$-I_C$ = 10 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	40		
$-I_C$ = 30 mA; $-V_{CE}$ = 10 V	h_{FE}	min.	25		

---

* Device mounted on an epoxy printed circuit board 40 mm x 40 mm x 1,5 mm; mounting pad for the collector lead min. 6 mm².

** Pulse test conditions: t_p = 300 μs; duty cycle ⩽2%.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P		1,6 to 6,0	V
Total quiescent current (at $V_P = 3$ V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at $R_L = 32\ \Omega$ $V_P = 3$ V; $d_{tot} = 10\%$	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max.	70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; $R_S = 5$ kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at $R_L = 32\ \Omega$ $d_{tot} = 10\%$; $V_P = 3$ V	P_o	typ.	35	mW
$d_{tot} = 10\%$; $V_P = 4,5$ V	P_o	typ.	75	mW
Channel separation at $R_S = 0\ \Omega$; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; $R_S = 5$ kΩ	$V_{no(rms)}$	typ.	100	μV

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at $R_S = \infty$)	$\lvert Z_i \rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at $R_S = \infty$)	$\lvert Z_i \rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

---

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6	V
Peak output current	I_{OM}	max.	150	mA
Total power dissipation	see derating curve Fig. 1			
Storage temperature range	T_{stg}	−55 to + 150		°C
Crystal temperature	T_c	max.	100	°C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5	s

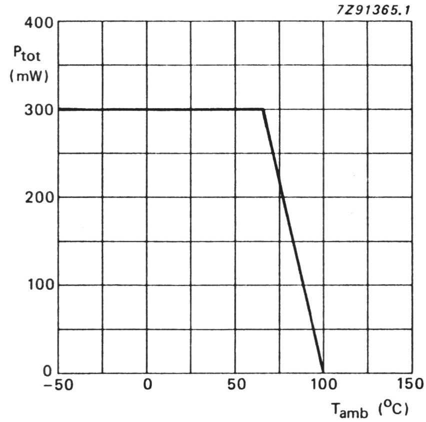


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient $R_{thj\text{-}a}$ = 110 K/W

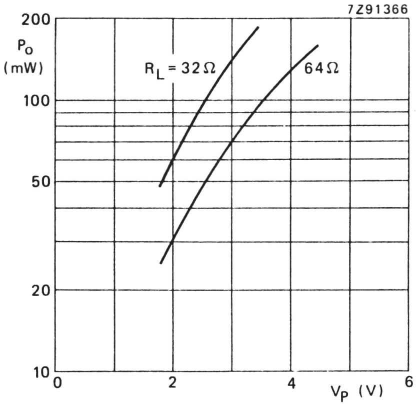


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

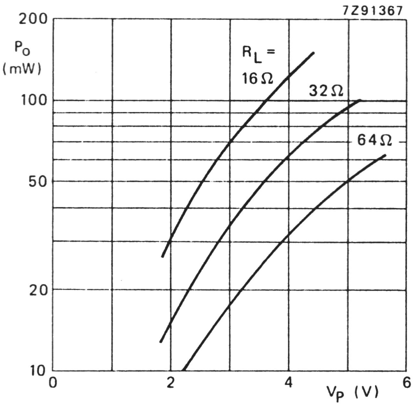


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

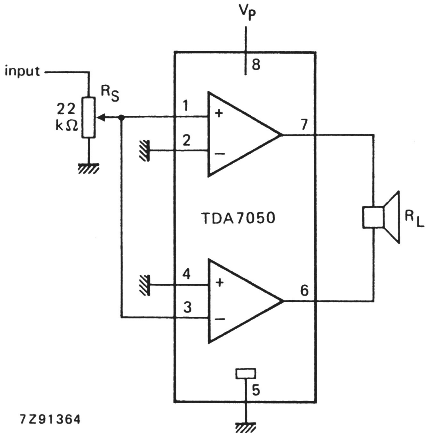

V_P
8
input
R_S
22 kΩ
1
+
2
−
7
TDA7050
R_L
4
+
3
−
6
5
7Z91364

Fig. 4 Application diagram (BTL); also used as test circuit.

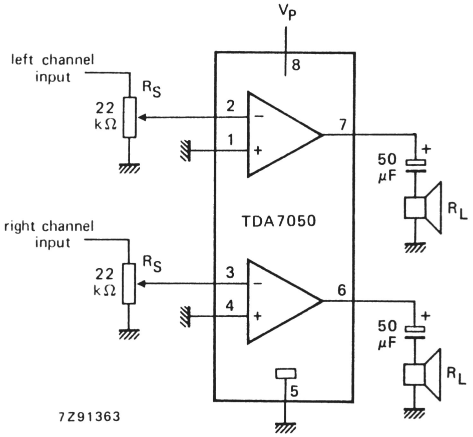

V_P
8
left channel input
R_S
22 kΩ
2
−
1
+
7
50 µF
+
R_L
TDA7050
right channel input
R_S
22 kΩ
3
−
4
+
6
50 µF
+
R_L
5
7Z91363

Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P		1,6 to 6,0 V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2 mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ.	140 mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max.	70 mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140 μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ.	35 mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75 mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100 μV

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6	V
Peak output current	I_{OM}	max.	150	mA
Total power dissipation	see derating curve Fig. 1			
Storage temperature range	T_{stg}	−55 to + 150		°C
Crystal temperature	T_c	max.	100	°C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5	s

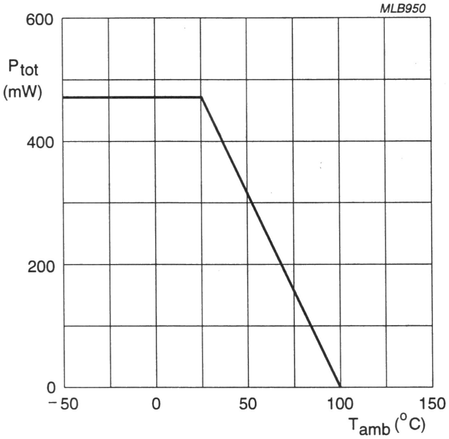


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}} = \frac{100-60}{160} = 0.25\ \text{W}$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at $R_S = \infty$)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at $R_S = \infty$)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

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* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

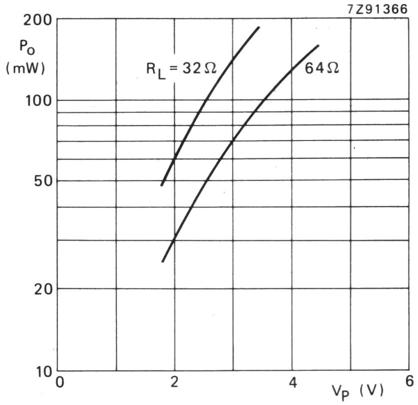


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

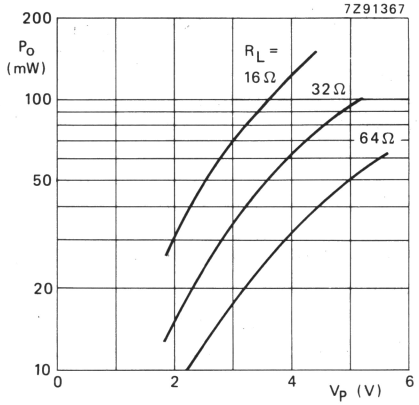


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

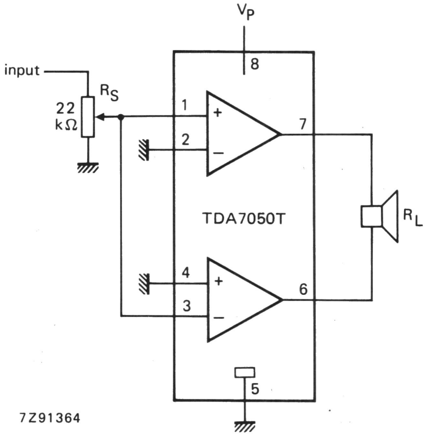

Vp
8
input
Rs
22 kΩ
1
2
7
+
−
TDA7050T
RL
4
3
6
5
7Z91364

Fig. 4 Application diagram (BTL); also used as test circuit.

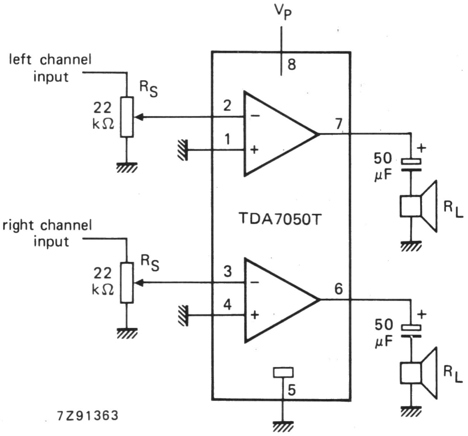

Vp
8
left channel input
Rs
22 kΩ
2
1
7
50 μF
RL
TDA7050T
right channel input
Rs
22 kΩ
3
4
6
50 μF
RL
5
7Z91363

Fig. 5 Application diagram (stereo); also used as test circuit.

1 Watt BTL mono audio amplifier with DC volume control

TDA7052A/AT

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins

GENERAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control. They are designed for use in TV and monitors, but also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
P_O	output power					
	TDA7052A	$R_L = 8\ \Omega$; $V_P = 6$ V	1.0	1.1	–	W
	TDA7052AT	$R_L = 16\ \Omega$; $V_P = 6$ V	0.5	0.55	–	W
G_v	maximum total voltage gain		34.5	35.5	36.5	dB
ϕ	gain control range		75	80	–	dB
I_P	total quiescent current	$V_P = 6$ V; $R_L = \infty$	–	7	12	mA
THD	total harmonic distortion					
	TDA7052A	$P_O = 0.5$ W	–	0.3	1	%
	TDA7052AT	$P_O = 0.25$ W	–	0.3	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7052A	8	DIL	plastic	SOT97
TDA7052AT	8	mini-pack	plastic	SOT96A

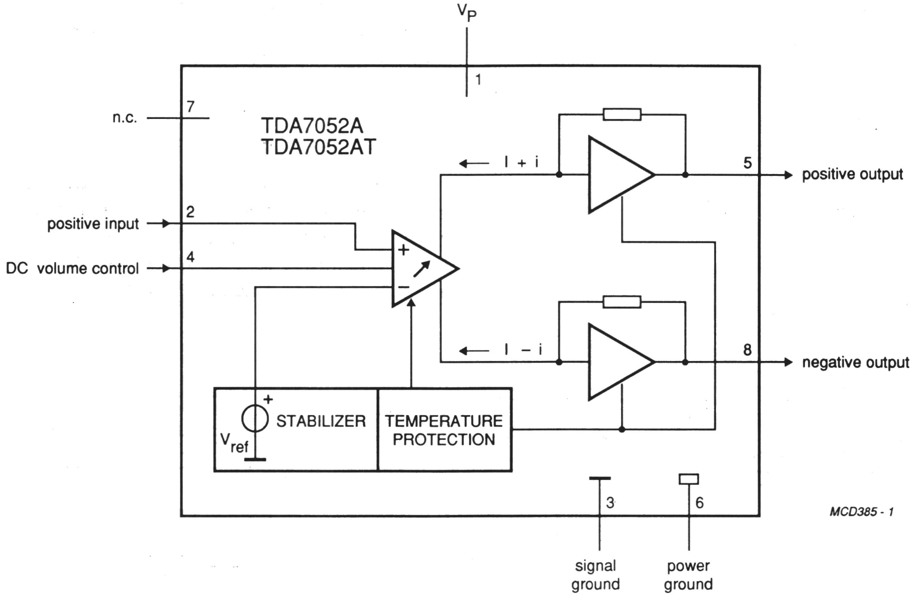

V$_P$
1
n.c.
7
TDA7052A
TDA7052AT
I + i
5
positive output
positive input
2
DC volume control
4
+
−
I − i
8
negative output
+
V$_{ref}$
STABILIZER
TEMPERATURE PROTECTION
3
6
MCD385 - 1
signal ground
power ground

Fig.1 Block diagram.

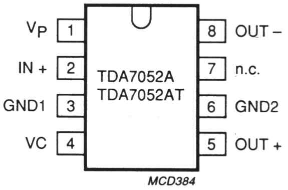

V$_P$
1
IN +
2
GND1
3
VC
4
TDA7052A
TDA7052AT
8
OUT −
7
n.c.
6
GND2
5
OUT +
MCD384

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V$_P$	1	positive supply voltage
IN+	2	positive input
GND1	3	signal ground
VC	4	DC volume control
OUT+	5	positive output
GND2	6	power ground
n.c	7	not connected
OUT−	8	negative output

FUNCTIONAL DESCRIPTION

The TDA7052A/AT are mono BTL output amplifiers with DC volume control, designed for use in TV and monitors but also suitable for battery fed portable recorders and radios.
In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.
In the TDA7052A/AT the DC volume control stage is integrated into the input stage so that no coupling capacitors are required and yet a low offset voltage is maintained. At the same time the minimum supply remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Thus a reduced power supply with smaller capacitors can be used which results in cost savings.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 35.5 dB. The DC volume control stage has a logarithmic control characteristic.

The total gain can be controlled from 35.5 dB to –44 dB. If the DC volume control voltage is below 0.3 V, the device switches to the mute mode.
The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, so the output power is reduced.
Special attention is given to switch on and off clicks, low HF radiation and a good overall stability.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	TDA7052A		–	1.25	W
	TDA7052AT		–	0.8	W
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	hr
V_2	input voltage pin 2		–	8	V
V_4	input voltage pin 4		–	8	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TDA7052A	100 K/W
	TDA7052AT	155 K/W

Note to the thermal resistance

TDA7052A: $V_P = 6$ V; $R_L = 8\ \Omega$. The maximum sine-wave dissipation is 0.9 W. Therefore $T_{amb(max)} = 150 - 100 \times 0.9 = 60$ °C.
TDA7052AT: $V_P = 6$ V; $R_L = 16\ \Omega$. The maximum sine-wave dissipation is 0.46 W. Therefore $T_{amb(max)} = 150 - 155 \times 0.46 = 78$ °C.

CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; f = 1 kHz; TDA7052A: R_L = 8 Ω; TDA7052AT: R_L = 16 Ω; unless otherwise specified (see Fig.6).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		4.5	–	18	V
I_P	total quiescent current	V_P = 6 V; R_L = ∞ note 1	–	7	12	mA
Maximum gain; V_4 = 1.4 V						
P_O	output power	THD = 10%				
	TDA7052A		1.0	1.1	–	W
	TDA7052AT		0.5	0.55	–	W
THD	total harmonic distortion					
	TDA7052A	P_O = 0.5 W	–	0.3	1	%
	TDA7052AT	P_O = 0.25 W	–	0.3	1	%
G_v	voltage gain		34.5	35.5	36.5	dB
V_I	input signal handling	V_4 = 0.8 V; THD < 1%	0.5	0.65	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	f = 500 kHz; note 2	–	210	–	μV
B	bandwidth	–1 dB	–	20 Hz to 300 kHz	–	
SVRR	supply voltage ripple rejection	note 3	38	46	–	dB
$\lvert V_{off}\rvert$	DC output offset voltage		–	0	150	mV
Z_I	input impedance (pin 2)		15	20	25	kΩ
Minimum gain; V_4 = 0.5 V						
G_v	voltage gain		–	–44	–	dB
$V_{no(rms)}$	noise output voltage (RMS value)	note 4	–	20	30	μV
Mute position						
V_O	output voltage in mute position	V_4 ≤ 0.3 V; V_I = 600 mV	–	–	30	μV
DC volume control						
ϕ	gain control range		75	80	–	dB
I_4	control current	V_4 = 0.4 V	60	70	80	μA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage dividend by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and bandwidth = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage of 200 mV, (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.

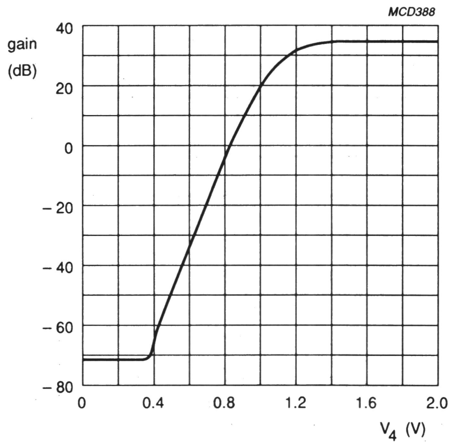


Fig.3 Gain control as a function of DC volume control.

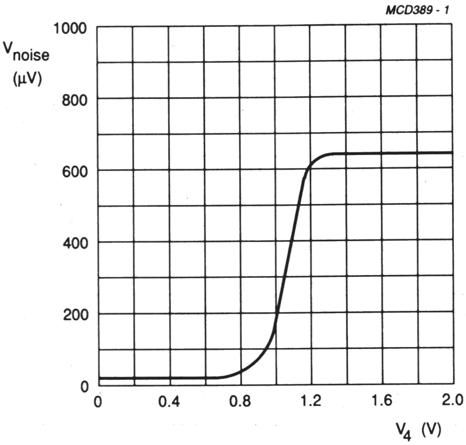


Fig.4 Noise output voltage as a function of DC volume control.

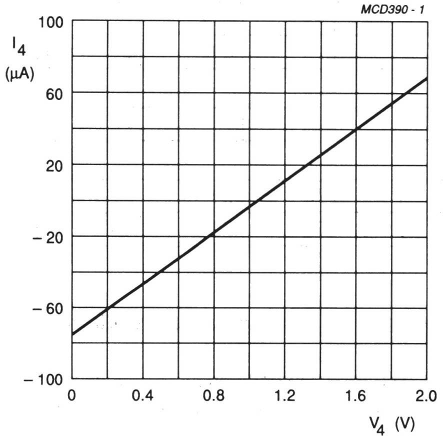
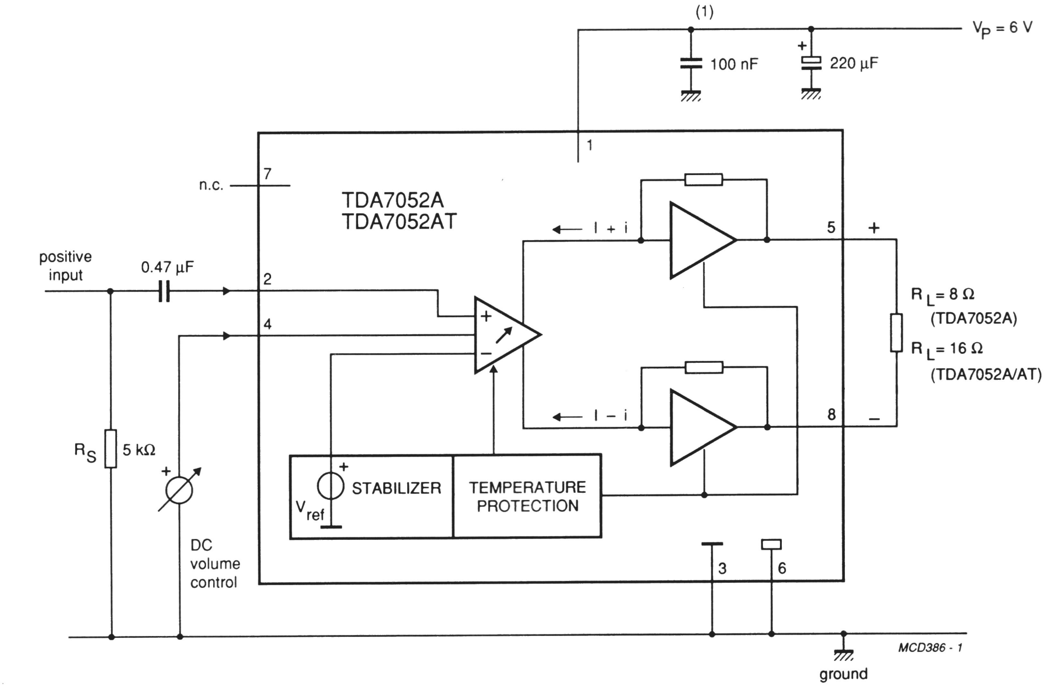


Fig.5 Control current as a function of DC volume control.

APPLICATION INFORMATION


(1)
V_P = 6 V
100 nF
220 µF
+
1
n.c.
7
TDA7052A
TDA7052AT
I + i
5
+
positive input
0.47 µF
2
4
R_L = 8 Ω (TDA7052A)
R_L = 16 Ω (TDA7052A/AT)
I − i
8
−
R_S
5 kΩ
+
STABILIZER
V_{ref}
TEMPERATURE PROTECTION
DC volume control
3
6
MCD386 - 1
ground

(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 1.

Fig.6 Test and application diagram.

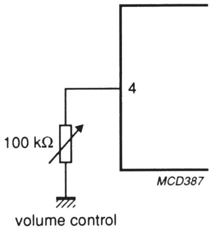

4
100 kΩ
MCD387
volume control

Fig.7 Application with potentiometer as volume control; maximum gain = 30 dB.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech, and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
Line current operating range (pin 1)		I_{line}	10	—	140	mA
Internal supply current						
power down input LOW		I_{CC}	—	0.96	1.3	mA
power down input HIGH		I_{CC}	82	55	—	μA
Supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH					
	I_P = 1.2 mA	V_{CC}	2.8	3.05	—	V
	I_P = 1.7 mA	V_{CC}	2.5	—	—	V
Voltage gain range						
microphone amplifier						
TEA1060		G_v	44	—	60	dB
TEA1061		G_v	30	—	46	dB
receiving amplifier		G_v	17	—	39	dB
Line loss compensation						
gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	—	60	V
Exchange feeding bridge resistance range		R_{exch}	400	—	1000	Ω
Operating ambient temperature range		T_{amb}	−25	—	+75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

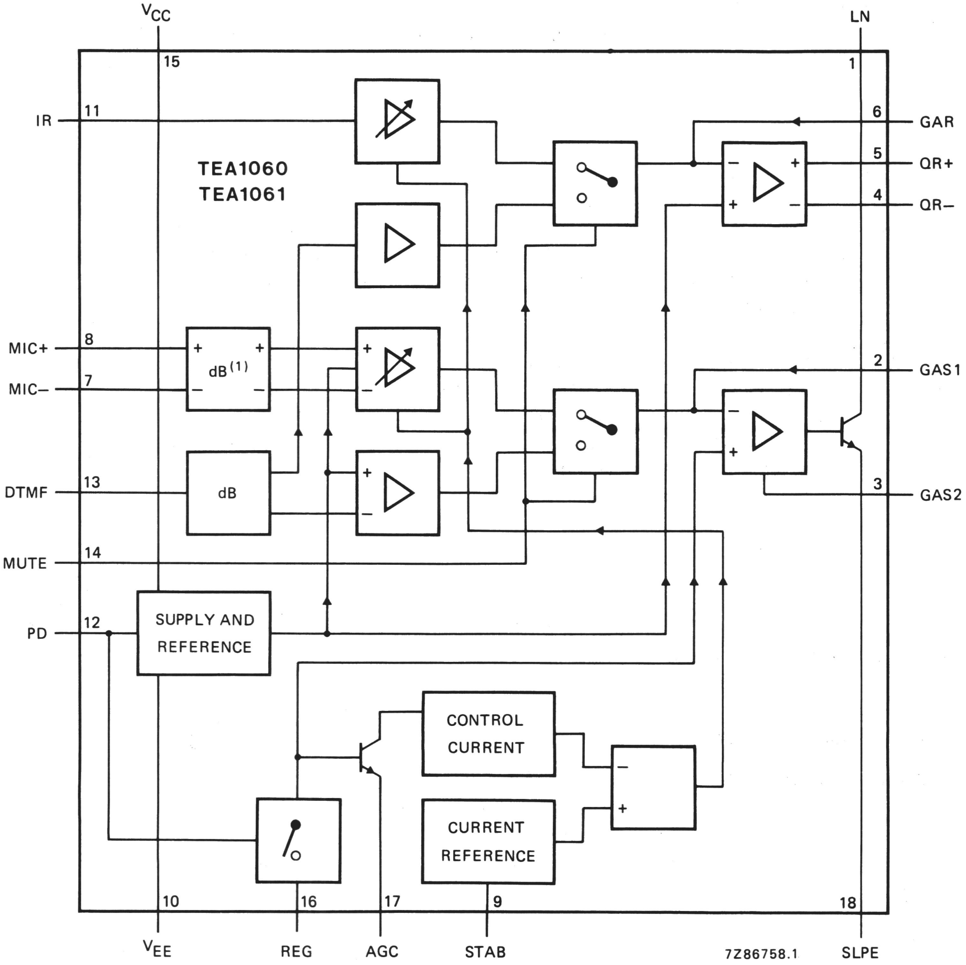

VCC
LN
15
1
IR
11
TEA1060
TEA1061
6
GAR
5
QR+
4
QR–
MIC+
8
MIC–
7
dB(1)
2
GAS1
DTMF
13
dB
3
GAS2
MUTE
14
PD
12
SUPPLY AND REFERENCE
CONTROL CURRENT
CURRENT REFERENCE
10
16
17
9
18
VEE
REG
AGC
STAB
7Z86758.1
SLPE

Fig.1 Block diagram.

The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

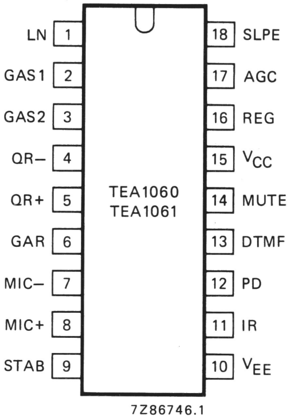


Fig.2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC−	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).

If the line current (I_{line}) exceeds the current I_{CC} + 0.5 mA required by the circuit itself (I_{CC} ca. 1 mA), plus the current I_P required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.
The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3} A - I_P) \times R9.$

V_{ref} being an internally generated temperature compensated reference voltage of 4.2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.
Under normal conditions $I_{SLPE} \gg I_{CC}$ + 0.5 mA + I_P. The static behaviour of the circuit then equals a 4.2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor connected between pins 1 and 16 (LN and REG) will decrease the internal reference voltage. R_{VA} connected between pins 16 and 18 (REG and SLPE) will increase the internal reference voltage.

Supply: V_{CC}, LN, SLPE, REG and STAB (continued)

The current I_P available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig.5 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, of which 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC– and gain adjustment connections GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.
The TEA1060 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 8.2 kΩ (2 x 4.1 kΩ) and its voltage amplification is typ. 52 dB.
The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage amplification is typ. 38 dB.
The arrangements with the microphone types mentioned are shown in Fig.6.

The gain of the microphone amplifier in both types can be adjusted over a range of + and –8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor (C6) of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig.7). The gain from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB and differential drive becomes possible.
This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of + and –8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability.
A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.8 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range. If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the antiside-tone network consisting of $R1//Z_{line}$, R2, R3, R8 and Z_{bal} (see Fig.11). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1[R3 + (R8//Z_{bal})]$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.

To obtain optimum side-tone-suppression, condition (b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor; k = (R8/R1)

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal} + R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} equals the average line impedance.

The anti-side-tone network as used in the standard application (Fig.11) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

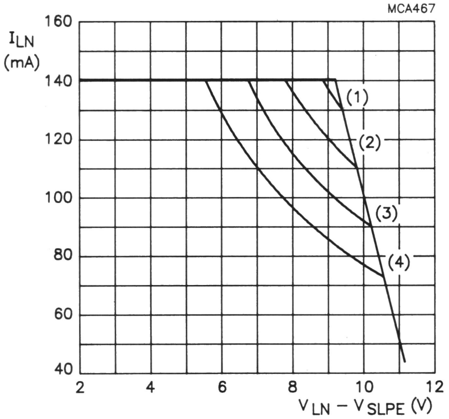
Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R10 = 13 Ω; R9 = 20 Ω; (see Fig.11)	V_{LN}	–	28	V
Line current TEA1060 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1061 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	$V_{CC} + 0.7$	V
		$-V_i$	–	0.7	V
Total power dissipation (2)		P_{tot}	–	769	mW
Storage temperature range		T_{stg}	–40	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

1. Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Fig.3).
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air
TEA1060 and TEA1061 $R_{th\ j\text{-}a}$ = 65 K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig.3 TEA1060/1061 safe operating area.

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C, R9 = 20 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)						
Voltage drop over circuit	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	–4	–2	0	mV/K
Voltage drop over circuit	I_{line} = 15 mA					
	$R_{VA} = R_{1\text{-}16}$ = 68 kΩ	V_{LN}	3.5	3.8	4.05	V
	$R_{VA} = R_{16\text{-}18}$ = 39 kΩ	V_{LN}	4.7	5.0	5.3	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.30	mA
	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH					
	I_P = 0 mA	V_{CC}	3.5	3.75	–	V
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
Microphone inputs MIC+ and MIC– (pins 7 and 8)						
Input impedance						
TEA1060		$\|Z_i\|$	3.3	4.1	4.9	kΩ
TEA1061		$\|Z_i\|$	16.5	20.4	24.5	kΩ
Common-mode rejection ratio						
TEA1060		k_{CMR}	–	82	–	dB
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060		G_v	51	52	53	dB
TEA1061		G_v	37	38	39	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	–0.5	±0.2	+0.5	dB
Variation with temperature referred to +25 °C	I_{line} = 50 mA; T_{amb} = –25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 13)						
Input impedance		$\lvert Z_i \rvert$	16.8	20.7	24.6	kΩ
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)						
Gain variation with R7 connected between pins 2 and 3; transmitting amplifier		ΔG_v	−8	–	+8	dB
Transmitting amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1.9	2.3	–	V
	d_{tot} = 10%	$V_{LN(rms)}$	–	2.6	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; pins 7 and 8 open circuit psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR (pin 11)						
Input impedance		$\lvert Z_i \rvert$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 4 and 5)						
Output impedance; single-ended		$\lvert Z_o \rvert$	–	4	–	Ω
Voltage gain from pin 11 to pin 4 or 5	I_{line} = 15 mA; R4 = 100 kΩ					
single-ended	R_L = 300 Ω	G_v	24	25	26	dB
differential	R_L = 600 Ω	G_v	30	31	32	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Variation with frequency referred to 800 Hz	f = 300 and 3400 Hz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 15 mA T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB
Output voltage	I_P = 0 mA; d_{tot} = 2%;					
sine-wave drive	R4 = 100 kΩ					
single-ended	R_L = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
single-ended	R_L = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	C_L = 47 nF					
R_{series} = 100 Ω	f = 3400 Hz	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; pin 11 open circuit psophometrically weighted (P53 curve)					
single-ended	R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)						
Gain variation with R4 connected between pins 6 and 5; receiving amplifier		ΔG_v	−8	–	+8	dB
MUTE input (pin 14)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Reduction of voltage gain from MIC+ and MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH R4 = 100 kΩ					
single-ended load	R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD (pin 12)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 17)						
Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 = 110 kΩ (connected between pins 17 and 10)						
Gain control range	I_{line} = 70 mA	$-\Delta G_v$	5.5	5.9	6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Lowest line current for lowest gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		$-\Delta G_v$	1.0	1.5	2.0	dB

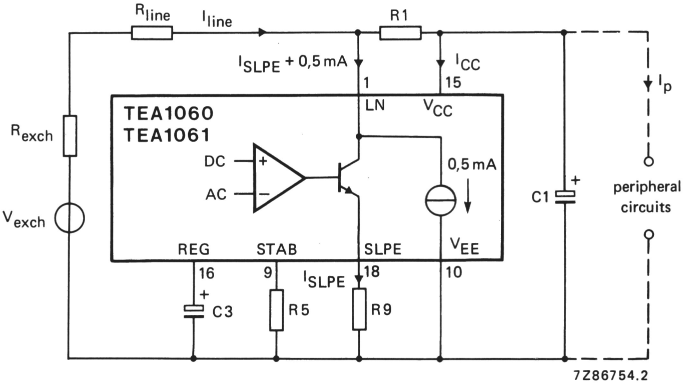
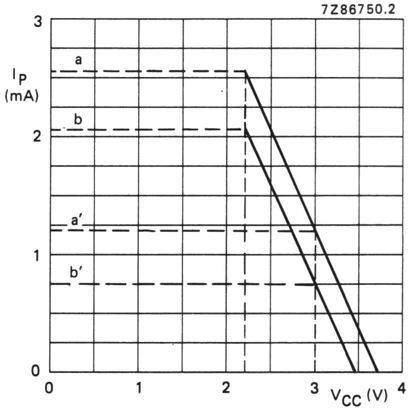

Rline
Iline
R1
ISLPE + 0,5 mA
ICC
Ip
1
15
LN
VCC
TEA1060
TEA1061
Rexch
DC
AC
0,5 mA
C1
peripheral circuits
Vexch
REG
STAB
SLPE
VEE
16
9
ISLPE
18
10
C3
R5
R9
7Z86754.2

Fig.4 Supply arrangement.



I_{line} = 15 mA at
V_{LN} = 4.45 V;
R1 = 620 Ω, R9 = 20 Ω

Fig.5 Maximum current I_P available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH. Curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven. $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).

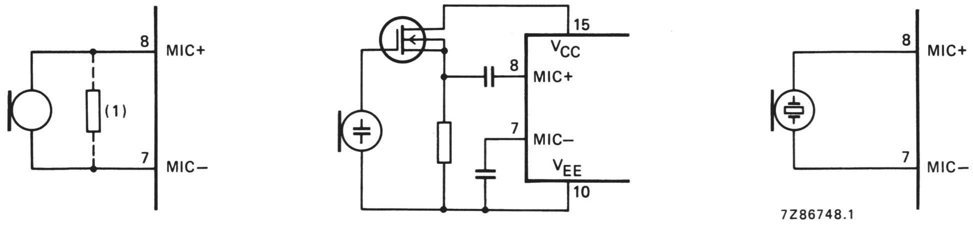

8
MIC+
(1)
7
MIC−
15
V_{CC}
8
MIC+
7
MIC−
V_{EE}
10
8
MIC+
7
MIC−
7Z86748.1

Fig.6 Alternative microphone arrangements: (a) magnetic or dynamic microphone for TEA1060, the resistor marked (1) may be connected to lower the terminating impedance, (b) electret microphone and (c) piezoelectric microphone for TEA1061.

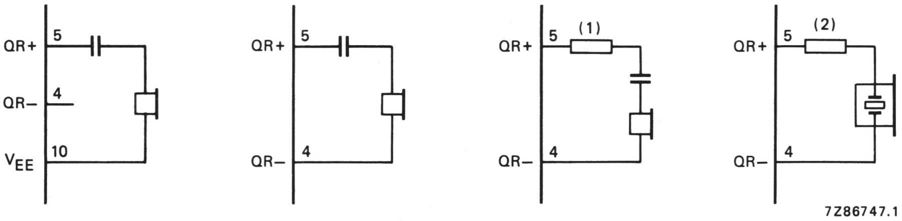

QR+
5
QR−
4
V_{EE}
10
QR+
5
QR−
4
QR+
5
(1)
QR−
4
QR+
5
(2)
QR−
4
7Z86747.1

Fig.7 Alternative receiver arrangements: (a) dynamic earpiece with less than 450 Ω impedance, (b) dynamic earpiece with more than 450 Ω impedance, (c) magnetic earpiece. The resistor marked (1) may be connected to prevent distortion [inductive load (d)] piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

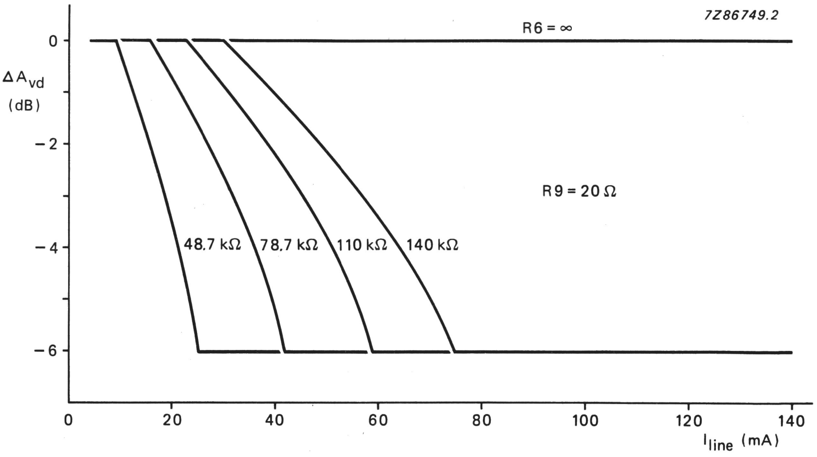


Fig.8 Variation of gain with line current with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

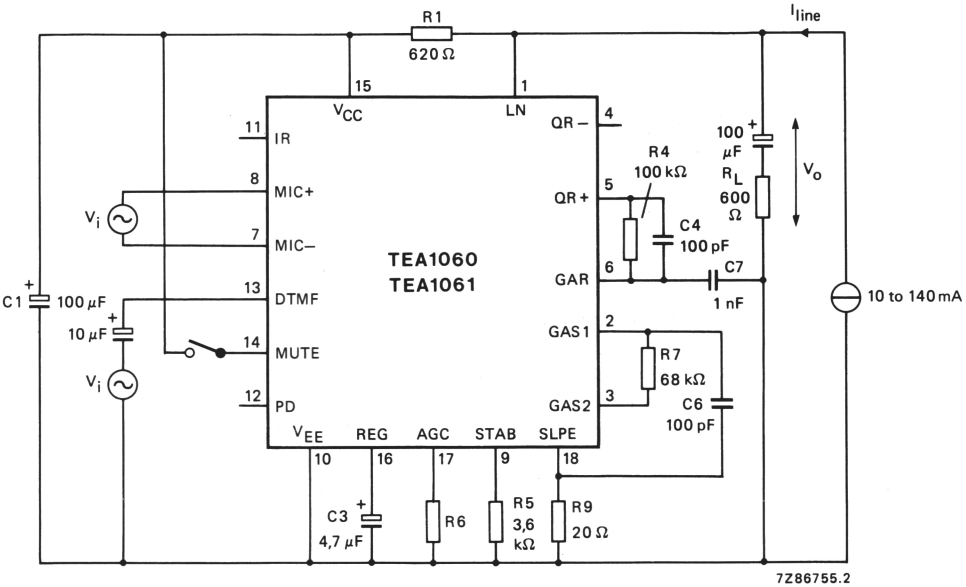

R1
620 Ω
I_{line}
15
1
V_{CC}
LN
11 IR
8 MIC+
7 MIC–
13 DTMF
14 MUTE
12 PD
4 QR –
5 QR +
6 GAR
2 GAS1
3 GAS2
TEA1060
TEA1061
V_i
V_i
C1 100 μF
10 μF
R4 100 kΩ
C4 100 pF
C7 1 nF
100 μF
R_L 600 Ω
V_o
10 to 140 mA
R7 68 kΩ
C6 100 pF
V_{EE} REG AGC STAB SLPE
10 16 17 9 18
C3 4,7 μF
R6
R5 3,6 kΩ
R9 20 Ω
7Z86755.2

Fig.9 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open circuit. For measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open circuit.

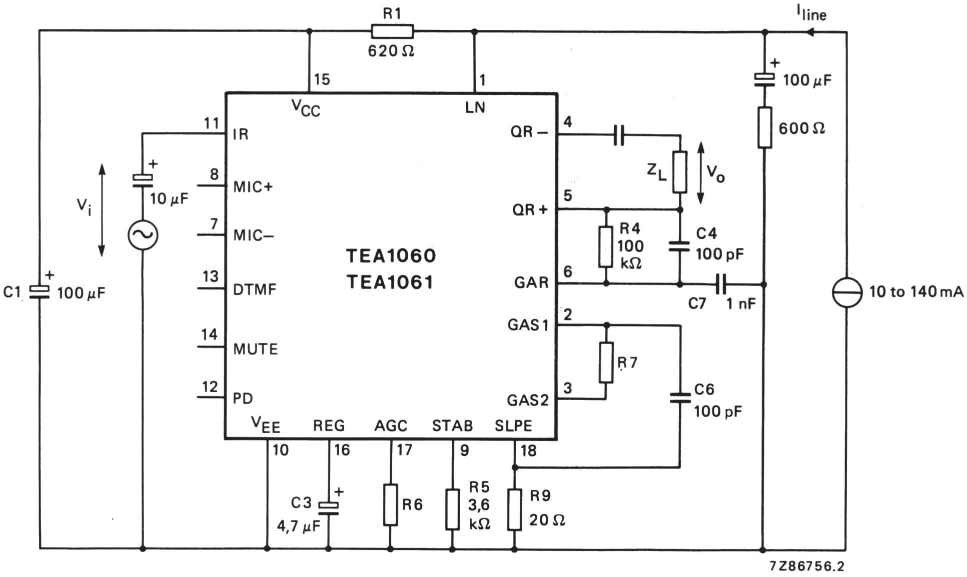

R1
620 Ω
I_{line}
15
1
V_{CC}
LN
11 IR
8 MIC+
7 MIC–
13 DTMF
14 MUTE
12 PD
4 QR –
5 QR +
6 GAR
2 GAS1
3 GAS2
TEA1060
TEA1061
V_i
10 μF
C1 100 μF
Z_L
V_o
R4 100 kΩ
C4 100 pF
C7 1 nF
100 μF
600 Ω
10 to 140 mA
R7
C6 100 pF
V_{EE} REG AGC STAB SLPE
10 16 17 9 18
C3 4,7 μF
R6
R5 3,6 kΩ
R9 20 Ω
7Z86756.2

Fig.10 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

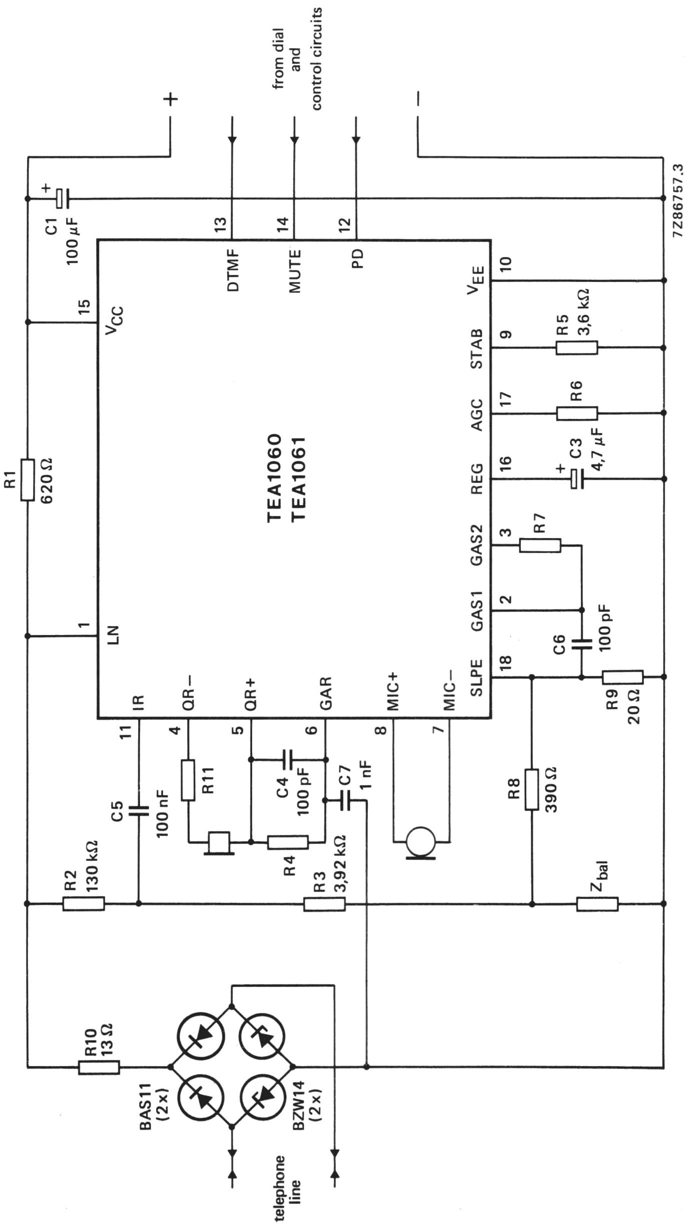

+
from dial
and
control circuits
−
7Z86757.3
C1
100 μF
R1
620 Ω
15
V_{CC}
13
DTMF
14
MUTE
12
PD
10
V_{EE}
9
STAB
R5
3,6 kΩ
17
AGC
R6
16
REG
C3
4,7 μF
3
GAS2
R7
2
GAS1
C6
100 pF
18
SLPE
R9
20 Ω
TEA1060
TEA1061
1
LN
11
IR
4
QR−
5
QR+
6
GAR
8
MIC+
7
MIC−
C5
100 nF
R11
C4
100 pF
C7
1 nF
R4
R8
390 Ω
R2
130 kΩ
R3
3,92 kΩ
Z_{bal}
R10
13 Ω
BAS11
(2x)
BZW14
(2x)
telephone
line

Fig.11 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

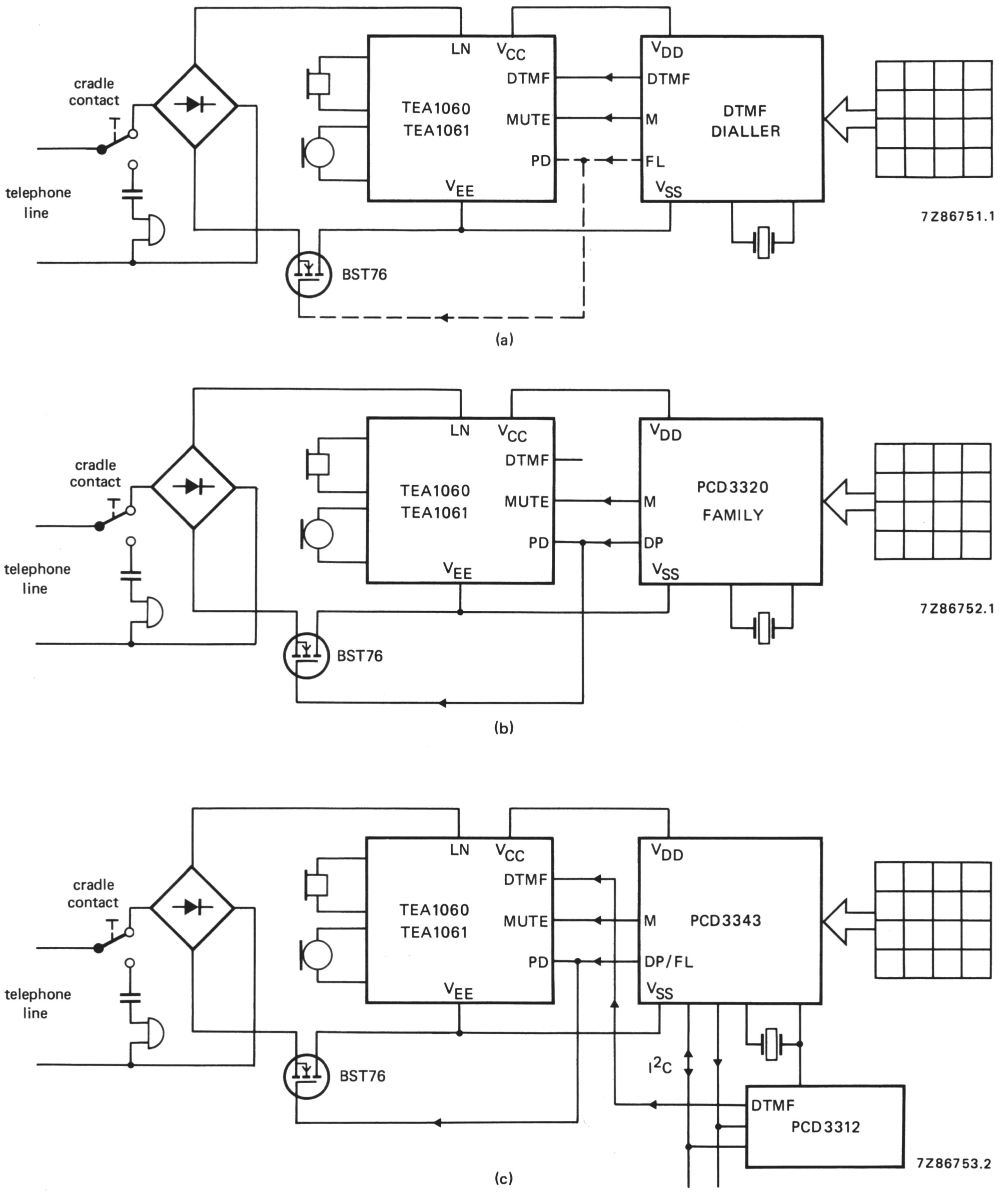

cradle contact
telephone line
LN
V_{CC}
DTMF
MUTE
PD
V_{EE}
TEA1060
TEA1061
V_{DD}
DTMF
M
FL
V_{SS}
DTMF DIALLER
BST76
7Z86751.1
(a)
cradle contact
telephone line
LN
V_{CC}
DTMF
MUTE
PD
V_{EE}
TEA1060
TEA1061
V_{DD}
M
DP
V_{SS}
PCD3320 FAMILY
BST76
7Z86752.1
(b)
cradle contact
telephone line
LN
V_{CC}
DTMF
MUTE
PD
V_{EE}
TEA1060
TEA1061
V_{DD}
M
DP/FL
V_{SS}
PCD3343
I^2C
DTMF
PCD3312
BST76
7Z86753.2
(c)

Fig.12 Typical applications of the TEA1060 or TEA1061 (simplified): (a) DTMF set with a CMOS DTMF dialling circuit, the dashed lines show an optional flash (register recall by timed loop break); (b) Pulse dial set with the one of the PCD3320 family of CMOS interrupted current-loop dialling circuits; (c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus.

COMPARISON OF TRANSMISSION ICs

	60	61	64	66T	67	68
Microphones						
low sensitivity dynamic or magnetic	*			*		*
medium sensitivity magnetic or dynamic	*		*	*	*	*
electret with preamplifier		*	*	*	*	*
piezo electric		*	*	*	*	*
very accurate microphone matching			*		*	*
dynamic limiter			*			
Receivers						
dynamic or magnetic or piezo (17-39 dB)	*	*		*		*
dynamic or magnetic or piezo (20-45 dB)			*		*	
Power-down input	*	*	*	*	*	*
DTMF and mute inputs	*	*	*	*	*	*
Voltage regulator						
adjustable DC voltage/resistance	*	*	*	*	*	*
parallel operation			*		*	
Peripheral supply						
unregulated - limited power	*	*		*	*	*
unregulated - extended power			*			
stabilized - extended power			*			
Automatic line loss compensation AGC	*	*	*	*	*	*

Low voltage transmission circuit with dialler interface

TEA1062; TEA1062A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides a supply for external circuits
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
  - TEA1062: active HIGH (MUTE)
  - TEA1062A: active LOW ($\overline{\text{MUTE}}$)
- Receiving amplifier for dynamic, magnetic or piezoelectric earpieces
- Large gain setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers
- Gain control curve adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1062 and TEA1062A are integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between dialling and speech. The ICs operate at line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel.

All statements and values refer to all versions unless otherwise specified.

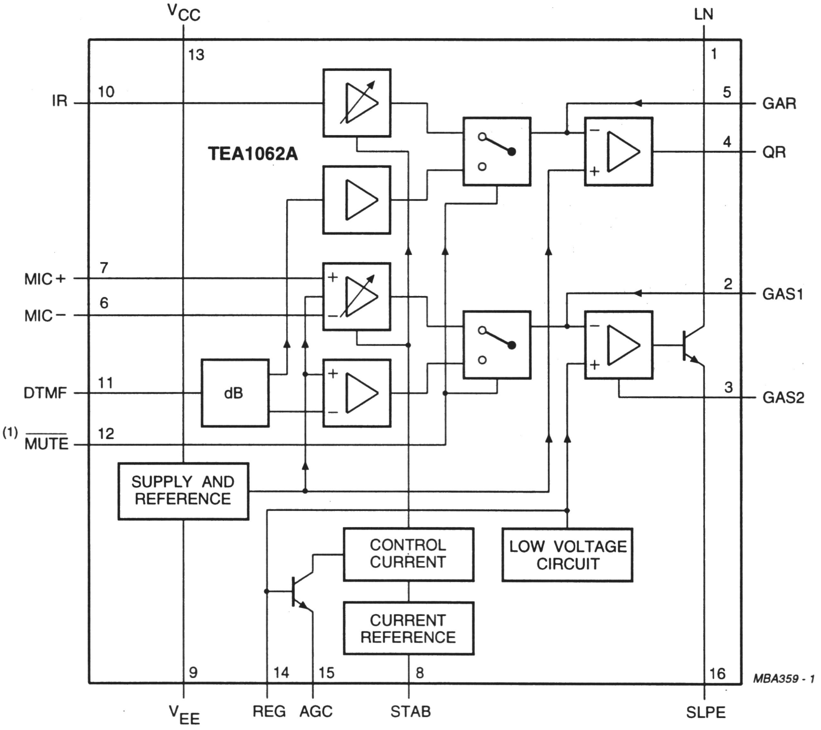
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	3.55	4.0	4.25	V
I_{line}	operating line current					
	normal operation		11	–	140	mA
	with reduced performance		1	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA				
	TEA1062	I_p = 1.2 mA; MUTE = HIGH	2.2	2.7	–	V
		I_p = 0 mA; MUTE = HIGH	–	3.4	–	V
	TEA1062A	I_p = 1.2 mA; $\overline{\text{MUTE}}$ = LOW	2.2	2.7	–	V
		I_p = 0 mA; $\overline{\text{MUTE}}$ = LOW	–	3.4	–	V
G_v	voltage gain					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	31	dB
T_{amb}	operating ambient temperature		–25	–	+75	°C
Line loss compensation						
ΔG_v	gain control		–	5.8	–	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		0.4	–	1	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1062	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062M1	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1062A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TEA1062AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM


VCC
13
LN
1
IR
10
TEA1062A
5
GAR
4
QR
MIC+
7
MIC−
6
2
GAS1
DTMF
11
dB
3
GAS2
(1) MUTE
12
SUPPLY AND REFERENCE
CONTROL CURRENT
LOW VOLTAGE CIRCUIT
CURRENT REFERENCE
9
14
15
8
16
VEE
REG
AGC
STAB
SLPE
MBA359 - 1

(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.1 Block diagram for TEA1062A.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR	4	non-inverting output; receiving amplifier
GAR	5	gain adjustment; receiving amplifier
MIC−	6	inverting microphone input
MIC+	7	non-inverting microphone input
STAB	8	current stabilizer
V_{EE}	9	negative line terminal
IR	10	receiving amplifier input
DTMF	11	dual-tone multi-frequency input
$\overline{\text{MUTE}}$	12	mute input (see note 1)
V_{CC}	13	positive supply decoupling
REG	14	voltage regulator decoupling
AGC	15	automatic gain control input
SLPE	16	slope (DC resistance) adjustment

Note

1. Pin 12 is active HIGH (MUTE) for TEA1062.

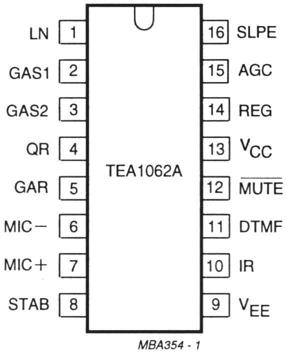

LN 1
GAS1 2
GAS2 3
QR 4
GAR 5
MIC− 6
MIC+ 7
STAB 8
16 SLPE
15 AGC
14 REG
13 V_{CC}
12 $\overline{\text{MUTE}}$
11 DTMF
10 IR
9 V_{EE}
TEA1062A
MBA354 - 1

Fig.2 Pin configuration for TEA1062A.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, LN, SLPE, REG and STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line. The supply voltage is derived from the line via a dropping resistor and regulated by the IC. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE}. The internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch} and the DC resistance of the telephone line R_{line}.

The circuit has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig.9). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.

The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

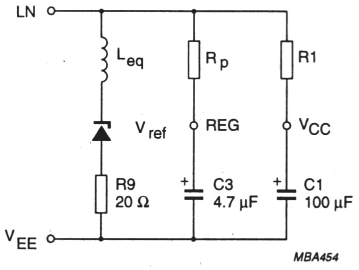
$$V_{LN} = V_{ref} + \{(I_{line} - I_{CC} - 0.5 \times 10^{-3}\ A) - I_p\} \times R9$$

V_{ref} is an internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}.

In normal use the value of R9 would be 20 Ω.

Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, sidetone level, maximum output swing on LN and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 3.7 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig.3 shows the equivalent impedance of the circuit.



$L_{eq} = C3 \times R9 \times R_p$.
$R_p = 16.2\ k\Omega$.

Fig.3 Equivalent impedance circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor when connected between LN and REG will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig.10 shows this current for V_{CC} > 2.2 V. If MUTE is LOW (TEA1062) or $\overline{\text{MUTE}}$ is HIGH (TEA1062A) when the receiving amplifier is driven, the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1 as shown in Fig.19 and Fig.20, or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE (Fig.18).

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Figures 14 and 15). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.11.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2.

Stability is ensured by two external capacitors, C6 connected between GAS1 and SLPE and C8 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C8 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 × C6.

Input MUTE (TEA1062)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Input $\overline{\text{MUTE}}$ (TEA1062A)

When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when $\overline{\text{MUTE}}$ is HIGH. $\overline{\text{MUTE}}$ switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the DTMF amplifier becomes active independent to the DC level applied to the $\overline{\text{MUTE}}$ input.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier IR, QR and GAR

The receiving amplifier has one input (IR) and a non-inverting output (QR). Earpiece arrangements are illustrated in Fig.12. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by subtracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 × C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic Gain Control input AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}.

The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km). Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.13 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line-loss compensation is required the AGC pin may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Sidetone suppression

The anti-sidetone network, R1//Z_{line}, R2, R3, R8, R9 and Z_{bal}, (see Fig.4) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1 \times \left(R3 + \frac{R8 \times Z_{bal}}{R8 + Z_{bal}} \right) \qquad (1)$$

$$\frac{Z_{bal}}{Z_{bal} + R8} = \frac{Z_{line}}{Z_{line} + R1} \qquad (2)$$

If fixed values are chosen for R1, R2, R3 and R9, then condition (1) will always be fulfilled when $|R8//Z_{bal}| << R3$.

To obtain optimum sidetone suppression, condition (2) has to be fulfilled which results in:

$$Z_{bal} = \frac{R8}{R1} \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; $k = \frac{R8}{R1}$

The scale factor k, dependent on the value of R8, is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| << R3$ fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain.

In practise Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

EXAMPLE

The balance impedance Z_{bal} at which the optimum suppression is present can be calculated by:

Suppose Z_{line} = 210 Ω + (1265 Ω//140 nF) representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).

When k = 0.64 then R8 = 390 Ω;
Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier.
The attenuation is almost constant over the whole audio-frequency range.

Figure 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication *"TEA1060 Family versatile speech transmission ICs for electronic telephone sets, order number 9398 341 10011")*.

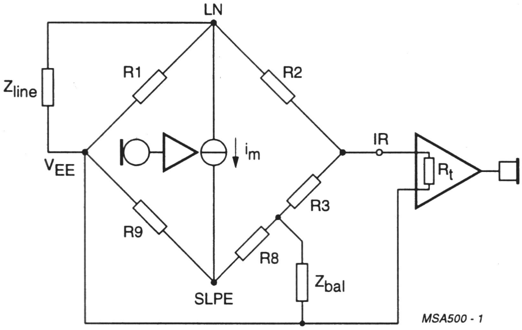

LN
R1
R2
Zline
VEE
im
IR
Rt
R3
R9
R8
Zbal
SLPE
MSA500 - 1

Fig.4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

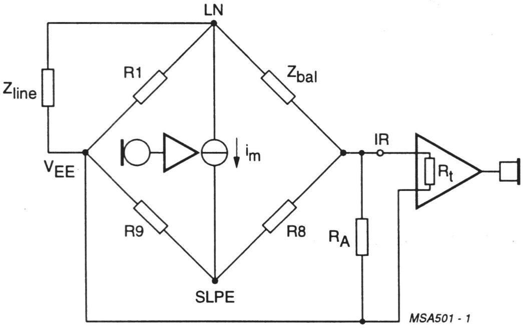

LN
R1
Zbal
Zline
VEE
im
IR
Rt
R9
R8
RA
SLPE
MSA501 - 1

Fig.5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.18	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1			
	TEA1062; TEA1062A		–	140	mA
	TEA1062T; TEA1062AT		–	140	mA
V_I	input voltage on all other pins	positive input voltage	–	V_{CC} + 0.7	V
		negative input voltage	–	–0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1062; TEA1062A		–	666	mW
	TEA1062M1		–	617	mW
	TEA1062T; TEA1062AT		–	454	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes

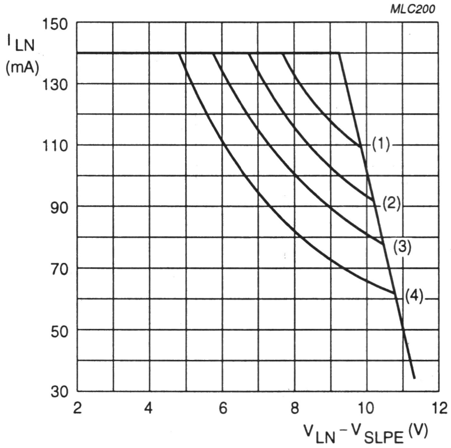
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Figs 6, 7 and 8).
2. Calculated for the maximum ambient temperature specified (T_{amb} = 75 °C) and a maximum junction temperature of 125 °C.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1062; TEA1062A	75	K/W
	TEA1062M1	81	K/W
	TEA1062T; TEA1062AT (note 1)	110	K/W

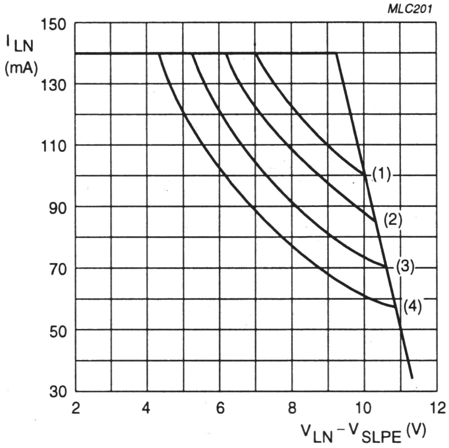
Note

1. Mounted on glass epoxy board 28.5 × 19.1 × 1.5 mm.



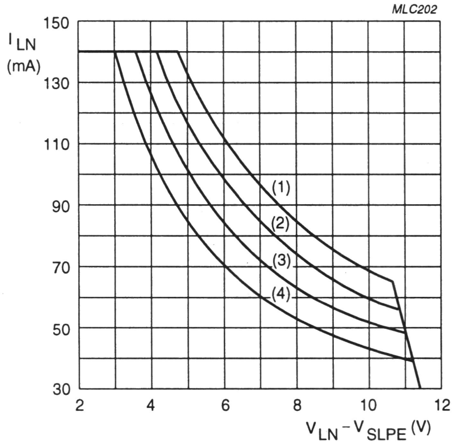
(1) T_{amb} = 45 °C; P_{tot} = 1068 mW.
(2) T_{amb} = 55 °C; P_{tot} = 934 mW.
(3) T_{amb} = 65 °C; P_{tot} = 800 mW.
(4) T_{amb} = 75 °C; P_{tot} = 666 mW.

Fig.6 TEA1062 and TEA1062A safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 988 mW.
(2) T_{amb} = 55 °C; P_{tot} = 864 mW.
(3) T_{amb} = 65 °C; P_{tot} = 741 mW.
(4) T_{amb} = 75 °C; P_{tot} = 617 mW.

Fig.7 TEA1062M1 safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 727 mW.
(2) T_{amb} = 55 °C; P_{tot} = 636 mW.
(3) T_{amb} = 65 °C; P_{tot} = 545 mW.
(4) T_{amb} = 75 °C; P_{tot} = 454 mW.

Fig.8 TEA1062T and TEA1062AT safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 13)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	MIC inputs open-circuit				
		I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	1.9	–	V
		I_{line} = 15 mA	3.55	4.0	4.25	V
		I_{line} = 100 mA	4.9	5.7	6.5	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–	−0.3	–	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	–	3.5	–	V
		R_{VA} (REG to SLPE) = 39 kΩ	–	4.5	–	V
I_{CC}	supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH				
	TEA1062	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; $\overline{\text{MUTE}}$ = LOW				
	TEA1062A	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
Microphone inputs MIC− and MIC+ (pins 6 and 7)						
$\lvert Z_i \rvert$	input impedance					
	differential	between MIC− and MIC+	–	64	–	kΩ
	single-ended	MIC− or MIC+ to V_{EE}	–	32	–	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain MIC+ or MIC− to LN	I_{line} = 15 mA; R7 = 68 kΩ	50.5	52.0	53.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 and +75 °C	–	±0.2	–	dB
DTMF input (pin 11)						
$\lvert Z_i \rvert$	input impedance		–	20.7	–	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.0	25.5	27.0	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	–	±0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain variation by adjustment of R7 between GAS1 and GAS2		–8	–	0	dB
Sending amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	THD = 10%				
		I_{line} = 4 mA	–	0.8	–	V
		I_{line} = 15 mA	1.7	2.3	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	–	–69	–	dBmp
Receiving amplifier input IR (pin 10)						
$\lvert Z_i \rvert$	input impedance		–	21	–	kΩ
Receiving amplifier output QR (pin 4)						
$\lvert Z_o \rvert$	output impedance		–	4	–	Ω
G_v	voltage gain from IR to QR	I_{line} = 15 mA; R_L = 300 Ω (from pin 9 to pin 4)	29.5	31	32.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB
$V_{o(rms)}$	output voltage (RMS value)	THD = 2%; sine wave drive; R4 = 100 kΩ; I_{line} = 15 mA; I_p = 0 mA				
		R_L = 150 Ω	0.22	0.33	–	V
		R_L = 450 Ω	0.3	0.48	–	V
$V_{o(rms)}$	output voltage (RMS value)	THD = 10%; R4 = 100 kΩ; R_L = 150 Ω; I_{line} = 4 mA	–	15	–	mV
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve); R_L = 300 Ω	–	50	–	µV
Gain adjustment input GAR (pin 5)						
ΔG_v	receiving amplifier gain variation by adjustment of R4 between GAR and QR		–11	–	0	dB
Mute input (pin 12)						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{MUTE}	input current		–	8	15	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reduction of gain						
ΔG_v	MIC+ or MIC– to LN					
	TEA1062	MUTE = HIGH	–	70	–	dB
	TEA1062A	$\overline{\text{MUTE}}$ = LOW	–	70	–	dB
G_v	voltage gain from DTMF to QR	R4 = 100 kΩ; R_L = 300 Ω				
	TEA1062	MUTE = HIGH	–	–17	–	dB
	TEA1062A	$\overline{\text{MUTE}}$ = LOW	–	–17	–	dB
Automatic gain control input AGC (pin 15)						
ΔG_v	controlling the gain from IR to QR and the gain from MIC+, MIC– to LN gain control range	R6 = 110 kΩ (between AGC and V_{EE}) I_{line} = 70 mA	–	–5.8	–	dB
I_{lineH}	highest line current for maximum gain		–	23	–	mA
I_{lineL}	lowest line current for minimum gain		–	61	–	mA

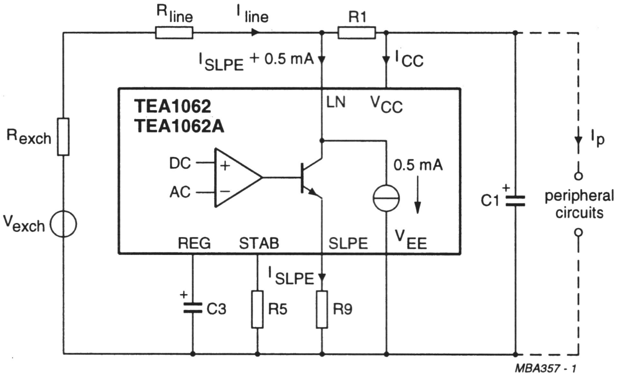
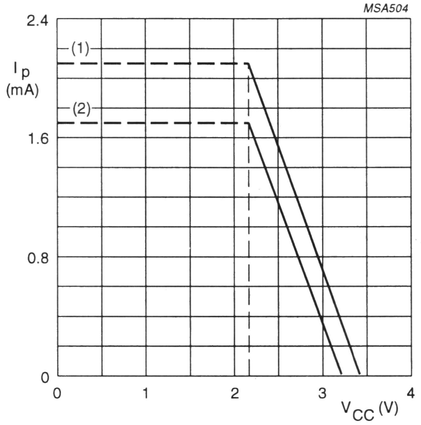

Rline
Iline
R1
ISLPE + 0.5 mA
ICC
TEA1062
TEA1062A
LN
VCC
Rexch
DC
AC
0.5 mA
Ip
C1
peripheral circuits
Vexch
REG
STAB
SLPE
VEE
ISLPE
C3
R5
R9
MBA357 - 1

Fig.9 Supply arrangement.



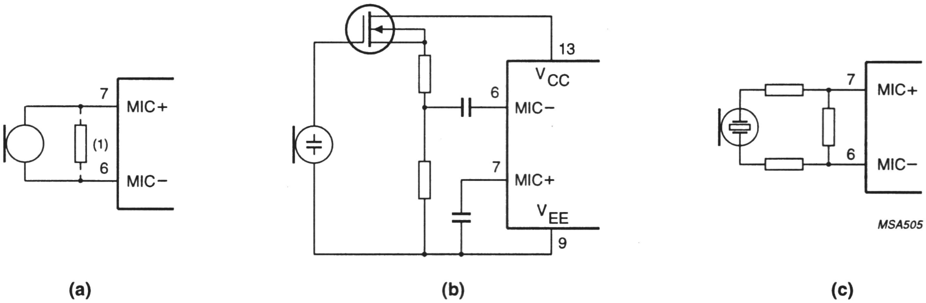
The supply possibilities can be increased by setting the voltage drop over the circuit V_{LN} to a higher value by resistor R_{VA} connected between REG and SLPE.

$V_{CC} > 2.2$ V; $I_{line} = 15$ mA at $V_{LN} = 4$ V; R1 = 620 Ω; R9 = 20 Ω.

(1) $I_p = 2.1$ mA. Is valid when the receiving amplifier is not driven or when MUTE = HIGH (TEA1062), $\overline{\text{MUTE}}$ = LOW (TEA1062A).

(2) $I_p = 1.7$ mA. Is valid when MUTE = LOW (TEA1062), $\overline{\text{MUTE}}$ = HIGH (TEA1062A) and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150$ Ω.

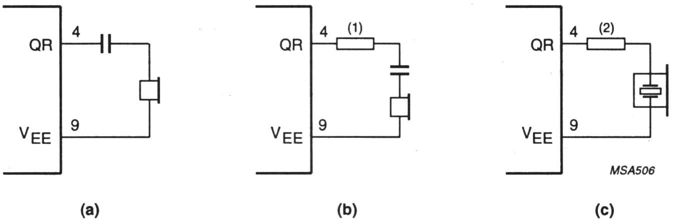
Fig.10 Typical current I_p available from V_{CC} for peripheral circuitry.


7
MIC+
(1)
6
MIC−
13
VCC
6
MIC−
7
MIC+
VEE
9
7
MIC+
6
MIC−
MSA505
(a)
(b)
(c)

(a) Magnetic or dynamic microphone.
(b) Electret microphone.
(c) Piezoelectric microphone.

(1) Resistor may be connected to reduce the terminating impedance.

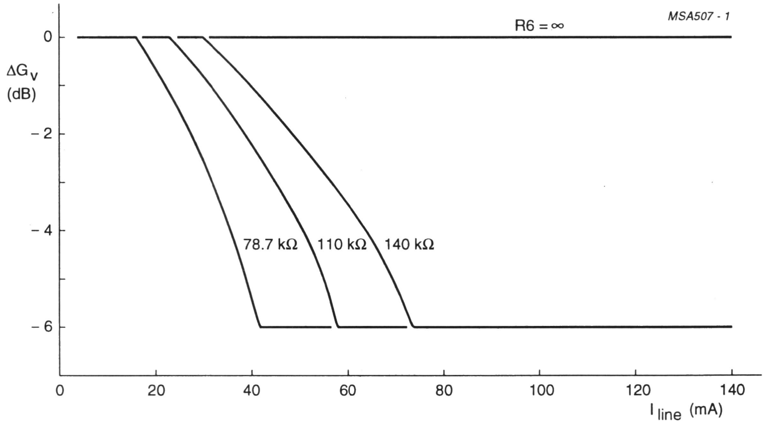
Fig.11 Alternative microphone arrangements.


QR
4
VEE
9
QR
4
(1)
VEE
9
QR
4
(2)
VEE
9
MSA506
(a)
(b)
(c)

(a) Dynamic earpiece.
(b) Magnetic earpiece.
(c) Piezoelectric earpiece.

(1) Resistor may be connected to prevent distortion (inductive load).
(2) Resistor is required to increase the phase margin (capacitive load).

Fig.12 Alternative receiver arrangements.

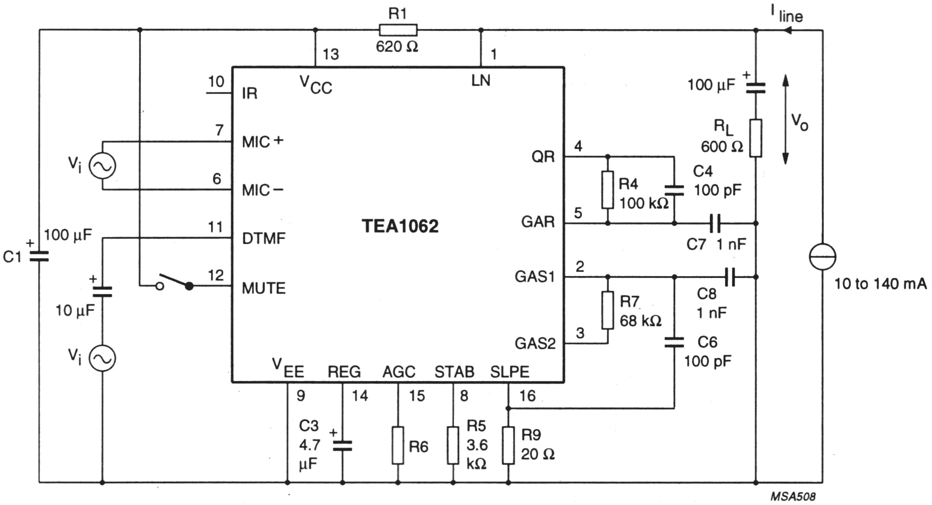


R9 = 20 Ω.

Fig.13 Variation of gain as a function of line current with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
36	100	78.7	−	−
48	140	110	93.1	82
60	−	−	120	102


R1
620 Ω
I_{line}
13
1
10
IR
V_{CC}
LN
100 µF
R_L
600 Ω
V_o
7
MIC+
V_i
6
MIC−
QR
4
R4
100 kΩ
C4
100 pF
5
GAR
TEA1062
11
DTMF
C1
100 µF
C7 1 nF
12
MUTE
GAS1
2
C8
1 nF
10 µF
R7
68 kΩ
10 to 140 mA
V_i
GAS2
3
C6
100 pF
V_{EE}
REG
AGC
STAB
SLPE
9
14
15
8
16
C3
4.7
µF
R6
R5
3.6
kΩ
R9
20 Ω
MSA508

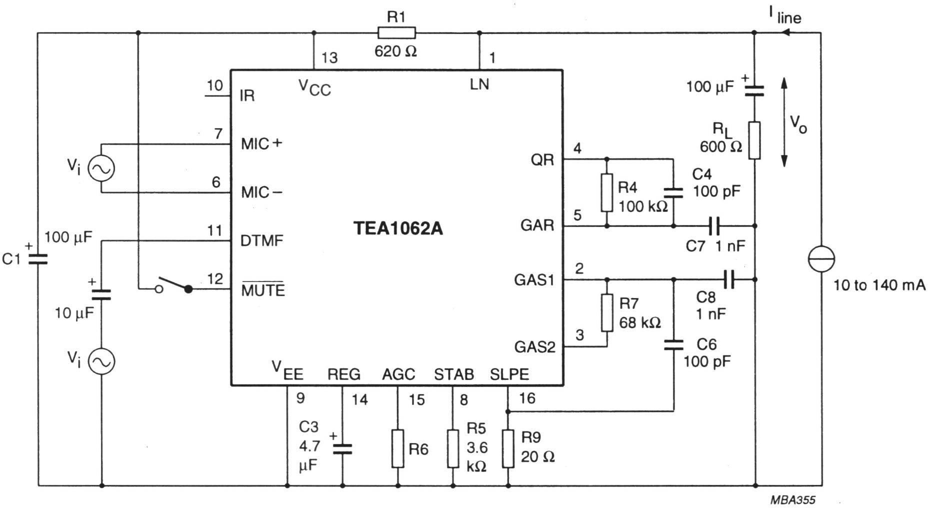
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

For measuring gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit.

For measuring the DTMF input, the MUTE input should be HIGH.

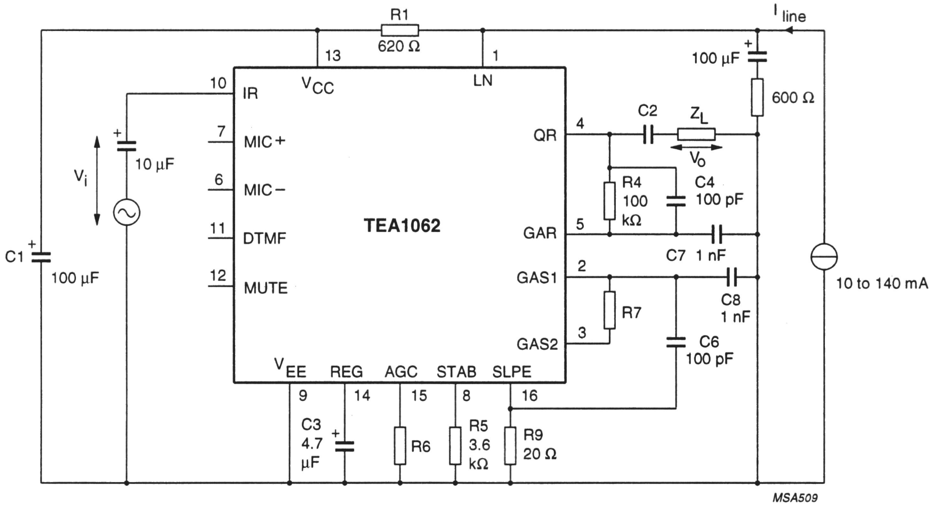
Inputs not being tested should be open-circuit.

Fig.14 Test circuit for defining TEA1062 voltage gain of MIC+, MIC− and DTMF inputs.


R1
620 Ω
I line
13
1
10
IR
VCC
LN
100 µF
7
MIC +
RL
600 Ω
Vo
Vi
QR
4
C4
100 pF
6
MIC –
R4
100 kΩ
11
TEA1062A
GAR
5
100 µF
DTMF
C7 1 nF
C1
2
12
GAS1
MUTE
C8
1 nF
10 µF
R7
68 kΩ
10 to 140 mA
3
GAS2
C6
100 pF
Vi
VEE
REG
AGC
STAB
SLPE
9
14
15
8
16
C3
4.7
µF
R6
R5
3.6
kΩ
R9
20 Ω
MBA355

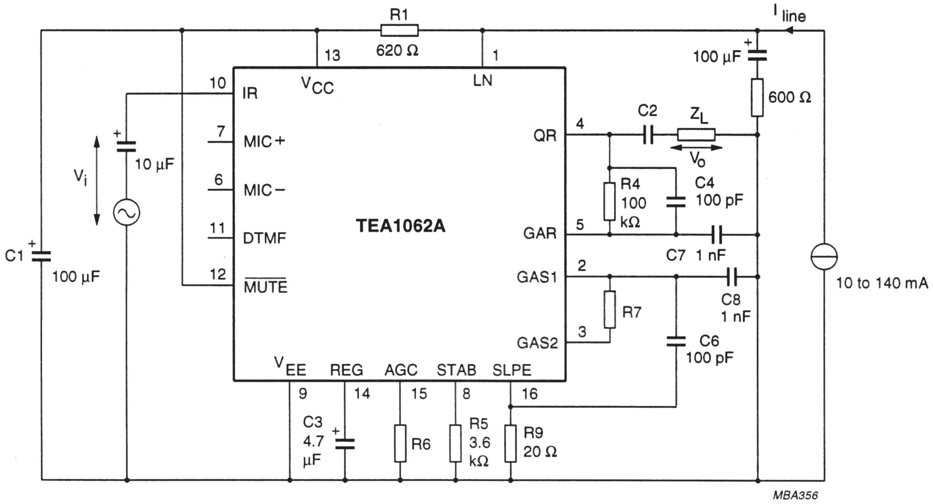
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.
For measuring gain from MIC+ and MIC– the $\overline{\text{MUTE}}$ input should be HIGH.
For measuring the DTMF input, the $\overline{\text{MUTE}}$ input should be LOW or open-circuit.
Inputs not being tested should be open-circuit.

Fig.15 Test circuit for defining TEA1062A voltage gain of MIC+, MIC– and DTMF inputs.


R1
620 Ω
13
1
I line
100 µF
600 Ω
10
IR
VCC
LN
7
MIC+
6
MIC−
11
DTMF
12
MUTE
TEA1062
QR
GAR
GAS1
GAS2
4
5
2
3
C2
ZL
Vo
R4
100 kΩ
C4
100 pF
C7 1 nF
C8
1 nF
R7
C6
100 pF
Vi
10 µF
C1
100 µF
10 to 140 mA
VEE
REG
AGC
STAB
SLPE
9
14
15
8
16
C3
4.7 µF
R6
R5
3.6 kΩ
R9
20 Ω
MSA509

Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

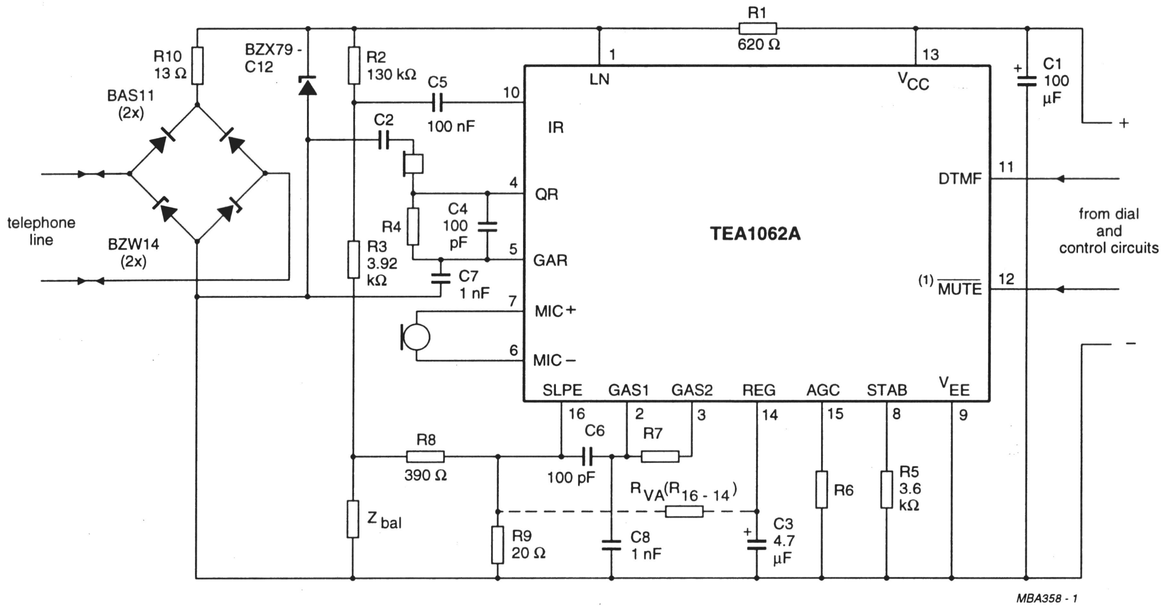
Fig.16 Test circuit for defining TEA1062 voltage gain of the receiving amplifier.


R1
620 Ω
13
1
I line
100 µF
600 Ω
10
IR
VCC
LN
7
MIC+
6
MIC−
11
DTMF
12
$\overline{\text{MUTE}}$
TEA1062A
QR
GAR
GAS1
GAS2
4
5
2
3
C2
ZL
Vo
R4
100 kΩ
C4
100 pF
C7 1 nF
C8
1 nF
R7
C6
100 pF
Vi
10 µF
C1
100 µF
10 to 140 mA
VEE
REG
AGC
STAB
SLPE
9
14
15
8
16
C3
4.7 µF
R6
R5
3.6 kΩ
R9
20 Ω
MBA356

Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

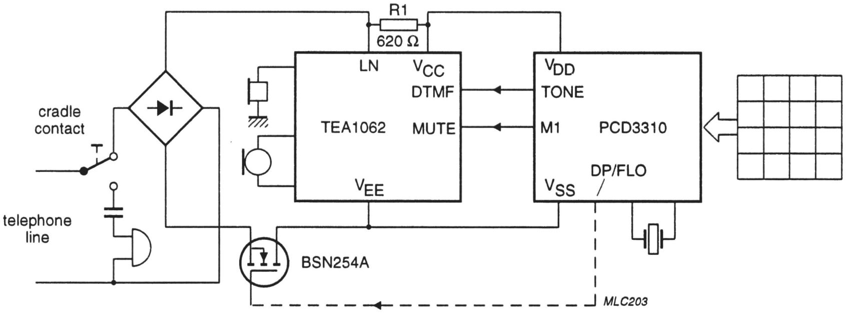
Fig.17 Test circuit for defining TEA1062A voltage gain of the receiving amplifier.

APPLICATION INFORMATION


R1
620 Ω
R10
13 Ω
BZX79 -
C12
R2
130 kΩ
C5
100 nF
10
1
LN
13
VCC
C1
100
µF
+
BAS11
(2x)
C2
IR
4
QR
DTMF
11
from dial
and
control circuits
telephone
line
BZW14
(2x)
R4
C4
100
pF
R3
3.92
kΩ
5
GAR
TEA1062A
(1) MUTE
12
C7
1 nF
7
MIC+
6
MIC−
−
SLPE
GAS1
GAS2
REG
AGC
STAB
VEE
16
2
3
14
15
8
9
R8
390 Ω
C6
100 pF
R7
RVA(R16 - 14)
R6
R5
3.6
kΩ
Z bal
R9
20 Ω
C8
1 nF
C3
4.7
µF
MBA358 - 1

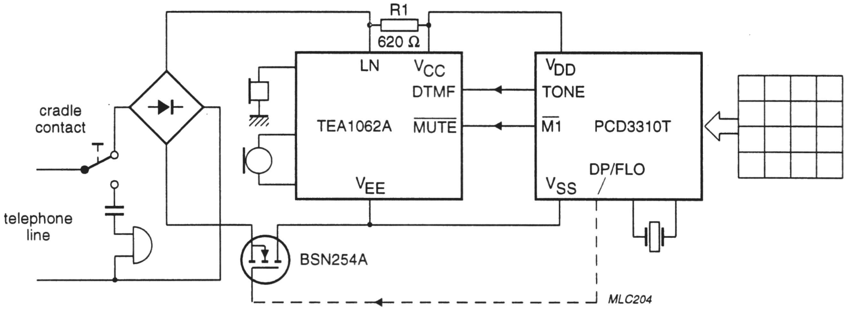
The diode bridge, the Zener diode and R10 limit the current into, and the voltage across, the circuit during line transients.
A different protection arrangement is required for pulse dialling or register recall.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).
Further application information can be found in Application note *"ETT/AN 89008"*.
(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.18 Typical application of TEA1062A, with piezoelectric earpiece and DTMF dialling.


R1
620 Ω
LN
V_{CC}
DTMF
TEA1062
MUTE
V_{EE}
V_{DD}
TONE
M1
PCD3310
DP/FLO
V_{SS}
cradle contact
telephone line
BSN254A
MLC203

(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310. The dashed line shows an optional flash (register recall by timed loop break).

Fig.19 Typical simplified application of the TEA1062.


R1
620 Ω
LN
V_{CC}
DTMF
TEA1062A
$\overline{\text{MUTE}}$
V_{EE}
V_{DD}
TONE
$\overline{\text{M1}}$
PCD3310T
DP/FLO
V_{SS}
cradle contact
telephone line
BSN254A
MLC204

(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310T. The dashed line shows an optional flash (register recall by timed loop break).

Fig.20 Typical simplified application of the TEA1062A.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE AND TRANSMIT LEVEL DYNAMIC LIMITING

GENERAL DESCRIPTION

The TEA1064A is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech and has a powerful DC supply for peripheral circuits. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

Features

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits in two options:
  unregulated supply, regulated line voltage;
  stabilized supply, line voltage varies with supply current
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for magnetic, dynamic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch

PACKAGE OUTLINES

TEA1064A : 20-lead DIL; plastic (SOT146).
TEA1064AT: 20-lead mini-pack; plastic (SO20; SOT163A).

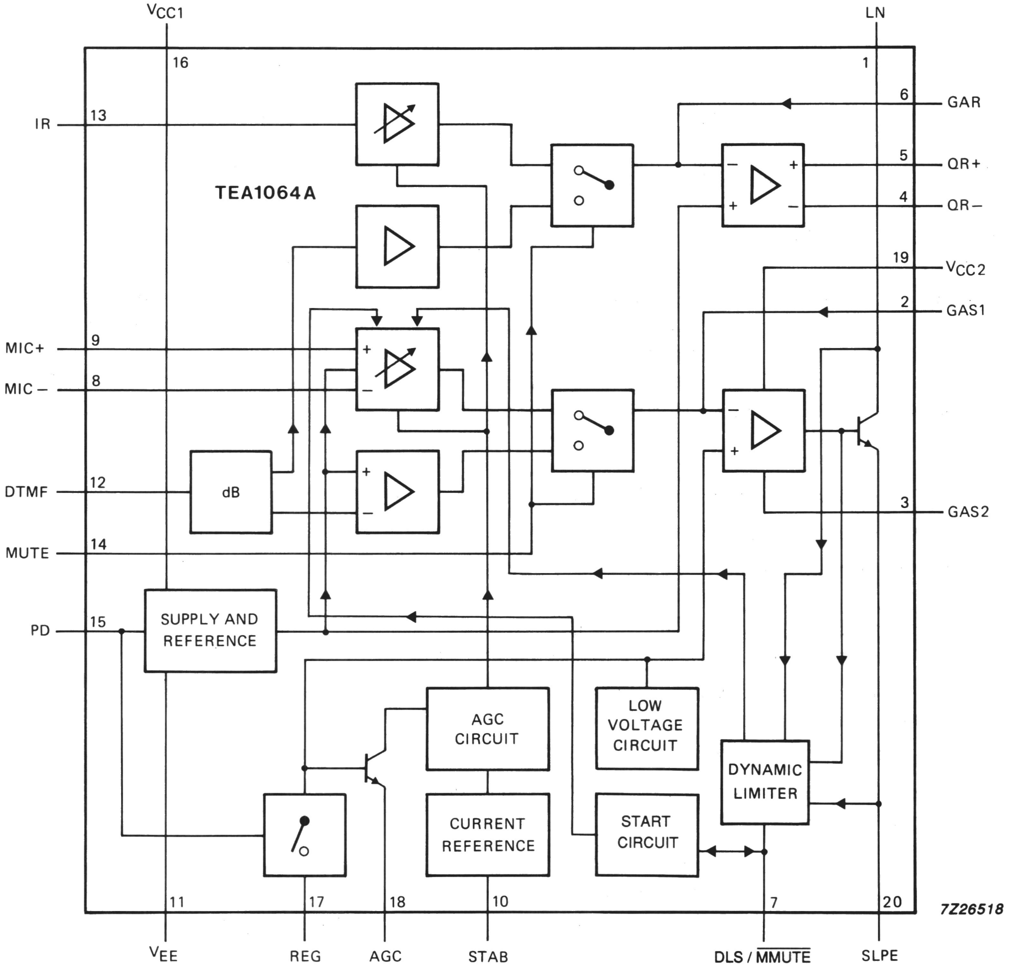

VCC1
16
LN
1
6
GAR
IR
13
5
QR+
4
QR−
TEA1064A
19
VCC2
2
GAS1
MIC+
9
MIC −
8
DTMF
12
dB
3
GAS2
MUTE
14
PD
15
SUPPLY AND REFERENCE
AGC CIRCUIT
LOW VOLTAGE CIRCUIT
DYNAMIC LIMITER
CURRENT REFERENCE
START CIRCUIT
11
17
18
10
7
20
7Z26518
VEE
REG
AGC
STAB
DLS / MMUTE
SLPE

Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating ambient temperature range		T_{amb}	−25	−	+ 75	°C
Line current operating range:						
normal operation		I_{line}	11	−	140*	mA
with reduced performance		I_{line}	2	−	11	mA
Internal supply current:						
power-down input LOW	$V_{CC1} = 2.8$ V	I_{CC1}	−	1.3	1.6	mA
power-down input HIGH	$V_{CC1} = 2.8$ V	I_{CC1}	−	60	82	μA
Voltage gain range:						
microphone amplifier		G_v	44	−	52	dB
receiving amplifier		G_v	20	−	45	dB
Line loss compensation:						
gain control range		G_v	5.7	6.1	6.5	dB
exchange supply voltage range		V_{exch}	36	−	60	V
exchange feeding bridge resistance range		R_{exch}	400	−	1000	Ω
Maximum output voltage swing on LN (peak-to-peak value)	R15 + R16 = 448 Ω $I_{line} = 15$ mA					
	$I_p = 2$ mA	$V_{LN(p\text{-}p)}$	3.7	3.95	4.2	V
	$I_p = 4$ mA	$V_{LN(p\text{-}p)}$	3.0	3.25	3.5	V
Regulated line voltage application						
	R15 = 0 Ω; R16 = 392 Ω					
Supply for peripherals	$I_{line} = 15$ mA					
	$I_p = 1.4$ mA	V_P	2.5	−	−	V
	$I_p = 2.7$ mA; $R_{REG\text{-}SLPE} = 20$ kΩ	V_P	2.9	−	−	V
DC line voltage	$I_{line} = 15$ mA					
	without $R_{REG\text{-}SLPE}$	V_{LN}	−	3.57	−	V
	$R_{REG\text{-}SLPE} = 20$ kΩ	V_{LN}	−	4.57	−	V
Stabilized supply voltage application						
	R15 = 392 Ω; R16 = 56 Ω					
Supply for peripherals	$I_{line} = 15$ mA					
	$I_p = 0$ to 4 mA	$V_{CC2\text{-}SLPE}$	3.05	3.3	3.55	V
DC line voltage	$I_{line} = 15$ mA					
	$I_p = 2$ mA	V_{LN}	4.2	4.4	4.8	V
	$I_p = 4$ mA	V_{LN}	4.9	5.1	5.5	V

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* For TEA1064AT the maximum line current depends on the heat dissipating qualities of the mounted device.

PINNING

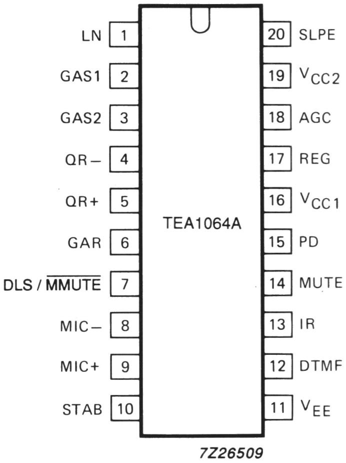

Fig. 2 Pinning diagram.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	DLS/$\overline{\text{MMUTE}}$	decoupling for transmit amplifier dynamic and microphone MUTE input
8	MIC−	inverting microphone input
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	DTMF	dual-tone multi-frequency input
13	IR	receiving amplifier input
14	MUTE	mute input
15	PD	power-down input
16	V_{CC1}	internal supply decoupling
17	REG	voltage regulator decoupling
18	AGC	automatic gain control input
19	V_{CC2}	reference voltage with respect to SLPE
20	SLPE	slope adjustment for DC curve/reference for peripheral circuits.

FUNCTIONAL DESCRIPTION

Supplies V_{CC1}, V_{CC2}, LN, SLPE, REG and STAB (Fig. 3)

Power for the TEA1064A and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC1} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC1} and V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig. 3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between V_{CC2} and SLPE [$V_{ref} = V_{CC2\text{-}SLPE} = 3.3$ V (typ.)]. This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE} (C3).

The reference voltage can be used to:

- regulate directly the line voltage (stabilized $V_{LN\text{-}SLPE} = V_{CC2\text{-}SLPE}$)*
- to stabilize the supply voltage for peripherals.

Regulated line voltage

In this application the V_{CC2} pin is connected to the LN pin as shown in Fig. 3. This configuration gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN\text{-}SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 μF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig. 4. To increase the supply capabilities, the DC voltage $V_{LN\text{-}SLPE}$ can be increased by using $R_{VA(REG\text{-}SLPE)}$ or by decreasing the value of R16.

* The TEA1064A application with regulated line voltage is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.

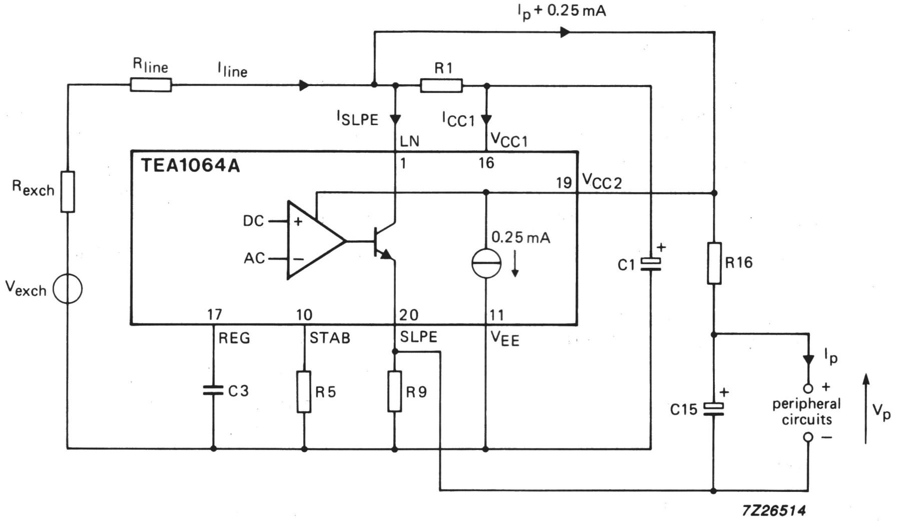
I_p + 0.25 mA
R_{line}
I_{line}
R1
I_{SLPE}
I_{CC1}
LN
V_{CC1}
TEA1064A
1
16
19
V_{CC2}
R_{exch}
DC
AC
0.25 mA
C1
R16
V_{exch}
17
10
20
11
REG
STAB
SLPE
V_{EE}
C3
R5
R9
I_p
peripheral circuits
V_p
C15
7Z26514

Fig. 3 Application with regulated line voltage (stabilized $V_{LN\text{-}SLPE}$). The voltage $V_{LN\text{-}SLPE}$ is fixed to $V_{ref} = 3.3 \pm 0.25$ V. Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary). The line voltage $V_{LN} = V_{ref} + ([I_{line} - 1.55\ \text{mA}] \times R9)$.

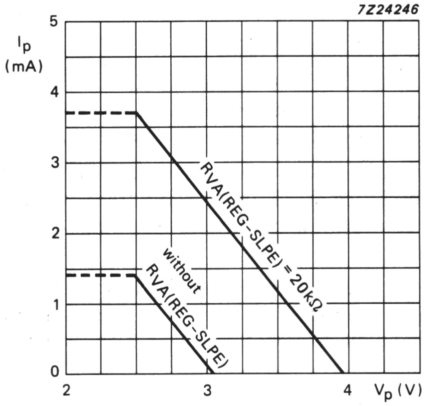

Fig. 4 Minimum supply current for peripherals (I_p) as a function of the peripheral supply voltage (V_p): I_{line} = 15 mA; R16 = 392 Ω; R15 = 0 Ω; valid for MUTE = 0 and 1. Line current has very little influence.

FUNCTIONAL DESCRIPTION (continued)

Regulated line voltage (continued)

The maximum AC output swing on the line at low line currents is influenced by R16 (limited by current) and the maximum output swing on the line at high line currents is influenced by the DC voltage $V_{LN\text{-}SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone input is overdriven. The maximum AC output swing on LN is shown in Fig. 5; practical values for R16 are from 200 to 600 Ω and this influences both the maximum output swing at low line currents and the supply capabilities.

The SLPE pin is the ground reference for peripheral circuits, therefore inputs MUTE, PD and DTMF are also referenced to SLPE.

Active microphones can be supplied between V_{CC1} and V_{EE}. Low-power circuits that provide only MUTE and/or PD inputs to the TEA1064A also can be powered from V_{CC1}. However V_{CC1} cannot be used for circuits that provide DTMF signals to the TEA1064A because V_{CC1} is referred to ground.

If the line current I_{line} exceeds I_{CC1} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC1} \approx 1.3$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9)$

$V_{LN} = V_{ref} + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3} A] \times R9)$

in which

$V_{ref} = 3.3\ V \pm 0.25\ V$ is the internal reference voltage between V_{CC2} and SLPE; its value can be adjusted by external resistor R_{VA}

R9 = external resistor between SLPE and V_{EE} (20 Ω in basic application).

With R9 = 20 Ω, this results in:

$V_{LN} = 3.57 \pm 0.25$ V at $I_{line} = 15$ mA

$V_{LN} = 4.17 \pm 0.3$ V at $I_{line} = 15$ mA, $R_{VA(REG\text{-}SLPE)} = 33\ k\Omega$

$V_{LN} = 4.57 \pm 0.35$ V at $I_{line} = 15$ mA, $R_{VA(REG\text{-}SLPE)} = 20\ k\Omega$

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone, and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC1} + 0.25\ mA)$ and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in the audio frequency range is shown in Fig. 6.

The internal reference voltage $V_{CC2\text{-}SLPE}$ can be increased by external resistor $R_{VA(REG\text{-}SLPE)}$ connected between REG and SLPE. The supply voltage $V_{CC2\text{-}SLPE}$ is shown as a function of $R_{VA(REG\text{-}SLPE)}$ in Fig. 7. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.

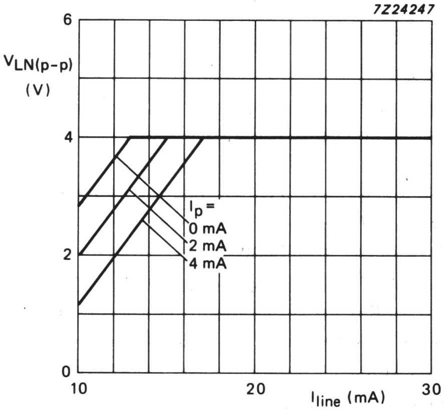

Fig. 5 Maximum AC output swing on the line as a function of line current with peripheral supply current as a parameter: R15 = 0 Ω; R16 = 392 Ω.

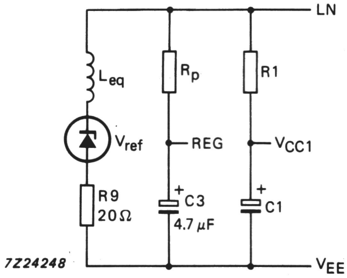

Fig. 6 Equivalent impedance between LN and V_{EE} in the application with stabilized $V_{LN\text{-}SLPE}$:

R15 = 0 Ω

L_{eq} = C3 x R9 x R_p

R_p = 15 kΩ

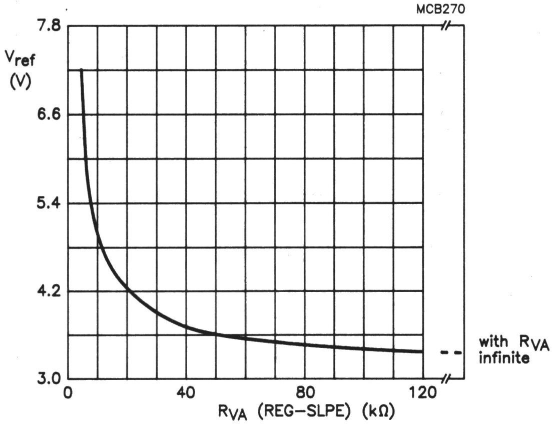

Fig. 7 Internal reference voltage $V_{CC2\text{-}SLPE}$ as a function of resistor $R_{VA(REG\text{-}SLPE)}$ for line currents between 11 and 140 mA.

In the stabilized supply application:

$$V_{LN} = V_{CC2\text{-}SLPE} + ([I_p + 0.25 \times 10^{-3}\,A] \times R15) + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

In the unregulated supply application (R15 = 0 Ω):

$$V_{LN} = V_{CC2\text{-}SLPE} + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage

The configuration shown in Fig. 8 provides a stabilized voltage across pins V_{CC2} and SPLE for peripheral circuits (such as dialling and control circuits); the DC voltage V_{LN} now varies with the peripheral supply current.

The $V_{CC2\text{-}SLPE}$ supply must be decoupled by capacitor C15. For stable loop operation, resistor R16 ($\approx 50\ \Omega$) is connected between V_{CC2} and SLPE in series with C15. The voltage regulator control loop is completed by resistor R15 between LN and V_{CC2}.

For sets with an impedance of 600 Ω, practical values are: R15 = 200 to 600 Ω; C15 = 220 µF; C3 = 470 nF. The ratio $R15/R16 \leqslant 8$ is for stable loop operation with sufficient phase margin, and $R15/R16 \geqslant 6$ is for satisfactory set impedance in the audio frequency range.

For sets with complex impedance, the value of C3 and the ratio R15/R16 are different (further information is given in the TEA1064A Application Report*).

The peripheral supply capability depends mainly on the available line current, the required AC output swing on the line, the maximum permitted DC voltage on the line and the values of external components (especially R15). With R15 = 392 Ω and R16 = 56 Ω (basic application) the maximum possible AC output swing on the line as a function of line current is as shown in Fig. 9, the curve parameter is the peripheral supply current (I_p). Different values for R15 (from 200 to 600 Ω) maintaining $6 < R15/R16 < 8$ give different results (these are described in the TEA1064A Application Report*).

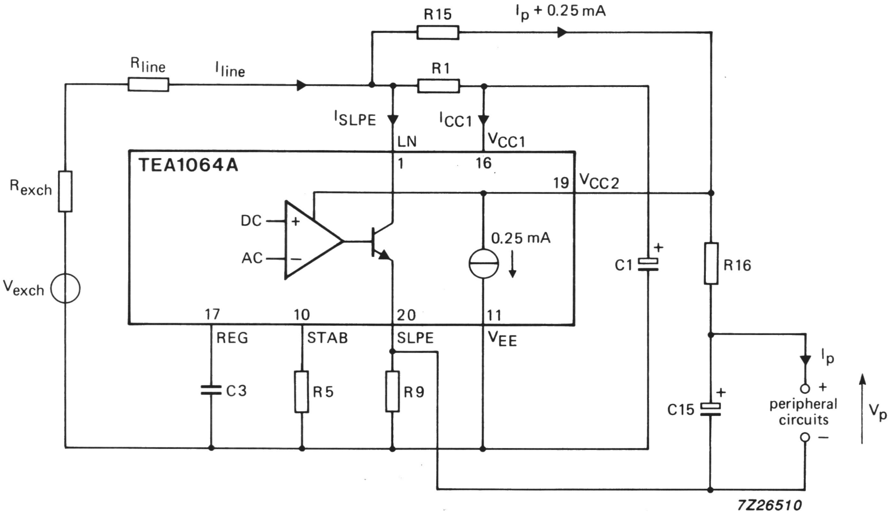

Fig. 8 Application with stabilized supply voltage for peripheral circuits: R15 = 392 Ω; R16 = 56 Ω.

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* Supplied on request.

The DC line voltage on LN is

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9).$$

Therefore

$$V_{LN} = V_{ref} + ([I_p + 0.25 \times 10^{-3} A] \times R15) + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3} A] \times R9)$$

in which:

V_{ref} is the internal reference voltage between V_{CC2} and SLPE (the value of V_{ref} can be adjusted by an external resistor, R_{VA}). V_{ref} = 3.3 V (typ.) without R_{VA}

I_p is the supply current used by peripheral circuits

R15 is an external resistor between LN and V_{CC2} (392 Ω in the basic application)

R9 is an external resistor between SLPE and V_{EE} (20 Ω in the basic application)

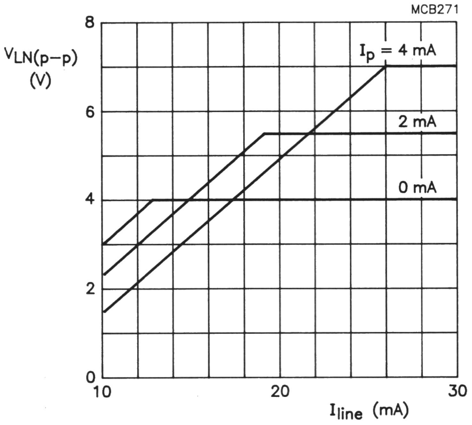


Fig. 9 Maximum output swing on line as a function of line current with the peripheral supply current as a parameter; R15 = 392 Ω; R16 = 56 Ω. As different values of R15 and R16 are allowed, different curves would then apply.

The DC voltage $V_{LN\text{-}SLPE}$ as a function of I_p with R15 as a parameter is shown in Fig. 10. In the audio frequency range, the dynamic impedance is determined mainly by R1. The equivalent impedance in the audio range of the circuit (Fig. 8) is shown in Fig. 11.

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage (continued)

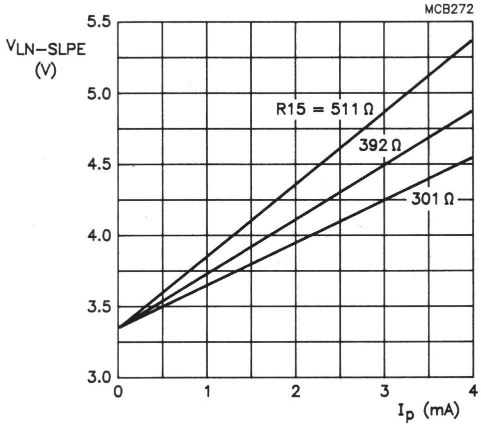
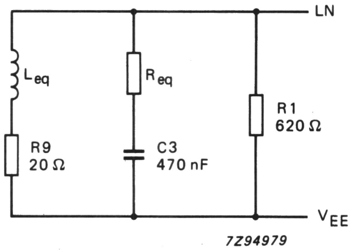


Fig. 10 Curves showing the typical voltage drop between LN and SLPE as a function of the supply current for peripherals with R15 as a parameter: $V_{CC2\text{-}SLPE} = 3.3$ V (R_{VA} not connected). $V_{CC2\text{-}SLPE}$ can be adjusted between approximately 3.3 and 4.3 V by changing the value of R_{VA}, this results in a parallel-shift of the curves.
The total voltage drop $V_{LN} \approx V_{LN\text{-}SLPE} + ([I_{line} - 1.55 \text{ mA}] \times R9)$.



$$R_{eq} = R_p \left(\frac{R15}{R16} + 1\right)$$

$$L_{eq} = C3 \times R9 \times R_{eq}$$

with $R_p = 15\ k\Omega$

Fig. 11 Equivalent impedance between LN and V_{EE} at f > 300 Hz in the application with stabilized supply voltage for peripheral circuits.

Microphone inputs MIC+ and MIC– and gain pins GAS1 and GAS2

The TEA1064A has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typ. 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig. 12.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.

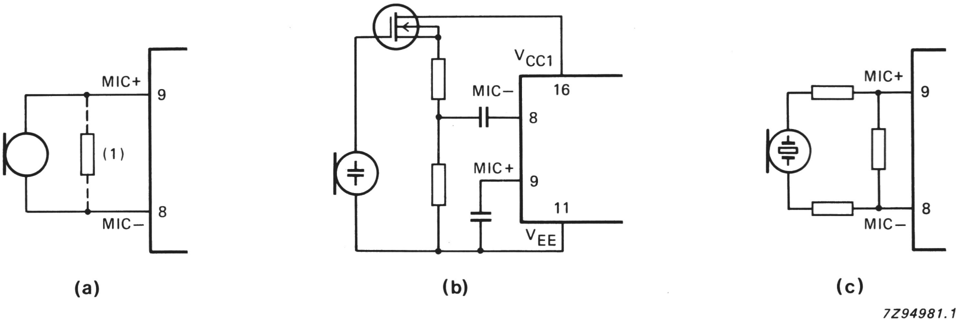


Fig. 12 Microphone arrangements: a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs; b) electret microphone; c) piezo-electric microphone.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC− but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.13.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit (voltage $V_{LN-SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased.
Fig. 14 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN-SLPE}$) with $I_{line} - I_p$ as a parameter.

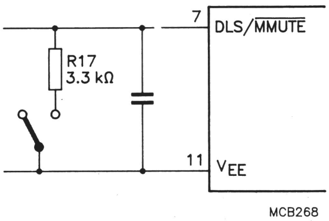


Fig. 13 Microphone-mute function.

FUNCTIONAL DESCRIPTION (continued)

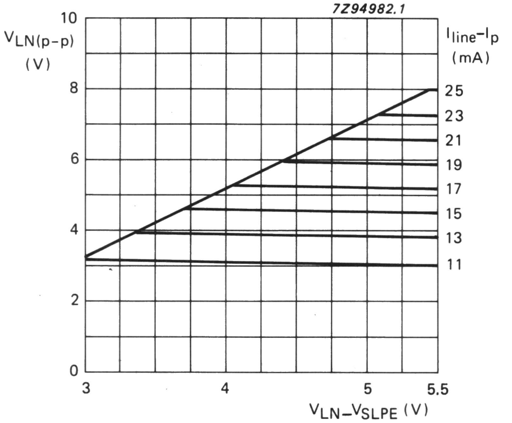


Fig. 14 Maximum output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_p$ as a parameter: R15 = 392 Ω; R16 = 56 Ω; or R15 = 0 Ω and R16 = 392 + 56 = 448 Ω.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

Receiving amplifier IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR– (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig. 15). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.

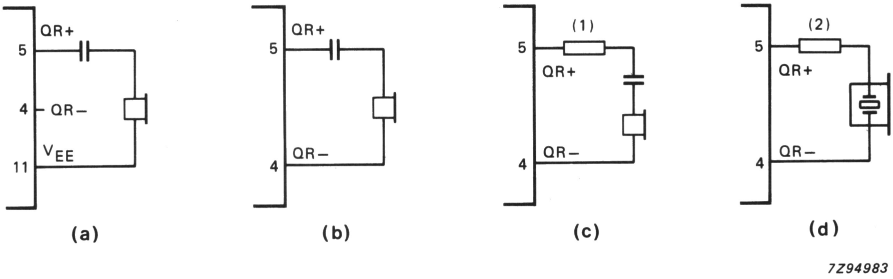


Fig. 15 Alternative receiver arrangements: a) dynamic earpiece with an impedance less than 450 Ω; b) dynamic earpiece with an impedance more than 450 Ω; c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); d) piezo-electric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig. 16 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

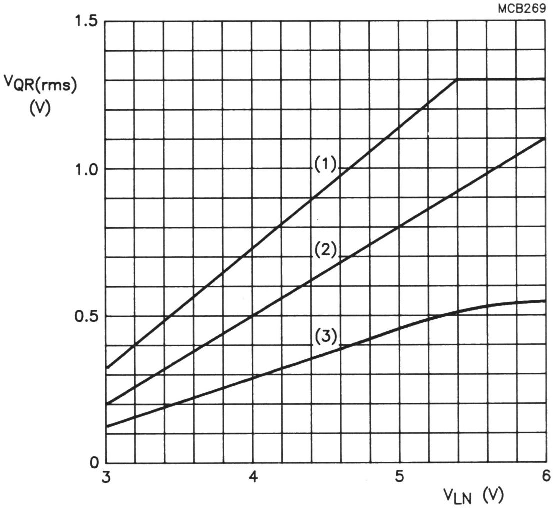


Fig. 16 Maximum output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter: valid for both supply options; THD = 2%; I_{line} = 15 mA. Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω); f = 3400 Hz. Curve (2) is for a differential load of 450 Ω; f = 1 kHz. Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig. 17 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open, the amplifiers then give their maximum gain.

FUNCTIONAL DESCRIPTION (continued)

Automatic gain control input AGC (continued)

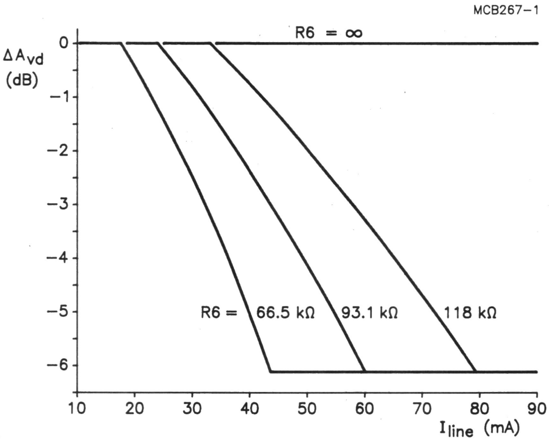


Fig. 17 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	84.5	66.5	X	X
	48	118	93.1	77.8	66.5
	60	X	X	97.6	84.5

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on to the line. The voltage gain between DTMF-SLPE and LN-V_{EE} is typ. 26 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 26 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC1} or for the peripherals between V_{CC2} and SLPE.
These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by applying a HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from (typ.) 1.3 mA to (typ.) 60 μA and switches off the voltage regulator to prevent discharge via LN and V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to SLPE.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line}, R2, R3, R8, R9 and Z_{bal} (see Fig. 18). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + [R8//Z_{bal}])$

b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) is always fulfilled provided $|R8//Z_{bal}| << R3$.

To obtain optimum sidetone suppression, condition b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal};
- $|Z_{bal}//R8| << R3$ to fulfill condition a) and thus ensure correct anti-sidetone bridge operation;
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain.

In practice Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω // 140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in: R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω // 220 nF).

Side-tone suppression (continued)

The anti-sidetone network for the TEA1060 family shown in Fig. 18 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (Fig. 19). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.)

Notes

1. The reference used for the MUTE, DTMF and PD inputs is SLPE.
2. A LOW level for any of these pins is defined by connection to SLPE, a HIGH level is defined as a voltage greater than V_{SLPE} + 1.5 V and smaller than V_{CC1} + 0.4 V.

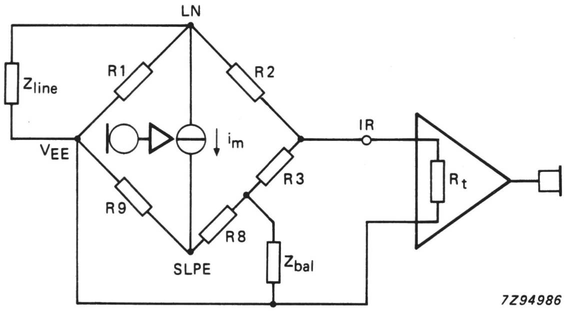


Fig. 18 Equivalent circuit of TEA1060 family anti-side-tone bridge.

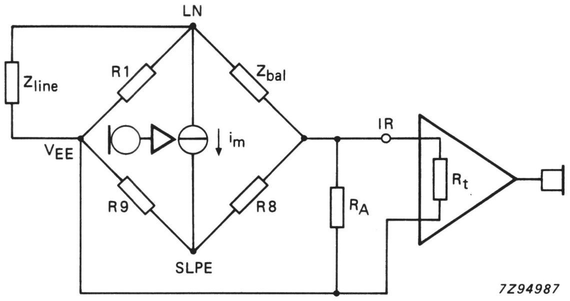


Fig. 19 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 24)	V_{LN}	–	28	V
Line current TEA1064A (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Line current TEA1064AT (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Input voltage on pins other than LN and V_{CC2}		V_i	$V_{EE}-0.7$	$V_{CC1}+0.7$	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1064A		P_{tot}	–	714	mW
TEA1064AT		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	–40	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 20 and 21 to determine the current as a function of the required voltage and the temperature.

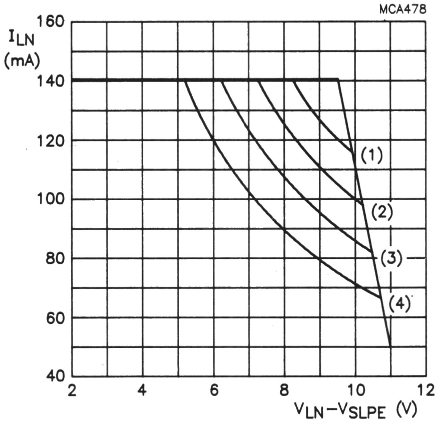
(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

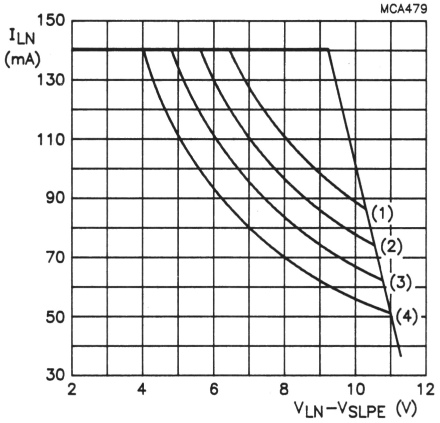
TEA1064A $R_{th\ j\text{-}a}$ = 70 K/W

TEA1064AT mounted on glass epoxy board 41 x 19 x 1.5 mm $R_{th\ j\text{-}a}$ = 90 K/W



	T_{amb}	P_{tot}
(1)	45 °C	1143 mW
(2)	55 °C	1000 mW
(3)	65 °C	857 mW
(4)	75 °C	714 mW

Fig. 20 TEA1064A safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig. 21 TEA1064AT safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuit of Fig. 22 or 23); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies LN, V_{CC1}, V_{CC2} (pins 1, 16, 19)						
Reference DC voltage between V_{CC2} and SLPE	I_{line} = 15 mA I_p = 0; 4 mA					
R_{VA} not connected		$V_{CC2-SLPE}$	3.05	3.3	3.55	V
Variation with temperature	I_{line} = 15 mA	$\frac{V_{CC2-SLPE}}{\Delta T}$	−3.0	−1.0	1.0	mV/K
Variation with line current referred to 15 mA	I_{line} = 100 mA	$\Delta V_{CC2-SLPE}$	–	60	–	mV
With R_{VA} connected between REG and SLPE	R_{VA} = 33 kΩ	$V_{CC2-SLPE}$	3.6	3.8	4.2	V
	R_{VA} = 20 kΩ	$V_{CC2-SLPE}$	3.95	4.2	4.65	V
DC line voltage: voltage drop between LN and V_{EE}	MIC−, MIC+ inputs open; R15 = 392 Ω; without R_{VA}					
at I_{line} = 15 mA	I_p = 0 mA	V_{LN}	3.4	3.6	4.0	V
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V
at I_{line} = 100 mA	I_p = 2 mA	V_{LN}	–	6.1	7.0	V
at I_{line} = 140 mA	I_p = 2 mA	V_{LN}	–	7.0	7.8	V
Voltage drop under low current conditions	I_p = 0 mA					
	I_{line} = 2 mA	V_{LN}	–	1.8	–	V
	I_{line} = 4 mA	V_{LN}	–	2.2	–	V
	I_{line} = 7 mA	V_{LN}	–	3.2	–	V
	I_{line} = 11 mA	V_{LN}	–	3.5	–	V
Internal supply current I_{CC1}: current into pin V_{CC1}	V_{CC1} = 2.8 V					
	PD = LOW	I_{CC1}	–	1.3	1.6	mA
	PD = HIGH	I_{CC1}	–	60	82	μA
Microphone inputs MIC−, MIC+ (pins 8, 9)						
Input impedance:						
differential		Z_i	51	64	77	kΩ
single-ended		Z_i	25.5	32.0	38.5	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Common mode rejection ratio		CMRR	–	82	–	dB
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_V	51	52	53	dB
Variation of G_V with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_V f$	–0.5	± 0.1	+ 0.5	dB
Variation of G_V with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to + 75 °C	$\Delta G_V T$	–	± 0.2	–	dB
DTMF input (pin 12)						
Input impedance		Z_i	16.8	20.7	24.6	kΩ
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_V	25	26	27	dB
Variation of G_V with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_V f$	–0.5	± 0.1	+ 0.5	dB
	f = 697 and 1633 Hz	$\Delta G_V f$	–0.2	± 0.05	+ 0.2	dB
Variation of G_V with temperature, referred to 25 °C	I_{line} = 50 mA; T_{amb} = –25 to + 75 °C	$\Delta G_V T$	–	± 0.2	0.5	dB
Gain adjustment inputs GAS1, GAS2 (pins 2, 3)						
Transmitting amplifier, gain adjustment range		ΔG_V	–8	–	+ 0	dB
Sending amplifier output LN (pin 1)						
Dynamic limiter						
Output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; I_p = 0 mA; $V_{i(rms)}$ = 3.6 mV	$V_{LN(p-p)}$	3.6	4.0	4.5	V
Total harmonic distortion	V_i = 3.6 mV + 10 dB	THD	–	1.5	2.0	%
	V_i = 3.6 mV + 15 dB	THD	–	2.8	10.0	%
Output voltage swing (peak-to-peak value)	V_i = 3.6 mV + 10 dB					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
	I_p = 0 mA; I_{line} = 7 mA	$V_{LN(p-p)}$	–	2	–	V
	I_p = 0 mA; I_{line} = 4 mA	$V_{LN(p-p)}$	–	1	–	V

parameter	conditions	symbol	min.	typ.	max.	unit
LN output (continued)						
Dynamic behaviour of limiter	C16 = 470 nF					
attack time, V_{mic} jumps from 2 mV to 40 mV		t_{att}	–	1.5	5.0	ms
release time, V_{mic} jumps from 40 mV to 2 mV		t_{rel}	50	150	–	ms
Noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		Z_i	17	21	25	kΩ
Receiving amplifier outputs QR– QR+ (pins 4, 5)						
Output impedance	single-ended	Z_o	–	4	–	Ω
Voltage gain	Fig. 23; I_{line} = 15 mA; R4 = 100 kΩ					
single-ended; R_T = 300 Ω		G_v	30	31	32	dB
differential; R_T = 600 Ω		G_v	36	37	38	dB
Variation with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	ΔG_vf	–0.5	–0.2	0	dB
Variation with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	ΔG_vT	–	± 0.2	–	dB
Output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA					
single-ended; R_T = 150 Ω	I_p = 0 mA	$V_{o(rms)}$	–	0.22	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.35	–	V
differential; R_T = 450 Ω	I_p = 0 mA	$V_{o(rms)}$	–	0.39	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.64	–	V
differential; C_T = 47 nF; (100 Ω series resistor); f = 3400 Hz	I_p = 0 mA	$V_{o(rms)}$	–	0.57	–	V
	I_p = 2 mA	$V_{o(rms)}$	–	0.9	–	V

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (RMS value)	I_p = 0 mA; THD = 10%; sinewave drive; R4 = 100 kΩ; single-ended; R_T = 150 Ω;					
	I_{line} = 4 mA	$V_{o(rms)}$	–	25	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	160	–	mV
Noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open					
	single-ended; R_T = 300 Ω	$V_{no(rms)}$	–	45	–	μV
	differential; R_T = 600 Ω	$V_{no(rms)}$	–	90	–	μV
Noise output voltage (RMS value)	in circuit of Fig. 23; S1 in position 2; 200 Ω between MIC+ and MIC−; single-ended; R_T = 300 Ω					
	R7 = 68 kΩ	$V_{no(rms)}$	–	100	–	μV
	R7 = 24.9 kΩ	$V_{no(rms)}$	–	65	–	μV
Gain adjustment input GAR (pin 6)						
Receiving amplifier, gain adjustment range		ΔG_v	–11	–	+8	dB
MUTE INPUT (pin 14)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{mute}	–	11	20	μA
Change of microphone amplifier gain at mute-ON	MUTE = HIGH	$-\Delta G_v$	–	100	–	dB
Voltage gain from input DTMF-SLPE to QR+ output with mute-ON	MUTE = HIGH; single-ended load; R_L = 300 Ω	G_v	–	–18	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Power-down input PD (pin 15)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 18)						
Controlling the gain from IR (pin 13) to QR+, QR– (pins 4, 5) and the gain from MIC+, MIC– (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)					
gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	$-G_v$	5.7	6.1	6.5	dB
Highest line current for maximum gain		I_{line}	–	24	–	mA
Lowest line current for minimum gain		I_{line}	–	61	–	mA
Change of gain between I_{line} = 15 and 35 mA		$-\Delta G_v$	0.9	1.4	1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
Input voltage low		V_{IL}	V_{EE}	–	V_{EE} + 0.3	V
Input current at low input voltage		I_{IL}	–85	–60	–35	μA
Release time after a low level on pin 7	C16 = 470 nF	t_{rel}	–	30	–	ms
Change of microphone amplifier gain at low input voltage on pin 7		$-\Delta G_v$	–	100	–	dB

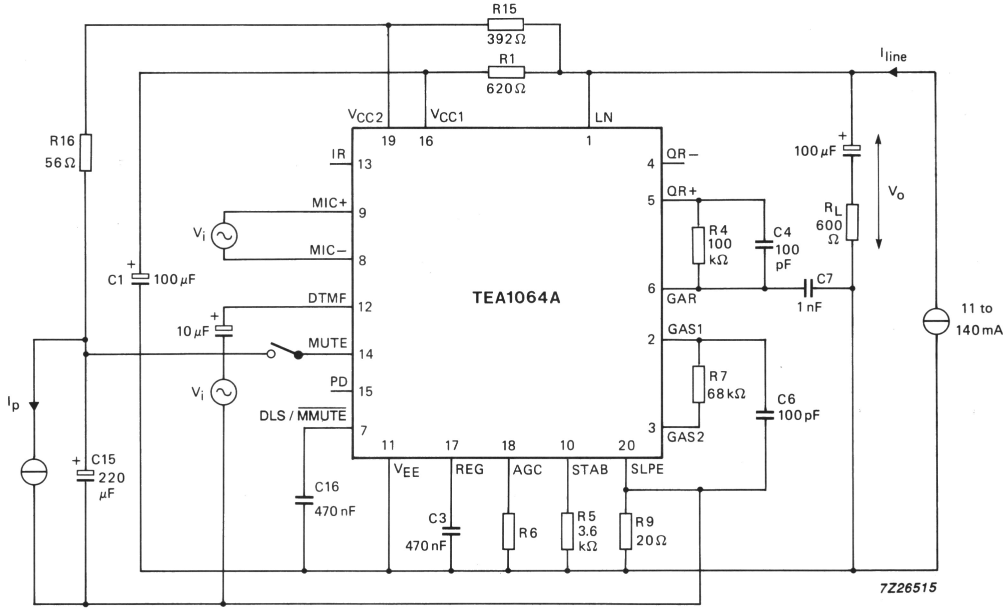

R15
392Ω
R1
620Ω
I_line
V_CC2
V_CC1
LN
19
16
1
R16
56Ω
IR
13
4
QR−
100 µF
MIC+
9
5
QR+
V_o
V_i
R4
100
kΩ
C4
100
pF
R_L
600
Ω
MIC−
8
C1
100 µF
6
C7
DTMF
12
TEA1064A
GAR
1 nF
11 to
140 mA
10 µF
MUTE
14
2
GAS1
V_i
PD
15
R7
68 kΩ
C6
100 pF
I_p
DLS / MMUTE
7
3
GAS2
11
17
18
10
20
C15
220
µF
V_EE
REG
AGC
STAB
SLPE
C16
470 nF
C3
470 nF
R6
R5
3.6
kΩ
R9
20Ω
7Z26515

Fig. 22 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_V) is defined as 20 log$|V_O/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit; for measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open-circuit.

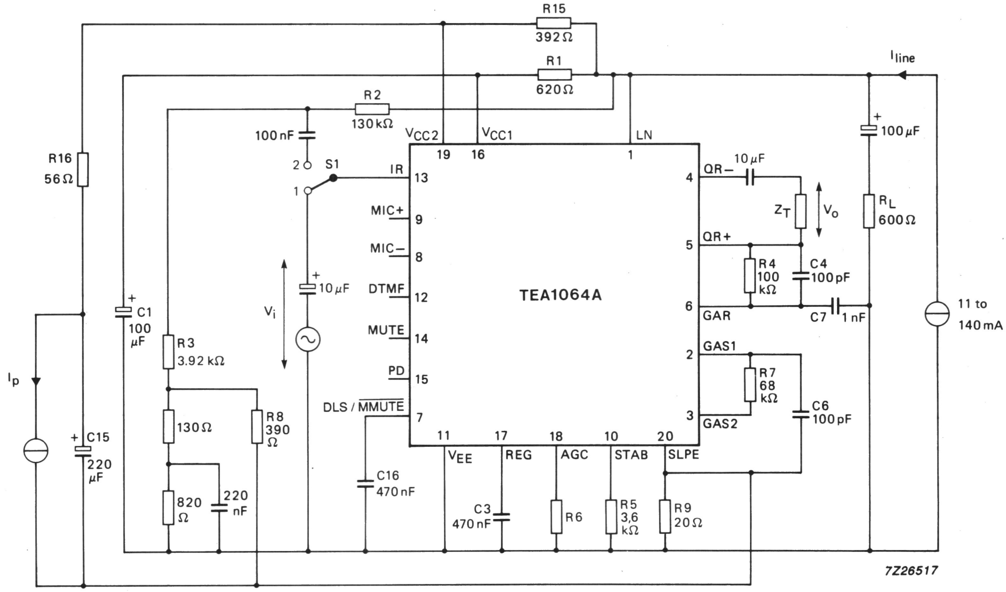

R15
392Ω
R1
620Ω
I_line
R2
130 kΩ
100 nF
V_CC2
V_CC1
LN
19
16
1
R16
56Ω
2
S1
1
IR
13
4
QR−
10 µF
100 µF
Z_T
V_o
R_L
600Ω
MIC+
9
MIC−
8
5
QR+
R4
100
kΩ
C4
100 pF
10 µF
DTMF
12
V_i
TEA1064A
6
GAR
C7
1 nF
11 to
140 mA
C1
100
µF
MUTE
14
R3
3.92 kΩ
2
GAS1
I_p
PD
15
R7
68
kΩ
R8
390
Ω
DLS / MMUTE
7
3
GAS2
C6
100 pF
130Ω
C15
220
µF
11
17
18
10
20
V_EE
REG
AGC
STAB
SLPE
C16
470 nF
820
Ω
220
nF
C3
470 nF
R6
R5
3.6
kΩ
R9
20Ω
7Z26517

Fig. 23 Test circuit for defining voltage gain of the receiving amplifier, voltage gain (G_V) is defined as 20 log$|V_O/V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig. 24 and some typical applications are shown in Figs 25, 26 and 27.

In the basic application, the circuit provides two possibilities for supplies to peripheral circuits:

- regulated line voltage V_{LN} (stabilized $V_{LN\text{-}SLPE}$) and unregulated supply voltage for peripheral circuits, the supply voltage is dependent only on the peripheral supply current. This application is the same as that used for TEA1060/TEA1061, TEA1067 and TEA1068;
- stabilized supply voltage for peripherals ($V_{CC2\text{-}SLPE}$), the DC line voltage depends on the current flowing to the peripheral circuits.

APPLICATION INFORMATION (continued)

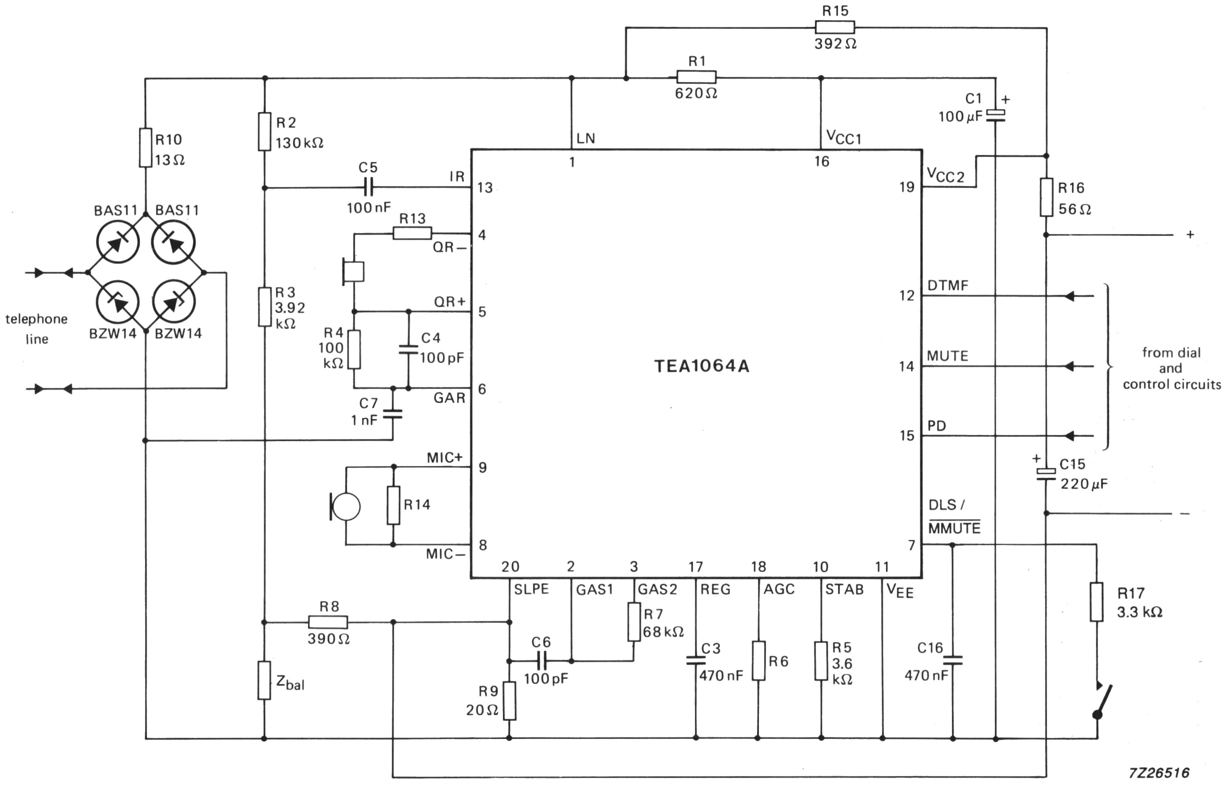

R15
392 Ω
R1
620 Ω
C1
100 μF
+
R10
13 Ω
R2
130 kΩ
C5
100 nF
IR
13
LN
1
VCC1
16
VCC2
19
R16
56 Ω
+
BAS11
BAS11
BZW14
BZW14
telephone line
R13
QR−
4
QR+
5
R3
3.92 kΩ
R4
100 kΩ
C4
100 pF
GAR
6
C7
1 nF
DTMF
12
MUTE
14
PD
15
from dial and control circuits
TEA1064A
C15
220 μF
+
MIC+
9
R14
MIC−
8
DLS / MMUTE
7
−
20
2
3
17
18
10
11
SLPE
GAS1
GAS2
REG
AGC
STAB
VEE
R8
390 Ω
R7
68 kΩ
C6
100 pF
C3
470 nF
R6
R5
3.6 kΩ
C16
470 nF
R17
3.3 kΩ
Zbal
R9
20 Ω
7Z26516

Fig. 24 Basic application of the TEA1064A with stabilized supply for peripherals, shown here with a piezo-electric earpiece and DTMF dialling. The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

For the basic application giving regulated line voltage the above circuit is changed as follows:

- R15 must be short-circuited;
- the value of R16 is changed to 392 Ω;
- the value of C3 is changed to 4.7 μF.

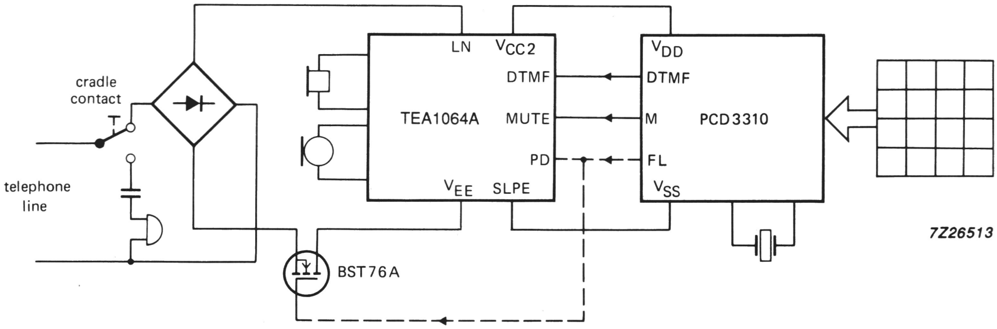

cradle contact
T
telephone line
LN
VCC2
DTMF
TEA1064A
MUTE
PD
VEE
SLPE
BST76A
VDD
DTMF
M
PCD3310
FL
VSS
7Z26513

Fig. 25 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064A with the CMOS bilingual dialling circuit PCD3310; the broken line indicates optional flash (register recall by timed loop break).

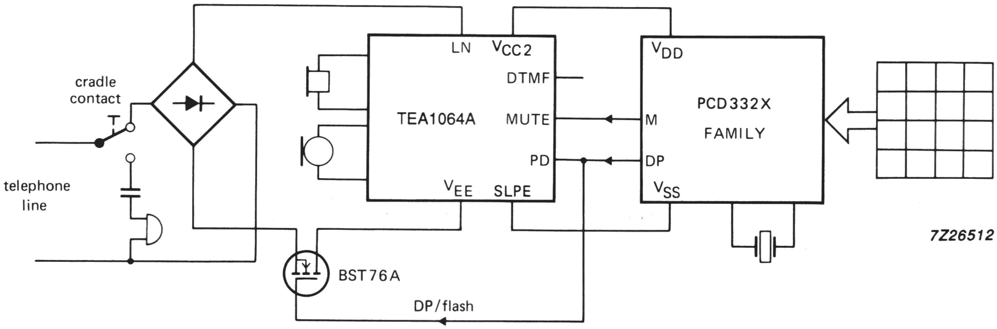

cradle contact
T
telephone line
LN
VCC2
DTMF
TEA1064A
MUTE
PD
VEE
SLPE
BST76A
DP/flash
VDD
PCD332X FAMILY
M
DP
VSS
7Z26512

Fig. 26 Typical pulse dial set application circuit (simplified) showing the TEA1064A with one of the PCD332X family of CMOS interrupted current-loop dialling circuits.

APPLICATION INFORMATION (continued)

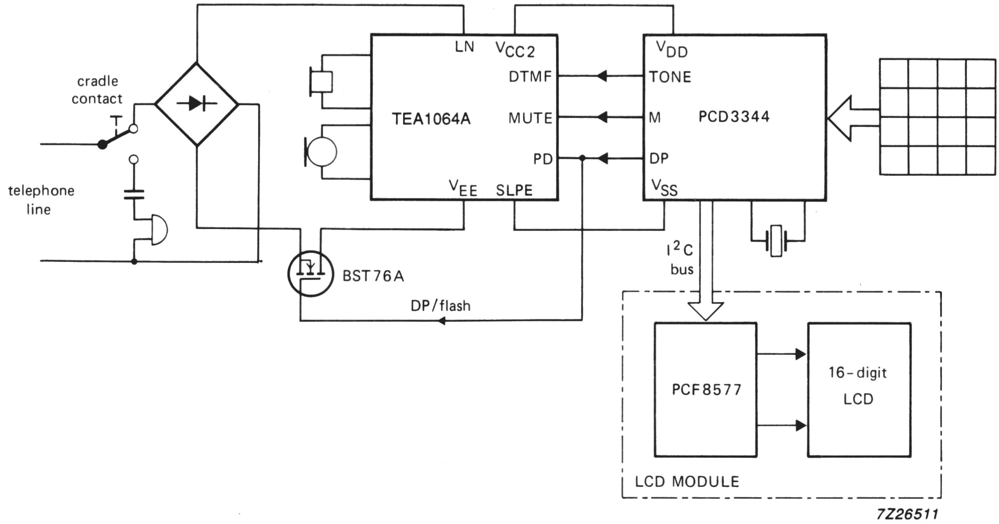

cradle
contact
telephone
line
LN
V_{CC2}
DTMF
TEA1064A
MUTE
PD
V_{EE}
SLPE
V_{DD}
TONE
M
PCD3344
DP
V_{SS}
BST76A
DP/flash
I^2C
bus
PCF8577
16-digit
LCD
LCD MODULE
7Z26511

Fig. 27 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064A and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I^2C-bus.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

FEATURES

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch
- MUTE, POWER-DOWN and DTMF input reference (pin V_{EE2}) can be connected either to V_{EE1} or SLPE.

GENERAL DESCRIPTION

The TEA1064B is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1064B	20	DIL	plastic	SOT146
TEA1064BT	20	mini-pack	plastic	SO20; SOT163A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range					
	normal operation	note 1	11	–	140	mA
	with reduced performance		2	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V				
	power-down input LOW		–	1.3	1.6	mA
	power-down input HIGH		–	60	82	µA
G_v	voltage gain range					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	45	dB
	line loss compensation ranges					
G_v	gain control		5.7	6.1	6.5	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		400	–	1000	Ω
$V_{LN(p-p)}$	maximum output voltage swing on LN (peak-to-peak value)	R16 = 392 Ω; I_{line} = 15 mA				
		I_p = 1.4 mA	3.55	3.80	4.05	V
		I_p = 2.7 mA	3.25	3.50	3.75	V
V_p	supply for peripherals	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	–	V
		I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	2.9	3.1	–	V
V_{LN}	DC line voltage	I_{line} = 15 mA				
		without $R_{REG-SLPE}$	3.25	3.5	3.75	V
		$R_{REG-SLPE}$ = 20 kΩ	4.05	4.4	4.75	V
T_{amb}	operating ambient temperature range		–25	–	+75	°C

Note

1. For the TEA1064BT the maximum line current depends on the heat dissipating qualities of the mounted device.

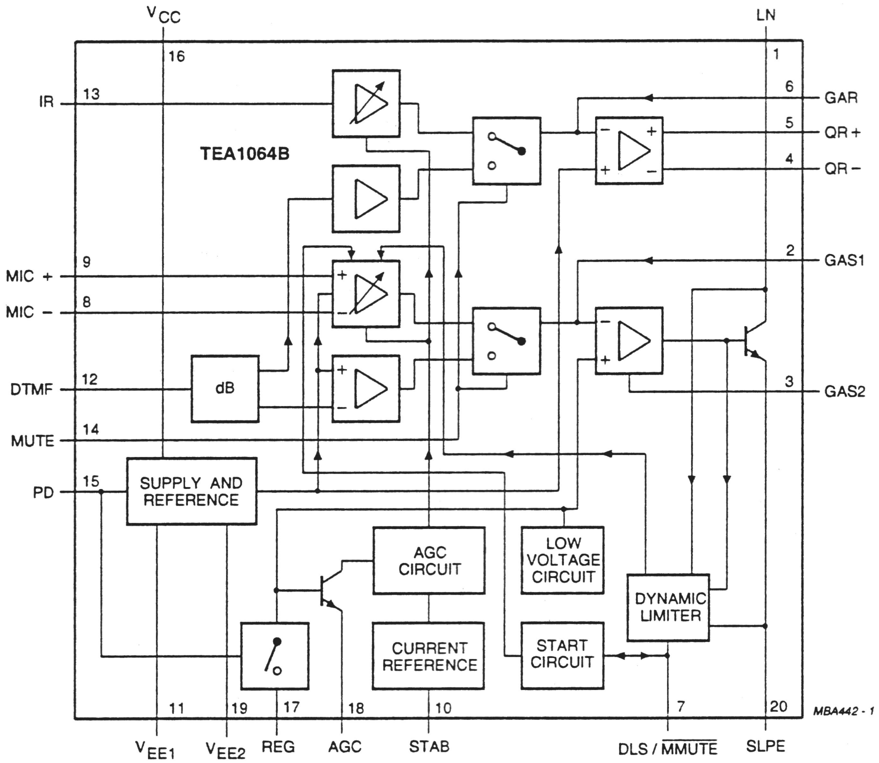

VCC
16
LN
1
IR
13
TEA1064B
6
GAR
5
QR +
4
QR −
MIC +
9
MIC −
8
2
GAS1
DTMF
12
dB
3
GAS2
MUTE
14
PD
15
SUPPLY AND REFERENCE
AGC CIRCUIT
LOW VOLTAGE CIRCUIT
DYNAMIC LIMITER
CURRENT REFERENCE
START CIRCUIT
11
19
17
18
10
7
20
MBA442 - 1
VEE1
VEE2
REG
AGC
STAB
DLS / MMUTE
SLPE

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR−	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
DLS/$\overline{\text{MMUTE}}$	7	decoupling for transmit amplifier dynamic and microphone MUTE input
MIC−	8	inverting microphone input
MIC+	9	non-inverting microphone input
STAB	10	current stabilizer
V_{EE1}	11	negative line terminal
DTMF	12	dual-tone multi-frequency input
IR	13	receiving amplifier input
MUTE	14	mute input
PD	15	power-down input
V_{CC}	16	internal supply decoupling
REG	17	voltage regulator decoupling
AGC	18	automatic gain control input
V_{EE2}	19	reference for POWER-DOWN (PD), MUTE and DTMF
SLPE	20	slope adjustment for DC curve/reference for peripheral circuits

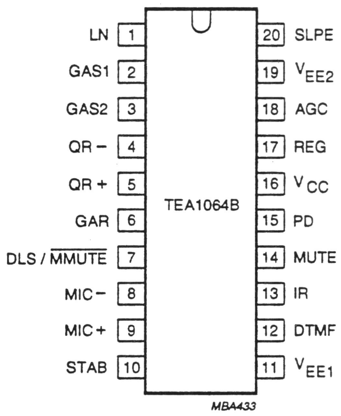

LN 1
GAS1 2
GAS2 3
QR − 4
QR + 5
GAR 6
DLS / MMUTE 7
MIC − 8
MIC + 9
STAB 10
20 SLPE
19 VEE2
18 AGC
17 REG
16 VCC
15 PD
14 MUTE
13 IR
12 DTMF
11 VEE1
TEA1064B
MBA433

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, V_{EE2}, LN, SLPE, REG and STAB (Figs 3 and 5)

Power for the TEA1064B and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC} and V_{EE1}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE1}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig.3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between LN and SLPE ($V_{ref} = V_{LN\text{-}SLPE} = 3.23$ V typ.). This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE1} (C3).

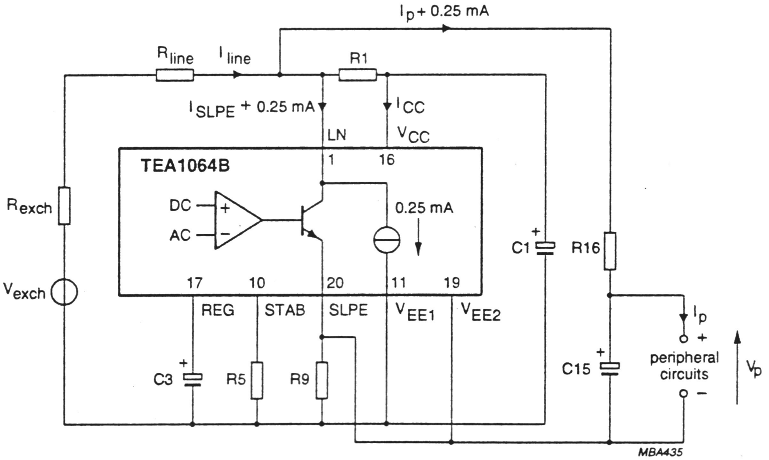
The configuration shown in Fig.3, gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is indendent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN\text{-}SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 µF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig.4.

To increase the supply capabilities, the value of R16 can be decreased or the DC voltage $V_{LN\text{-}SLPE}$ can be increased by using $R_{VA(REG\text{-}SLPE)}$.

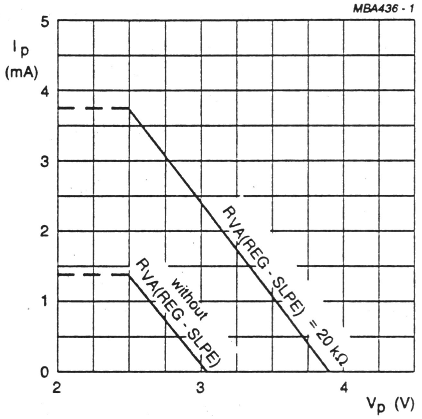
Note

The TEA1064B application is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.



The voltage $V_{LN\text{-}SLPE}$ is fixed to $V_{ref} = 3.323 \pm 0.25$ V.
Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary).
The line voltage $V_{LN} = V_{ref} + (\{I_{line} - 1.55 \text{ mA}\} \times R9)$.

Fig.3 Supply arrangement with reference to SLPE.



I_{line} = 15 mA; R16 = 392 Ω; valid for MUTE = 0 and 1.
Line current has very little influence.

Fig.4 Maximum supply current with respect to Fig.3 for peripherals (I_p) as a function of the peripheral supply voltage (V_p).

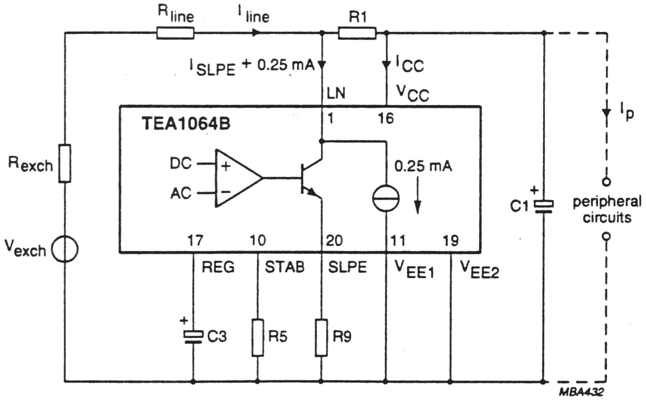
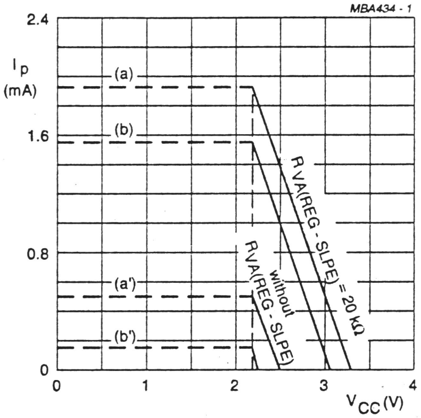

R_{line}
I_{line}
R1
I_{SLPE} + 0.25 mA
I_{CC}
LN
V_{CC}
TEA1064B
1
16
DC
AC
+
−
0.25 mA
R_{exch}
V_{exch}
C1
I_p
peripheral circuits
17
10
20
11
19
REG
STAB
SLPE
V_{EE1}
V_{EE2}
C3
R5
R9
MBA432

Fig.5 Supply arrangement with reference to V_{EE1}.



(a) I_p = 1.94 mA
(b) I_p = 1.54 mA
(a') I_p = 0.54 mA
(b') I_p = 0.16 mA
I_{line} = 15 mA
R1 = 620 Ω and R9 = 20 Ω
Curve (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH.
Curve (b) and (b') are valid when the receiving amplifier is driven and when MUTE = LOW.
$V_{o(RMS)}$ = 150 mV, R_T = 150 Ω.

Fig.6 Maximum current I_p with respect to Fig.5 available from V_{CC} for peripheral circuitry with V_{CC} > 2.2 V.

The maximum AC output swing on the line at low currents is influenced by R16 (limited by current) and the maximum output swing on the line at high currents is influenced by DC voltage $V_{LN\text{-}SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone is overdriven. The maximum AC output swing on LN is shown in Fig.7; practical values for R16 are from 200 Ω to 600 Ω and this influences both maximum output swing at low line currents and the supply capabilities.

When the SLPE pin is the reference for peripheral circuits, inputs MUTE, PD and DTMF must be referenced to SLPE. This is achieved by connecting pin V_{EE2} to pin SLPE; V_{EE2} being the reference of MUTE, PD and DTMF input stages.

Active microphones can be supplied between V_{CC} and V_{EE1} as shown in Fig.5. Low power circuits that provide MUTE, PD and DTMF inputs to the TEA1064B can also be powered from V_{CC} (see Fig.6 for the supply capability of V_{CC}). MUTE, PD and DTMF are then referenced to V_{EE1} and the pin V_{EE2} must therefore be connected to V_{EE1}.
If the line current I_{line} exceeds I_{CC} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC} \approx 1.3$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

- $V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9)$
- $V_{LN} = V_{ref} + (\{I_{line} - I_{CC} - 0.25 \times 10^{-3}\ A\} \times R9)$

in which:

- $V_{ref} = 3.23\ V \pm 0.25\ V$ is the internal reference voltage between LN and SLPE; its value can be adjusted by external resistor R_{VA}.
- R9 = external resistor between SLPE and V_{EE1} (20 Ω in basic operation).

With R9 = 20 Ω, this results in:

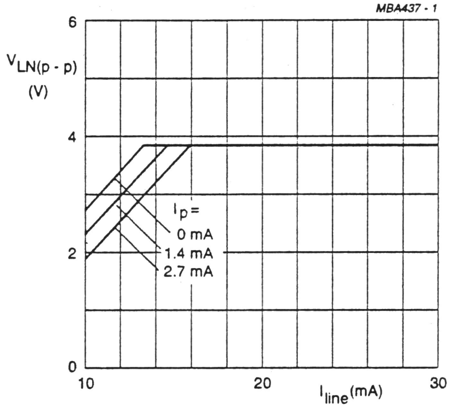
- $V_{LN} = 3.3 \pm 0.25\ V$ at $I_{line} = 15\ mA$
- $V_{LN} = 4.1 \pm 0.3\ V$ at $I_{line} = 15\ mA$, $R_{VA(REG\text{-}SLPE)} = 33\ k\Omega$
- $V_{LN} = 4.4 \pm 0.35\ V$ at $I_{line} = 15\ mA$, $R_{VA(REG\text{-}SLPE)} = 20\ k\Omega$

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} \gg (I_{CC} + 0.25\ mA)$ and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in audio frequency range is shown in Fig.8.

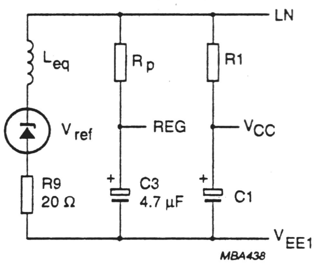
The internal reference voltage $V_{LN\text{-}SLPE}$ can be increased by external resistor $R_{VA(REG\text{-}SLPE)}$ connected between REG and SLPE. The voltage $V_{LN\text{-}SLPE}$ is shown as a function of $R_{VA(REG\text{-}SLPE)}$ in Fig.9. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.



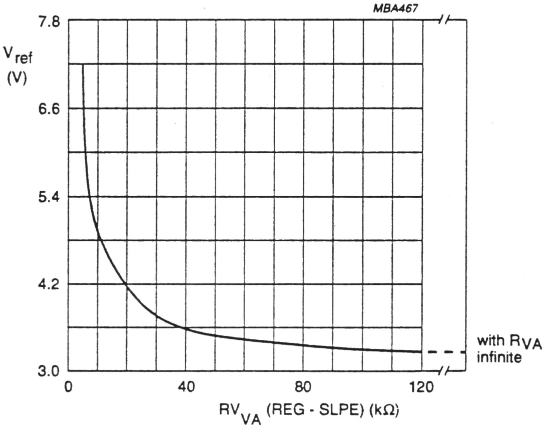
R16 = 392 Ω; I_p with respect to Fig.3.

Fig.7 Typical AC output swing at total harmonic distortion (THD) = 2% on the line as a function of line current with peripheral supply current as a parameter.



L_{eq} = C3 x R9 x R_p
R_p = 15 kΩ

Fig.8 Equivalent impedance between LN and V_{EE}.



$V_{LN} = V_{LN\text{-}SLPE} + (\{I_{line} - 1.55 \times 10^{-3}\ A\} \times R9)$.

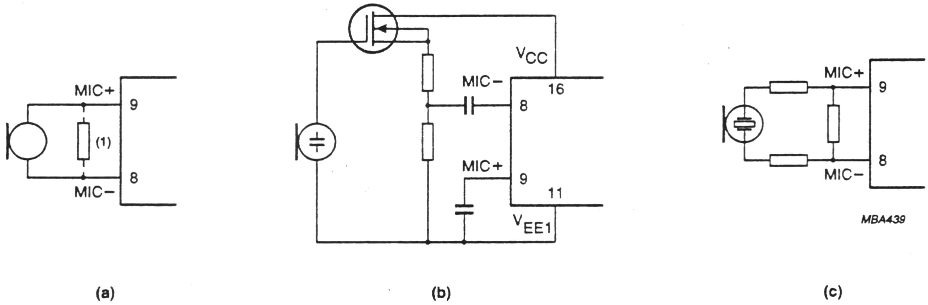
Fig.9 Internal reference voltage $V_{LN\text{-}SLPE}$ as a function of resistor $R_{VA(REG\text{-}SLPE)}$ for line currents between 11 mA and 140 mA.

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The TEA1064B has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typicallly 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig.10.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.



Resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs.

Fig.10 Microphone arrangements (a) magnetic or dynamic microphone (b) electret microphone (c) piezo-electric microphone currents.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC– but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.11.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit ($V_{LN\text{-}SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased. Fig.12 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN\text{-}SLPE}$) with I_{line} $-I_p$ as a parameter.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

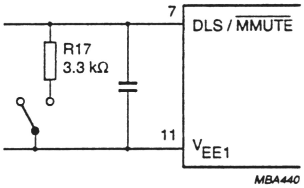
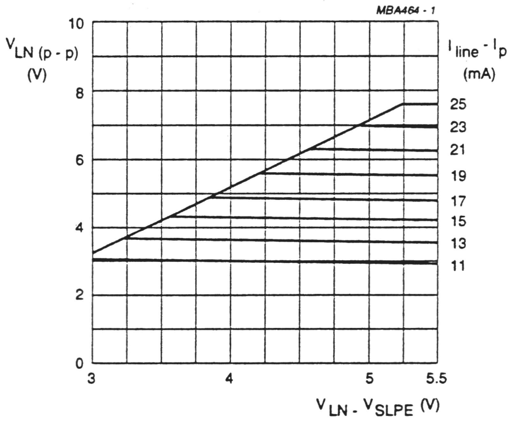
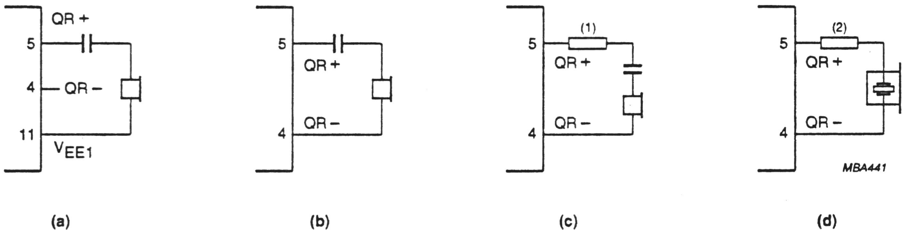


Fig.11 Microphone-mute function.



R16 = 392 Ω.

Fig.12 Typical output swing on line as a function of the DC voltage drop $V_{LN\text{-}SLPE}$ with I_{line} - I_p as a parameter.

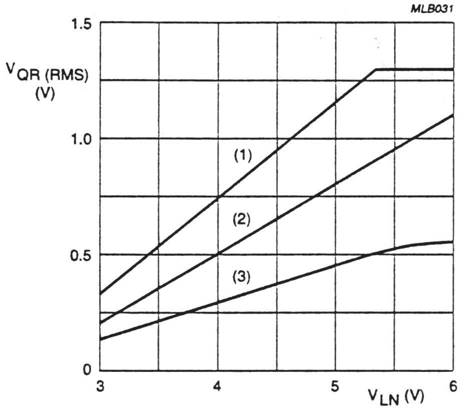


Resistor (1) may be connected to prevent distortion (inductive load).
Resistor (2) is required to increase the phase margin (stability with capacitive load).

Fig.13 Alternative receiver arrangements (a) dynamic earpiece with an impedance less than 450 Ω (b) dynamic earpiece with an impedance more than 450 Ω (c) magnetic earpiece with an impedance more than 450 Ω (d) piezo-electric earpiece.

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complimentary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.13). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.



Valid for both options; THD = 2%, I_{line} = 15 mA.
Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω; f = 3400 Hz.
Curve (2) is for a differential load of 450 Ω; f = 1 kHz.
Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Fig.14 Typical output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter.

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig.14 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE1}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 dB diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig.15 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then provide their maximum gain.

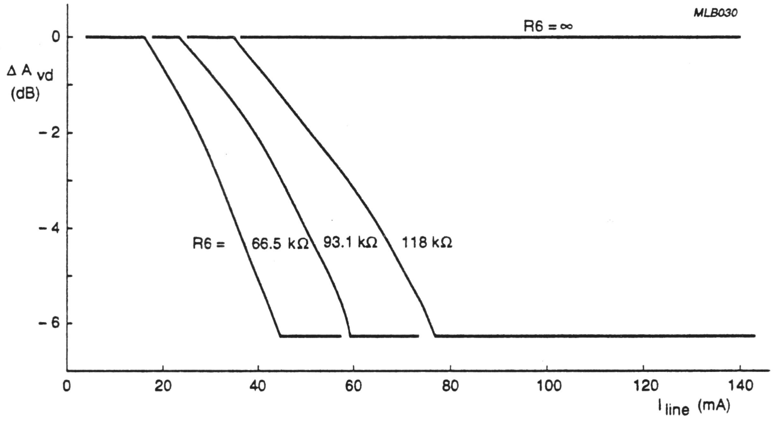


Fig.15 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	35	84.5	66.5	x	x
	48	118	93.1	77.8	66.5
	60	x	x	97.6	84.5

V_{EE2} input

V_{EE2} is the reference for MUTE, POWER-DOWN and DTMF inputs. These signals are referenced to V_{EE1} when generated by peripherals powered between V_{CC} and V_{EE1}, but they can also be referenced to SLPE when peripherals are powered as shown in Fig.3. In the first instance (reference to V_{EE1}), V_{EE2} has to be connected to V_{EE1}. In the second instance (reference to SLPE), V_{EE2} has to be connected to SLPE.

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on the line. The voltage gain between DTMF-V_{EE2} and LN-V_{EE1} is typically 26.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 25.5 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC} or for the peripherals between V_{LN} and SLPE. These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by an applied HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from 1.3 mA (typ.) to 60 µA (typ.) and switches off the voltage regulator to prevent discharge via LN to V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to V_{EE2}.

Sidetone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig.16). Maximum compensation is obtained when the following conditions are fulfilled:

(a) $R9 \times R2 = R1 \times (R3 + \{R8//Z_{bal}\})$

(b) $(Z_{bal}/\{Z_{bal} + R8\}) = (Z_{line}/\{Z_{line} + R1\})$

If fixed values are chosen for R1, R2, R3 and R9, then condition (a) is always fulfilled provided $|R8//Z_{bal}| \ll R3$

To obtain optimum sidetone suppression, condition (b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensure correct anti-sidetone bridge operation
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain

In practise Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

EXAMPLE

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω//140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in : R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.16 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (see Fig.17). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011).

Notes

1. The reference level used for the MUTE, DTMF and PD inputs is V_{EE2}.
2. A LOW level for any of these pins is defined by connection to V_{EE2}, a HIGH level is defined as a voltage greater than V_{EE2} + 1.5 V and smaller than V_{CC} + 0.4 V.

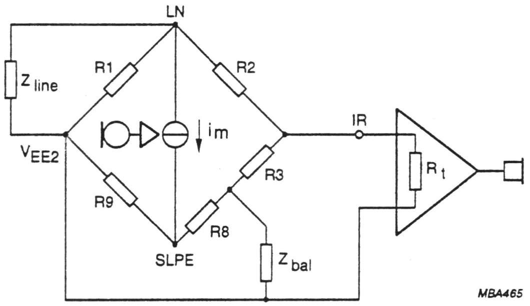


Fig.16 Equivalent circuit of TEA1060 family anti-sidetone bridge.

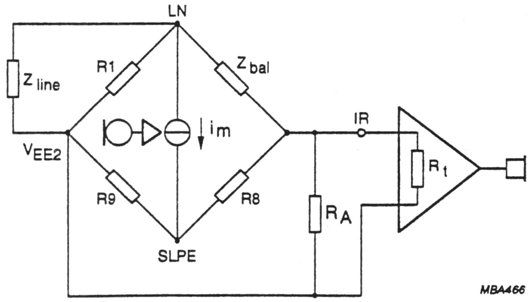


Fig.17 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		–	12	V
V_{LN}	repetitive line voltage during switch-on line interruption		–	13.2	V
V_{LN}	repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.22	–	28	V
I_{LN}	line current	R9 = 20 Ω			
	TEA1064B	note 1	–	140	mA
	TEA1064BT	note 1	–	140	mA
V_i	input voltage on pins other than LN		$V_{EE1}-0.7$	$V_{CC}+0.7$	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1064B		–	717	mW
	TEA1064BT		–	555	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes

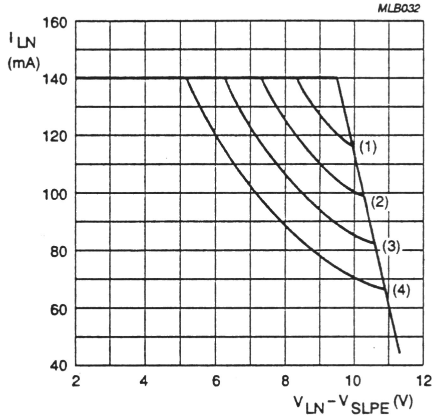
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs18 and 19 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	70 K/W
	SOT163A (note 1)	90 K/W

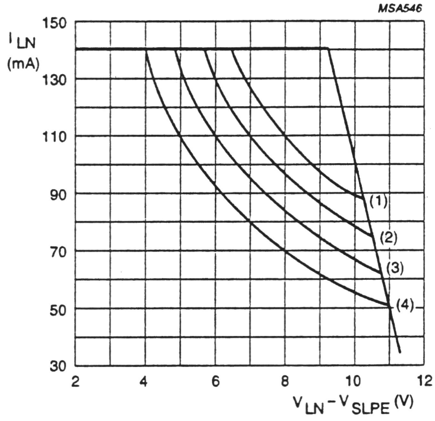
Note

1. Mounted on glass epoxy board 41 x 19 x 1.5 mm.



(1) T_{amb} = 45 °C; P_{tot} = 1143 mW.
(2) T_{amb} = 55 °C; P_{tot} = 1000 mW.
(3) T_{amb} = 65 °C; P_{tot} = 857 mW.
(4) T_{amb} = 75 °C; P_{tot} = 714 mW.

Fig.18 TEA1064B safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.19 TEA1064BT safe operating area.

CHARACTERISTICS

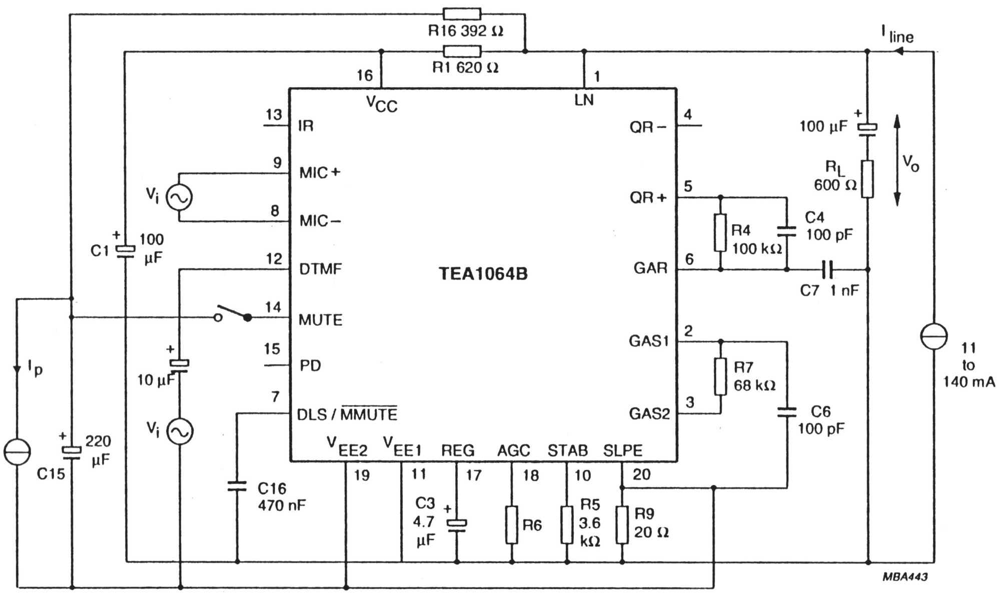
I_{line} = 11 to 140 mA; V_{EE1} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuits of Fig.20 or Fig.21; V_{EE2} connected to SLPE; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 16)						
V_{LN}	DC line voltage: voltage drop between LN and V_{EE1}	MIC−, MIC+ inputs open-circuit; without R_{VA}				
		I_{line} = 2 mA	−	1.8	−	V
		I_{line} = 4 mA	−	2.2	−	V
		I_{line} = 7 mA	−	3.2	−	V
		I_{line} = 11 mA	−	3.4	−	V
		I_{line} = 15 mA	3.25	3.5	3.75	V
		I_{line} = 100 mA	−	5.25	6.05	V
		I_{line} = 140 mA	−	6.1	7.0	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	−3	−1	+1	mV/K
V_{LN}	voltage drop over circuit with R_{VA} connected between REG and SLPE					
		R_{VA} = 33 kΩ	3.8	4.1	4.4	V
		R_{VA} = 20 kΩ	4.05	4.4	4.75	V
I_{CC}	internal supply current into pin 16	V_{CC} = 2.8 V				
		PD = LOW	−	1.3	1.6	mA
		PD = HIGH	−	60	82	µA
V_{CC}	supply voltage available for peripheral circuitry V_{EE2} connected to V_{EE1}	I_{line} = 15 mA; MUTE = HIGH; see Fig.5				
		I_p = 0.54 mA	2.2	2.4	−	V
		I_p = 0 mA	2.5	2.7	−	V
V_p	supply voltage available for peripheral circuitry	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	−	V
		I_p = 2.7 mA; $R_{REG\text{-}SLPE}$ = 20 kΩ	2.9	3.1	−	V
Microphone inputs MIC− and MIC+ (pins 8 and 9)						
Z_i	input impedance					
	differential		51	64	77	kΩ
	single-ended		25.5	32.0	38.5	kΩ
CMRR	common mode rejection ratio		−	82	−	dB
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	51	52	53	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	−0.5	±0.1	+0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_vT	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	–	dB
DTMF input (pin 12)						
Z_i	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
ΔG_vf	variation of G_v with frequency referred to 0.8 kHz					
		f = 300 and 3400 Hz	−0.5	±0.01	+0.5	dB
		f = 697 and 1633 Hz	−0.2	±0.05	+0.2	dB
ΔG_vT	variation of G_v with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	0.5	dB
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain adjustment range		−8	–	+0	dB
Sending amplifier output LN (pin 1)						
DYNAMIC LIMITER						
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; $V_{i(RMS)}$ = 3.6 mV	3.4	3.8	4.2	V
THD	total harmonic distortion					
		V_i = 3.6 mV +10 dB	–	1.5	–	%
		V_i = 3.6 mV +15 dB	–	2.8	–	%
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	V_i = 3.6 mV +10 dB				
		I_p = 1.4 mA	3.55	3.8	4.05	V
		I_p = 2.7 mA	3.25	3.5	3.75	V
		I_p = 0 mA; I_{line} = 7 mA	–	1.8	–	V
		I_p = 0 mA; I_{line} = 4 mA	–	0.9	–	V
	dynamic behaviour of limiter	C16 = 470 nF				
t_{att}	attack time V_{mic} jumps from 2 mV to 40 mV		–	1.5	5.0	ms
t_{rel}	release time V_{mic} jumps from 40 mV to 2 mV		50	150	–	ms
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	–	−72	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiving amplifier input IR (pin 13)						
Z_i	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR− and QR+ (pins 4 and 5)						
Z_o	output impedance	single-ended	–	4	–	Ω
G_v	voltage gain (see Fig.21)	I_{line} = 15 mA; R4 = 100 kΩ				
	single-ended	R_T = 300 Ω	30	31	32	dB
	differential	R_T = 600 Ω	36	37	38	dB
$\Delta G_v f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	−0.5	−0.2	0	dB
$\Delta G_v T$	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	–	dB
$V_{o(RMS)}$	output voltage (RMS value)	TDA = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA				
	single-ended	R_T = 150 Ω	–	0.2	–	V
	differential	R_T = 450 Ω	–	0.37	–	V
	differential	C_T = 47 nF; R_s = 100 Ω; f = 3400 Hz	–	0.52	–	V
$V_{o(RMS)}$	output voltage (RMS value)	I_p = 0 mA; TDA = 10%; sinewave drive; R4 = 100 kΩ; R_T = 150 Ω				
		I_{line} = 4 mA	–	20	–	mV
		I_{line} = 7 mA	–	160	–	mV
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open-circuit				
	single-ended	R_T = 300 Ω	–	45	–	µV
	differential	R_T = 600 Ω	–	90	–	µV
$V_{no(RMS)}$	noise output voltage (RMS value)	see Fig.21; S1 in position 2; 200 Ω between MIC− and MIC+; single-ended; R_T = 300 Ω				
		R7 = 68 kΩ	–	100	–	µV
		R7 = 24.9 kΩ	–	65	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment input GAR (pin 6)						
ΔG_v	receiving amplifier gain adjustment range		−11	−	+8	dB
MUTE input (pin 14)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	−	V_{CC} +0.4	V
V_{IL}	LOW level input voltage		0	−	0.3 +V_{EE2}	V
I_{mute}	input current		−	11	20	µA
ΔG_v	change of microphone amplifier gain at mute on	MUTE = HIGH	−	−100	−	dB
G_v	voltage gain from input DTMF-SLPE to QR+ output with mute on	MUTE = HIGH; single-ended load; R_L = 300 Ω	−	−18	−	dB
Power-down input PD (pin 15)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	−	V_{CC1} +0.4	V
V_{IL}	LOW level input voltage		0	−	0.3 +V_{EE2}	V
I_{PD}	input current		−	5	10	µA
Automatic gain control input AGC (pin 18)						
	controlling the gain from IR (pin13) to QR+, QR− (pins 4, 5) and the gain from MIC+, MIC− (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)				
G_v	gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	−5.7	−6.1	−6.5	dB
I_{line}	highest line current for maximum gain		−	24	−	mA
I_{line}	lowest line current for minimum gain		−	61	−	mA
ΔG_v	change of gain between I_{line} = 15 and 35 mA		−0.9	−1.4	−1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
V_{IL}	LOW level input voltage		V_{EE1}	−	V_{EE1} +0.3	V
I_{IL}	input current at LOW level input voltage		−85	−60	−35	µA
t_{rel}	release time after a LOW level on pin 7	C16 = 470 nF	−	30	−	ms
ΔG_v	change of microphone amplifier gain at LOW level input voltage on pin 7		−	−100	−	dB


R16 392 Ω
R1 620 Ω
I line
16
1
VCC
LN
TEA1064B
13
IR
9
MIC+
8
MIC−
12
DTMF
14
MUTE
15
PD
7
DLS / MMUTE
VEE2
VEE1
REG
AGC
STAB
SLPE
19
11
17
18
10
20
4
QR−
5
QR+
6
GAR
2
GAS1
3
GAS2
Vi
Vi
C1 100 µF
10 µF
C15 220 µF
Ip
C16 470 nF
C3 4.7 µF
R6
R5 3.6 kΩ
R9 20 Ω
R4 100 kΩ
C4 100 pF
C7 1 nF
R7 68 kΩ
C6 100 pF
100 µF
RL 600 Ω
Vo
11 to 140 mA
MBA443

For measuring gain from MIC+ amd MIC– the MUTE input should be LOW or open-circuit.
For measuring the DTMF input, the MUTE input should be HIGH.
Inputs not being tested should be open-circuit.

Fig.20 Test circuit for defining voltage gain of MIC–, MIC+ and DTMF inputs; voltage gain (G_v) is defined as $20\log|V_o/V_i|$.

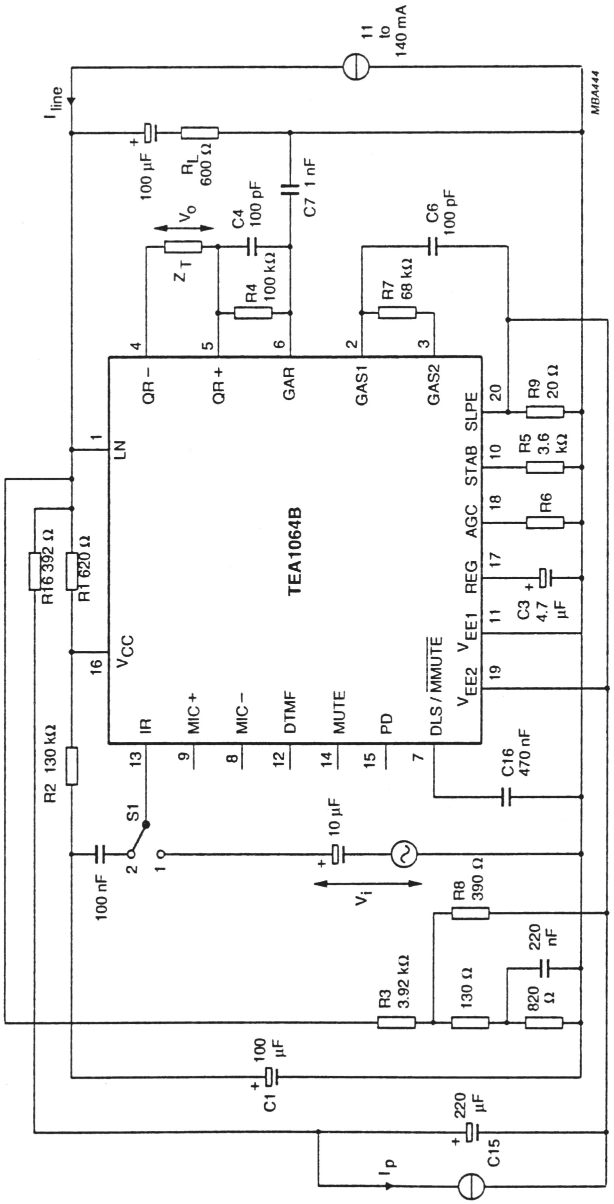
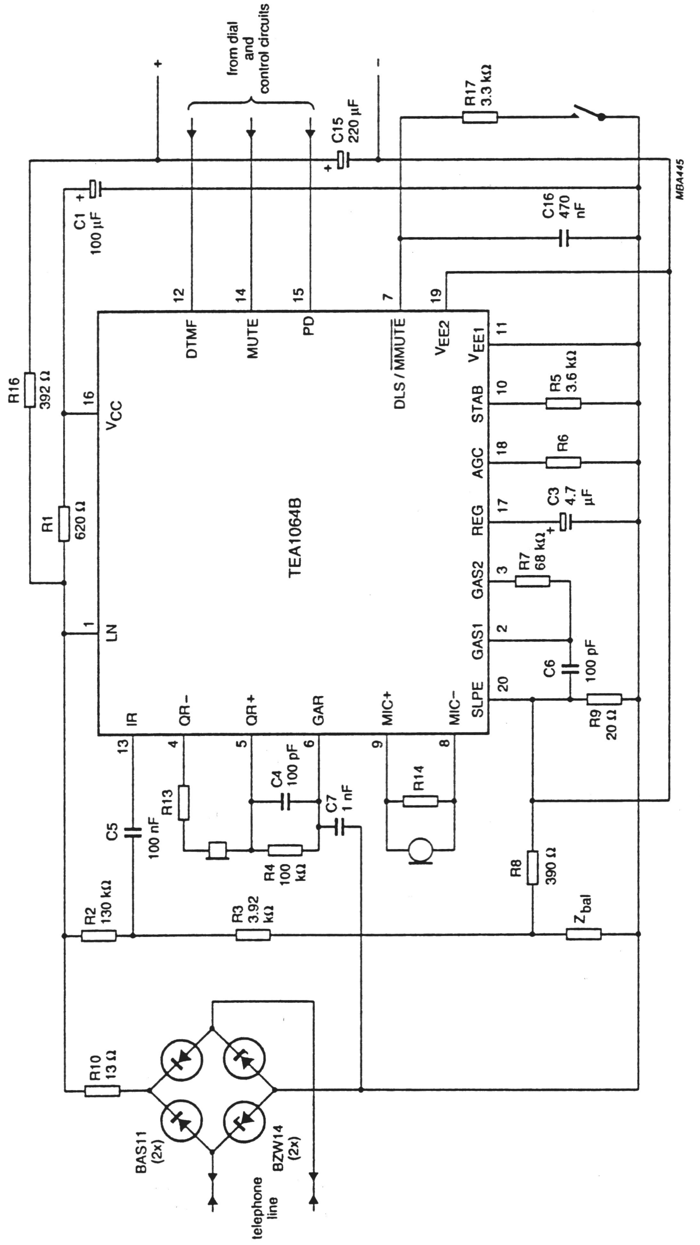

11 to 140 mA
I_{line}
MBA444
100 µF
R_L 600 Ω
C7 1 nF
V_o
C4 100 pF
Z_T
R4 100 kΩ
C6 100 pF
R7 68 kΩ
4
5
6
2
3
QR −
QR +
GAR
GAS1
GAS2
SLPE
20
R9 20 Ω
STAB
10
R5 3.6 kΩ
AGC
18
R6
REG
17
C3 4.7 µF
V_{EE1}
11
V_{EE2}
19
DLS / MMUTE
LN
1
TEA1064B
V_{CC}
16
R16 392 Ω
R1 620 Ω
R2 130 kΩ
IR
13
MIC +
9
MIC −
8
DTMF
12
MUTE
14
PD
15
7
C16 470 nF
S1
2
1
100 nF
10 µF
V_i
R8 390 Ω
220 nF
R3 3.92 kΩ
130 Ω
820 Ω
C1 100 µF
C15 220 µF
I_p

Fig.21 Test circuit for defining voltage gain of the receiving amplifier; voltage gain (G_v) is defined as $20\log|V_o/V_i|$ (with S1 in position 1).

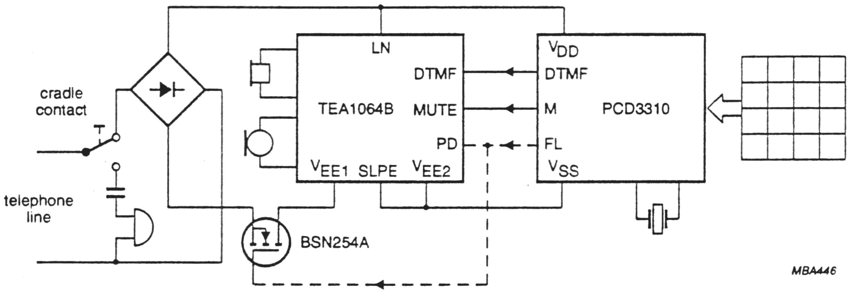
APPLICATION INFORMATION

The basic application circuit is shown in Fig.22 and some typical application are shown in Fig.23, Fig.24 and Fig.25.


TEA1064B
from dial and control circuits
+
−
C15 220 µF
R17 3.3 kΩ
C1 100 µF
C16 470 nF
MBA445
R16 392 Ω
R1 620 Ω
16 VCC
1 LN
12 DTMF
14 MUTE
15 PD
7 DLS / MMUTE
19 VEE2
11 VEE1
10 STAB
18 AGC
17 REG
3 GAS2
2 GAS1
20 SLPE
13 IR
4 QR−
5 QR+
6 GAR
9 MIC+
8 MIC−
R5 3.6 kΩ
R6
C3 4.7 µF
R7 68 kΩ
C6 100 pF
R9 20 Ω
C5 100 nF
R13
C4 100 pF
C7 1 nF
R4 100 kΩ
R14
R8 390 Ω
R2 130 kΩ
R3 3.92 kΩ
Zbal
R10 13 Ω
BAS11 (2x)
BZW14 (2x)
telephone line

The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

Fig.22 Basic application of TEA1064B with SLPE as supply reference for peripherals, shown here with piezo-electric earpiece and DTMF dialling.


LN
DTMF
TEA1064B
MUTE
PD
V_{EE1} SLPE V_{EE2}
V_{DD}
DTMF
M
PCD3310
FL
V_{SS}
cradle contact
telephone line
BSN254A
MBA446

The broken line indicates optional flash (register recall by timed loop break).

Fig.23 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064B with the CMOS bilingual dialling circuit PCD3310.

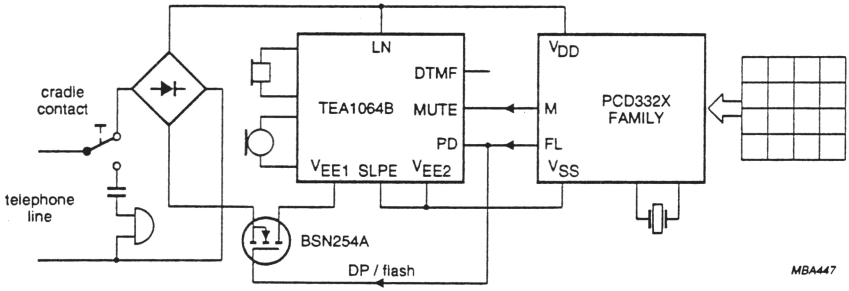

LN
DTMF
TEA1064B
MUTE
PD
V_{EE1} SLPE V_{EE2}
V_{DD}
M
PCD332X FAMILY
FL
V_{SS}
cradle contact
telephone line
BSN254A
DP / flash
MBA447

Fig.24 Typical pulse dial set application circuit (simplified) showing the TEA1064B with one of the PCD331X family of CMOS interrupted current-loop dialling circuits.

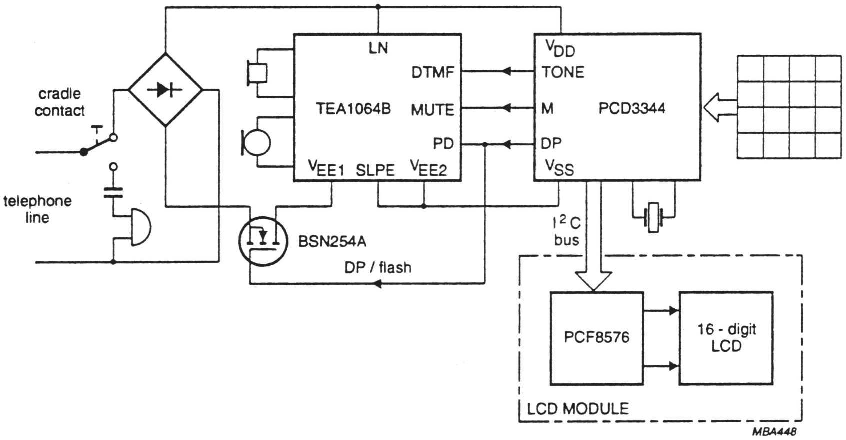

cradle contact
telephone line
LN
DTMF
TEA1064B
MUTE
PD
V_{EE1} SLPE V_{EE2}
V_{DD}
TONE
M
PCD3344
DP
V_{SS}
I^2C bus
BSN254A
DP / flash
PCF8576
16 - digit LCD
LCD MODULE
MBA448

Fig.25 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064B and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I^2C-bus.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	March 1994

TEA1065

Versatile telephone transmission circuit with dialler interface

FEATURES

- Current and voltage regulator mode with adjustable static resistances
- Provides supply for external circuitry
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power-down input for pulse dial or register recall
- Digital pulse input to drive an external switch transistor
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (on microphone and earpiece amplifiers)
- Adjustable gain control
- DC line voltage adjustment facility

GENERAL DESCRIPTION

The TEA1065 is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets with adjustable DC mask. The circuit performs electronic switching between dialling and speech internally.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1065	24	DIL	plastic	SOT101L
TEA1065T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.25	4.45	4.65	V
I_{line}	normal operation line current range		10	-	150	mA
I_{CC}	internal supply consumption					
	power-down input LOW		-	1.14	1.5	mA
	power-down input HIGH		-	73	105	µA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH				
		I_P = 1.2 mA	2.7	-	-	V
		I_P = 1.55 mA	2.5	-	-	V
G_V	voltage gain range					
	microphone amplifier		30	-	46	dB
	earpiece amplifier		20	-	45	dB
ΔG_V	line loss compensation gain control range		−5.5	−5.9	−6.3	dB
T_{amb}	operating ambient temperature range		−25	-	+75	°C

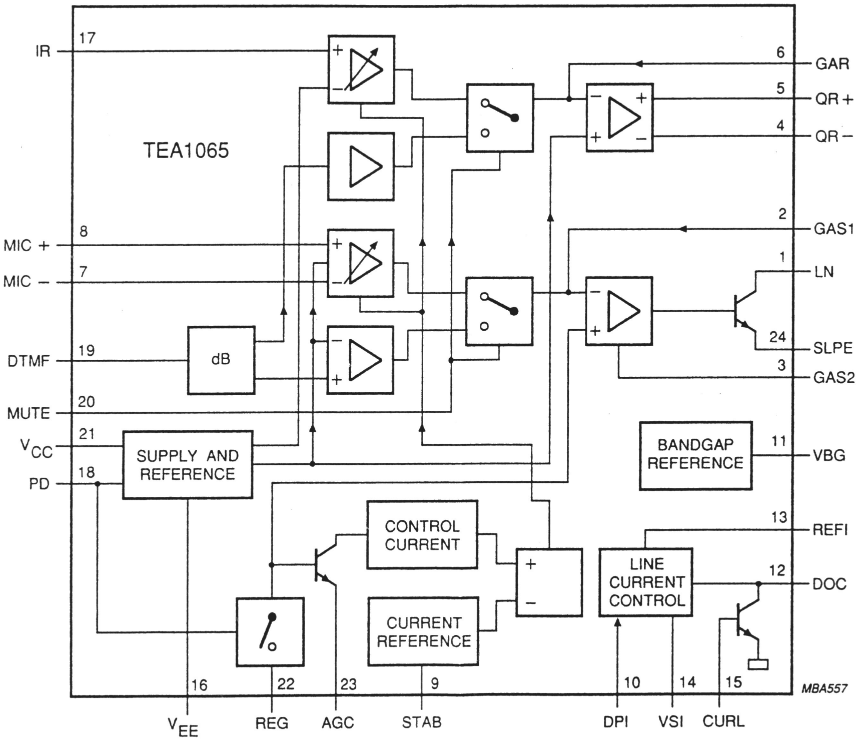

IR
17
TEA1065
MIC +
8
MIC −
7
DTMF
19
dB
MUTE
20
VCC
21
SUPPLY AND REFERENCE
PD
18
6
GAR
5
QR +
4
QR −
2
GAS1
1
LN
24
SLPE
3
GAS2
BANDGAP REFERENCE
11
VBG
13
REFI
CONTROL CURRENT
CURRENT REFERENCE
LINE CURRENT CONTROL
12
DOC
16
VEE
22
REG
23
AGC
9
STAB
10
DPI
14
VSI
15
CURL
MBA557

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; sending amplifier
GAS2	3	gain adjustment; sending amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
MIC–	7	inverting microphone input
MIC+	8	non-inverting microphone input
STAB	9	current stabilizer
DPI	10	digital pulse input
VBG	11	bandgap output reference
DOC	12	drive current output
REFI	13	reference voltage input
VSI	14	voltage sense input
CURL	15	current limitation input
V_{EE}	16	negative line terminal
IR	17	receiving amplifier input
PD	18	power-down input
DTMF	19	dual-tone multifrequency input
MUTE	20	MUTE input
V_{CC}	21	positive supply decoupling
REG	22	voltage regulator decoupling
AGC	23	automatic gain control input
SLPE	24	slope (DC resistance) adjustment

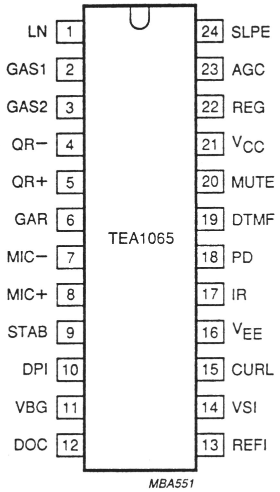

LN 1
GAS1 2
GAS2 3
QR− 4
QR+ 5
GAR 6
MIC− 7
MIC+ 8
STAB 9
DPI 10
VBG 11
DOC 12
24 SLPE
23 AGC
22 REG
21 V_{CC}
20 MUTE
19 DTMF
18 PD
17 IR
16 V_{EE}
15 CURL
14 VSI
13 REFI
TEA1065
MBA551

Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripherals are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} (pin 21) and regulates its voltage drop between LN and SLPE (pins 1 and 24). The internal supply requires a decoupling capacitor between V_{CC} and V_{EE} (pin 16); the internal voltage regulator has to be decoupled by a capacitor from REG (pin 22) to V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor connected between STAB (pin 9) and V_{EE}.
The TEA1065 can be set either in a DC voltage regulator mode or in a DC current regulator mode. The DC mask can be selected by connecting the appropriate external components to the dedicated pins (VSI, REFI, DOC, VBG).
When the DC current regulator mode is not required it can be cancelled by connecting pin VSI to V_{EE}; pins REFI, VBG and DOC are left open-circuit.

Voltage regulator mode

The voltage regulator mode is achieved when the line current is less than the current I_{knee} as illustrated in Fig.3. With R13 = R14 = 30 kΩ, the current I_{knee} = 30 mA (I_p = 0 mA).

This line current value will be reached when the voltage on pin VSI (almost equal to the voltage on pin SLPE) exceeds the voltage on pin REFI (equal to the voltage on pin VBG divided by the resistor tap R13, R14). For other values of R13 and R14, the I_{knee} current is given by the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} - (R15/R9) \times I_O(VSI)$$

I_{CC} is the current required by the circuit itself (typ. 1.14 mA).
I_P is the current required by the peripheral circuits connected between V_{CC} and V_{EE}. $I_{O(VSI)}$ is the output current from pin VSI (typ. 2.5 μA).

The DC slope of the V_{line}/I_{line} curve is, in this mode, determined by R9(R9 = R9a + R9b) in series with the r_{ds} of the external line current control transistor (see Fig.4; $r_{ds} = \partial V_{GS}/\partial I_D$ at $V_{GS} = V_{DS}$).

Current regulator mode

The current regulator mode is achieved when the line current is greater than I_{knee}. In this mode, the slope of the V_{line}/I_{line} curve is approximately 1300 Ω with R9 = 20 Ω, R16 = 1 MΩ, R13 = R14 = 30 kΩ. For other values of these resistances, the slope value can be approximated by the following formula:
$R9 \times \{1 + R16 \times (1/R13 + 1/R14)\}$

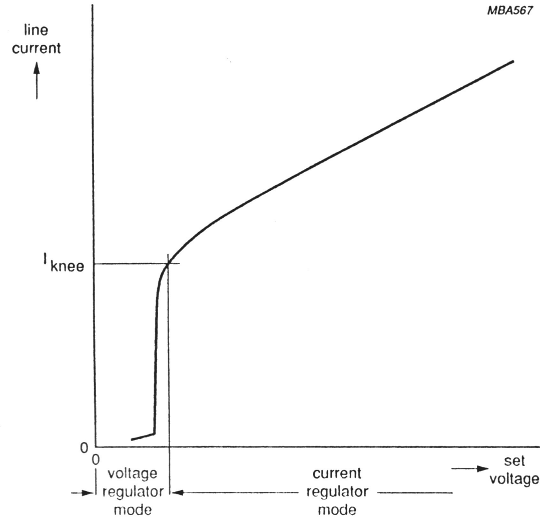


Fig.3 Voltage and current regulator mode.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).
If the line current exceeds I_{CC} +0.3 mA, required by the circuit itself ($I_{CC} \approx 1.14$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC} then the voltage regulator will divert the excess current via LN.

$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.3 \times 10^{-3} - I_p) \times R9$

where: V_{ref} is an internally generated temperature compensated reference voltage of 4.18 V and R9 is an external resistor connected between SLPE and V_{EE}.

The preferred value of R9 is 20 Ω. Changing R9 will influence the microphone gain, gain control characteristics, sidetone and the maximum output swing on LN. In this instance, the voltage on the line (excluding the diode rectifier bridge; see Fig.4) is:

$V_{line} = V_{LN} + V_{GS} + R16 \times I_{DOC}$

where: V_{GS} is the voltage drop between the gate and source terminal of the external line current control transistor and I_{DOC} is the current sunk by pin DOC (I_{DOC} = 0 in the voltage regulator mode and increases with I_{line} in the current regulator mode).
Under normal conditions $I_{SLPE} >> I_{CC} + 0.3\text{ mA} + I_p$ and for the voltage regulator mode ($I_{line} < I_{knee}$), the static behavior of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor. For the current regulator mode ($I_{line} > I_{knee}$), the static behaviour of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor and also in series with a DC voltage source R16 x I_{DOC} (the preferred value of R16 is 1 MΩ at this value the current I_{DOC} is negligible compared to I_{line}).

In the audio frequency range the dynamic impedance between LN and V_{EE} is equal to R1 (see Fig.8). The internal reference voltage V_{ref} can be adjusted by means of an external resistor R_{VA}. This resistor, connected between LN and REG, will decrease the internal reference voltage. When R_{VA} is connected between REG and SLPE the internal reference voltage will increase.
The maximum allowed line current is given in Figs 5 and 6, where the current is shown as a function of the required reference voltage, ambient temperature and applied package.

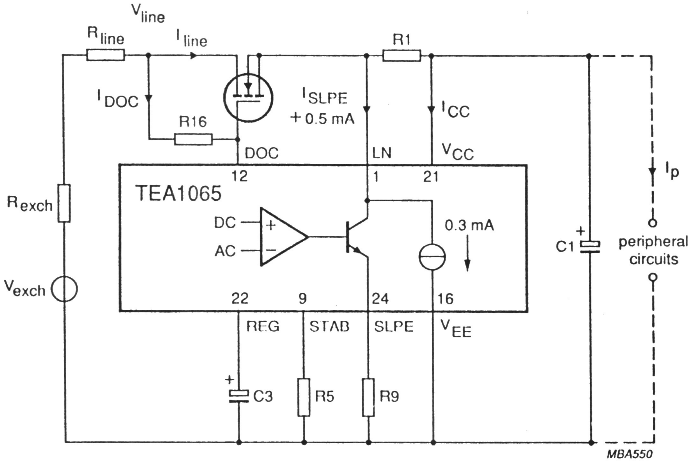
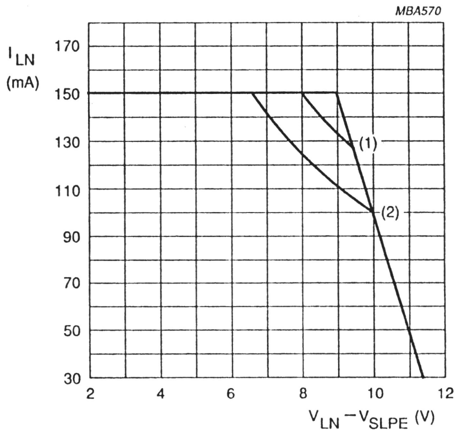


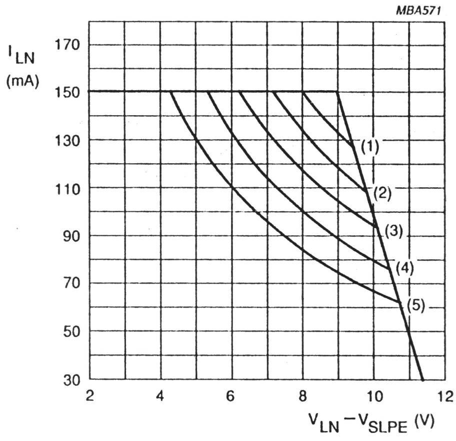
Fig.4 Supply arrangement.

The current I_P, available from V_{CC} for supplying peripheral circuits, depends on the external components and on the line current. Fig.7 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, where 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for a back-up diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven (earpiece amplifier supplied from V_{CC}).



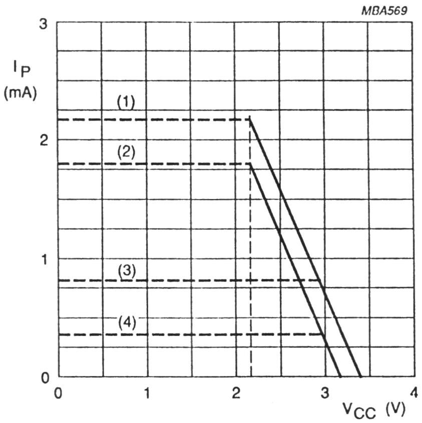
	T_{amb}	P_{tot}
(1)	65 °C	1.2 W
(2)	75 °C	1.0 W

Fig.5 TEA1065 safe operating area.



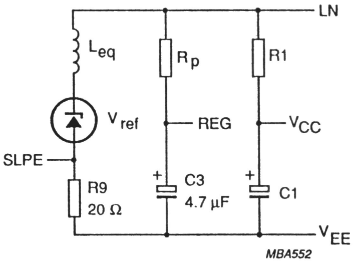
	T_{amb}	P_{tot}
(1)	35 °C	1.2 W
(2)	45 °C	1.07 W
(3)	55 °C	0.93 W
(4)	65 °C	0.8 W
(5)	75 °C	0.67 W

Fig.6 TEA1065T safe operating area.



I_{line} = 15 mA at V_{LN} = 4.45 V
R1 = 620 Ω
R9 = 20 Ω

Fig.7 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curve (1) and (3) are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (2) and (4) are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical). (1) = 2.2 mA; (2) = 1.77 mA; (3) = 0.78 mA and (4) = 0.36 mA.



L_{eq} = C3 x R9 x R_p
R_p = 17.5 kΩ

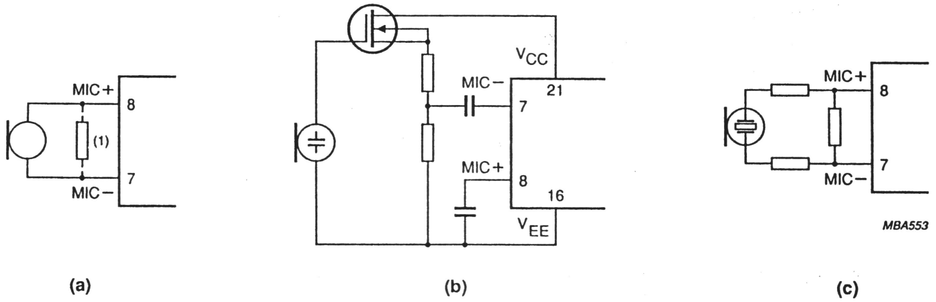
Fig.8 Equivalent circuit impedance between LN and V_{EE}.

Microphone inputs MIC+ and MIC– and gain adjustment connections GAS1 and GAS2

The TEA1065 has symmetrical microphone inputs, its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage gain is typ. 38 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezoelectric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphones types are illustrated in Fig.9.

The gain of the microphone amplifier is proportional to external resistor R7, connected between GAS1 and GAS2, which can be adjusted between 30 dB and 46 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R7 x C6.



(a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs;

(b) electret microphone;

(c) piezoelectric microphone.

Fig.9 Microphone arrangements.

MUTE input

When MUTE = HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. When MUTE = LOW or open-circuit the DTMF input is inhibited and the microphone and receiving amplifier inputs are enabled. Switching the MUTE input will cause negligible clicks at the earpiece outputs and on the line. An electrostatic discharge protection diode is connected between pin MUTE and pin V_{CC} (pins 20 and 21).

Dual-tone multifrequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 12.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier. When R7 = 68 kΩ the gain is typically 25.5 dB. The signaling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifiers: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR– (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.10). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, which is sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when earpiece impedance exceeds 450 Ω as with high impedance dynamic, magnetic or piezoelectric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of −11 dB to +8 dB to suit the sensitivity of the transducer that is used. The gain is proportional to external resistor R4 connected between GAR and QR+.

Two external capacitors, C4 = 100 pF and C7 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

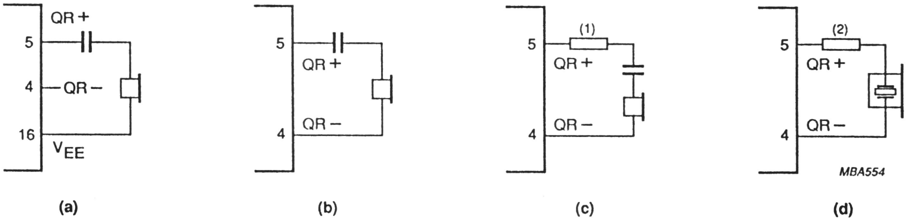


Fig.10 Alternative receiver arrangements: (a) dynamic earpiece with an impedance less than 450 Ω; (b) dynamic earpiece with an impedance more than 450 Ω; (c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); (d) piezoelectric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

Automatic gain control

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current (see Fig.12). The control range is 5.9 dB; this corresponds to a line length of 3.5 km of twisted pair cable (see Fig.11). The DTMF gain is not affected by this feature.

If automatic line loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then give their maximum gain.

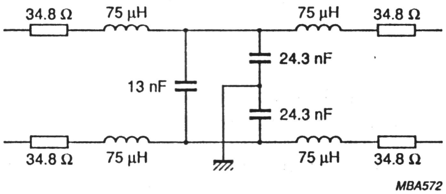


Fig.11 Typical 0.5 km line cell model used for automatic gain control optimization.

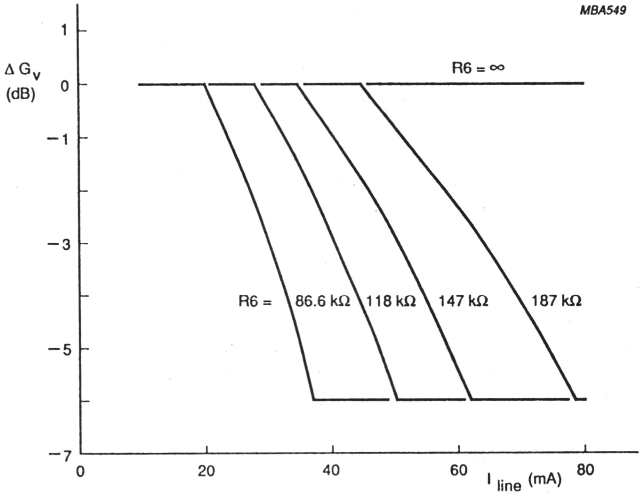


Fig.12 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Power-down input PD

During pulse dialling or register recall (timed-loop-break) the telephone line is interrupted, consequently it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirement on this capacitor is relaxed by applying a HIGH level to the PD input during the loop-break. This reduces the internal supply current from typ. 1.14 mA to 73 μA.

A HIGH level at PD also disconnects the capacitor at REG which results in the voltage stabilizer having no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit or connected to V_{EE}. An electrostatic discharge protection diode is connected between pin PD and V_{CC}.

Digital pulse input DPI

A HIGH level at DPI creates a current which flows from pin DOC to V_{EE} in order to interrupt the line current by the external line current control transistor (see Fig.18; MOSFET BUK554). A LOW level (or pin left open-circuit) disables this current to provide the normal DC regulation (voltage or current). A simple application without regulation of current in pulse dialling mode is given in Fig.18.

When DPI is activated (HIGH level), the external line current control transistor is switched off resulting in no current in the TEA1065. The voltage on pin SLPE becomes zero and capacitor C15 discharges cancelling the current regulation when DPI becomes inactive (LOW level).

To provide a constant regulation (in speech mode and pulse mode), an external transistor is required to keep C15 charged during DPI active (see Fig.19 in which the Field Effect Transistor BSJ177 is directly driven by the DPI signal).
An electrostatic discharge protection diode is connected between pin DPI and pin V_{CC}.

Voltage sense input and reference voltage input VSI and REFI

The voltage on pin VSI represents the DC voltage of pin SLPE. The RC filter (R15 x C15) is also intended to disable the DC regulation when C15 is shunted or not yet charged (especially directly after hook-off).
The time constant R15 x C15 determines approximatively the time when no regulation (except CURL pin limitation) is activated.
The voltage applied on pin REFI represents a fraction of the bandgap reference voltage given by pin VBG (resistor tap R13 and R14) in order to determine I_{knee}.

Drive current output DOC

Pin DOC drives the external line current control transistor in order to achieve line interruption during pulse dialling (or register recall) and also the DC slope when $I_{line} > I_{knee}$. The current sunk by pin DOC is determined by the voltage on pin VSI in comparison with the voltage on pin VBG divided by the resistor tap R13 and R14.
When pin DPI is activated, pin DOC changes to a low voltage (by trying to sink typ. 900 μA to V_{EE}) to switch off the external line current control transistor.

Bandgap reference output VBG

This output provides a voltage reference to set the knee line current with the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} \quad (R15/R9) \times 2.5 \times 10^{-6}$$

In order to improve stability, a capacitive load is not allowed on this output.

Current limit input CURL

This input is applied to the base of an internal NPN transistor which has its collector connected to pin DOC and its emitter to V_{EE} (see Fig.13). The transistor limits the line current just after hook-off or during line transients to a value given by the following formula:

$$I_{hook\text{-}off} = I(R1) + V_{BE}/R9b$$

V_{BE} is the base-emitter voltage of the transistor (typ. 700 mV at 25 °C).
I(R1) is the current flowing through R1 to charge C1 just after hook-off.

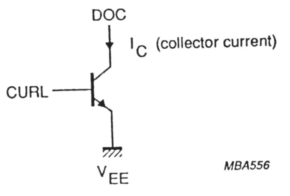


Fig.13 Internal current limiting transistor.

The maximum hook-off current then becomes:

$I_{hook\text{-}off} = V_Z/R1 + V_{BE}$ x (R9a + R9b + R1)/(R1 x R9b)

where V_Z is the Zener voltage of diode D5 (see Fig.18).

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line}, R2, R3, R9 and Z_{bal} (see Fig.18). Maximum compensation is obtained when the following conditions are fulfilled:

a) R9 x R2 = R1 x (R3 + R8)
b) k = R3 x (R8 + R9)/(R2 x R9)
c) Z_{bal} = k x Z_{line}

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice Z_{line} varies considerably with the line length and line type. Therefore, the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with long and short times. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

With k = 1, R1 = 619 Ω, R9 = 20 Ω and an average line impedance represented by 270 Ω + (120 nF // 1100 Ω), the calculation results in:

- R2 = 130 kΩ
- R3 = 3650 Ω
- R8 = 715 Ω

The anti-sidetone network for the TEA1060 family, shown in Fig.15, attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Note

More information on the balancing of the anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.

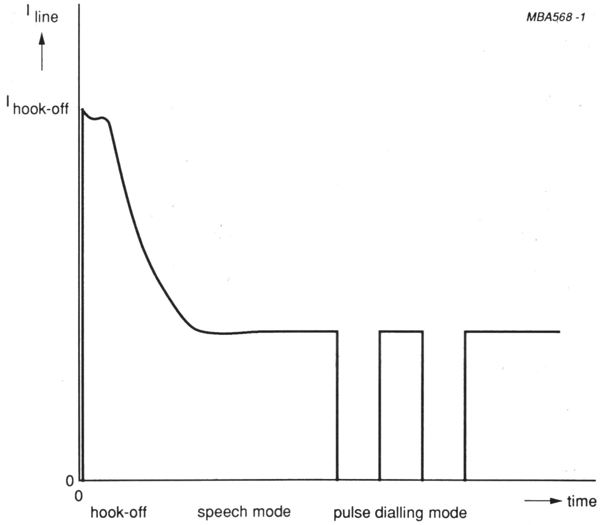


Fig.14 Example of line current shape in pulse dialling mode (see also Fig.18).

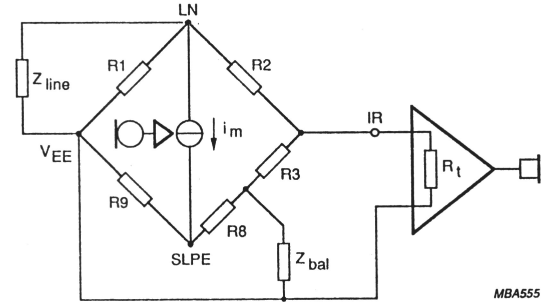


Fig.15 Equivalent circuit of TEA1060 family anti-sidetone bridge.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		-	12	V
V_{DOC}	positive DOC voltage continuous		-	12	V
V_{LN}	repetitive line voltage during switch-on or line interruption		-	13.2	V
I_{LN}	line current (see also Fig.5 and 6)		-	150	mA
V_I	input voltage on pins other than LN, DOC, VSI, REFI and CURL		V_{EE}-0.7	V_{CC}+0.7	V
P_{tot}	total power dissipation	see Figs 5 and 6			
T_{stg}	storage temperature range		−40	+ 125	°C
T_{amb}	operating ambient temperature range		−25	+75	°C
T_j	junction temperature		-	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\,j\text{-}a}$	from junction to ambient in free air	-	50	K/W
$R_{th\,j\text{-}a}$	from junction to ambient in free air	-	75	K/W

TEA1065T is mounted on glassy epoxy board 28.5 x 19.1 x 1.5 mm

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2, method 3015 (HBM 1500 Ω, 100 pF, 3 positive pulses and 3 negative pulses on each pin as a function of pin V_{EE}.

CHARACTERISTICS

I_{LN} = 10 to 150 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R9 = 20 Ω; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply LN and V_{CC} (pins 1 and 21)						
V_{LN}	voltage drop over circuit	I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.25	4.45	4.65	V
		I_{line} = 100 mA	5.4	6.1	6.7	V
		I_{line} = 140 mA	-	-	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	−3	−1	+1	mV/K
V_{LN}	voltage drop over circuit	I_{line} = 15 mA				
		$R_{VA} = R_{1-22}$ = 68 kΩ	3.6	3.9	4.15	V
		$R_{VA} = R_{22-24}$ = 39 kΩ	4.7	5.0	5.3	V
I_{CC}	supply current	PD = LOW; V_{CC} = 2.8 V	-	1.14	1.5	mA
		PD = HIGH; V_{CC} = 2.8 V	-	73	105	µA
Microphone inputs MIC+ and MIC− (pins 8 and 7)						
$\lvert Z_I \rvert$	input impedance		18.5	20.4	24.3	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	37	38	39	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA; f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to 75 °C; without R6	-	±0.5	-	dB
Dual-tone multi-frequency input DTMF (pin 19)						
$\lvert Z_I \rvert$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +75 °C	-	±0.5	-	dB
Gain adjustment GAS1 and GAS2 (pin 2 and 3)						
ΔG_v	gain variation with R7 connected between pins 2 and 3; transmitting amplifier		−8	-	+8	dB
Transmitting amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA				
		d_{tot} = 2%	1.9	2.3	-	V
		d_{tot} = 10%	-	2.6	-	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; pin 7 and 8 open-circuit psophometrically weighted (P53 curve); control transistor included (MOS BUK554 type see Fig.18)	-	−68	-	dBmp
Receiving amplifier input IR (pin 17)						
Z_I	input impedance		17	21	25	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiving amplifier outputs QR+ and QR – (pin 5 and 4)						
Z_O	output impedance		-	4	-	Ω
G_v	voltage gain	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	30	31	32	dB
		differential; RT = 600 Ω	36	37	38	dB
$\Delta G_v f$	variation with frequency referred to 800 Hz	f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v T$	variation with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	-	±0.2	-	dB
$V_{O(rms)}$	output voltage (RMS value)	I_{line} = 15 mA; THD = 2 %; sinewave drive; R4 = 100 kΩ				
		single-ended; RT = 150 Ω	0.3	0.38	-	V
		differential; RT = 450 Ω	0.56	0.72	-	V
		differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	0.87	1.07	-	V
		I_{line} = 30 mA; differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	1.02	1.22	-	V
$V_{O(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	-	50	-	µV
		differential; RT = 600 Ω	-	100	-	µV
Gain adjustment GAR (pin 6)						
ΔG_v	receiving amplifier, gain adjustment range		−11	-	+8	dB
Mute input MUTE (pin 20)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{MUTE}	input current		-	8	15	µA
ΔG_v	change of microphone amplifier gain	MUTE = HIGH	-	−70	-	dB
G_v	voltage gain from DTMF input to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ single-ended; RT = 300 Ω	−19	−17	−15	dB
Power-down input PD (pin 18)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{PD}	input current		-	2.5	5.0	µA
Automatic gain control input AGC (pin 23)						
ΔG_v	controlling the gain from IR to QR+, QR− and the gain from MIC+, MIC− to LN; gain control range with respect to I_{line} = 15 mA	R6 = 118 kΩ	−5.5	−5.9	−6.3	dB
I_{line}	highest line current for maximum gain		-	28	-	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	lowest line current for minimum gain		-	50	-	mA
ΔG_v	change of gain between I_{line} = 15 and 35.5 mA		–	-1.5	–	dB
Current limiting input CURL (pin 15)						
V_{BE}	base-emitter voltage drop of internal transistor	see Fig.13; $I_C = 50\ \mu A = I_{DOC}$	-	0.7	-	V
H_{FE}	current gain of internal transistor	see Fig.13; $I_C = 50\ \mu A = I_{DOC}$	60	120	-	
$I_{C(max)}$	maximum collector current of internal transistor	see Fig.13	-	-	2	mA
Bandgap reference voltage output VBG (pin 12)						
V_{BG}	reference voltage		–	1.22	–	V
I_{BG}	output drive capability	note 1	−100	-	+50	µA
Z_O	output impedance		-	12	-	Ω
Voltage sense input VSI (pin 14)						
I_O	output current	pin VSI connected to V_{EE}	-	-2.5	-	µA
Reference input REFI (pin 13)						
I_O	output current		-	-	2.0	mA
Drive current output DOC (pin 11)						
I_O	output current	REFI connected to V_{EE}; VSI not connected; DPI = LOW	120	300	-	µA
		REFI not connected; VSI connected to V_{EE}; DPI = HIGH	200	900	-	µA
Digital pulse input DPI (pin 10)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{DPI}	input current		-	2.5	5	µA

Note to the characteristics

1. No capacitive load on the V_{BG} output. Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

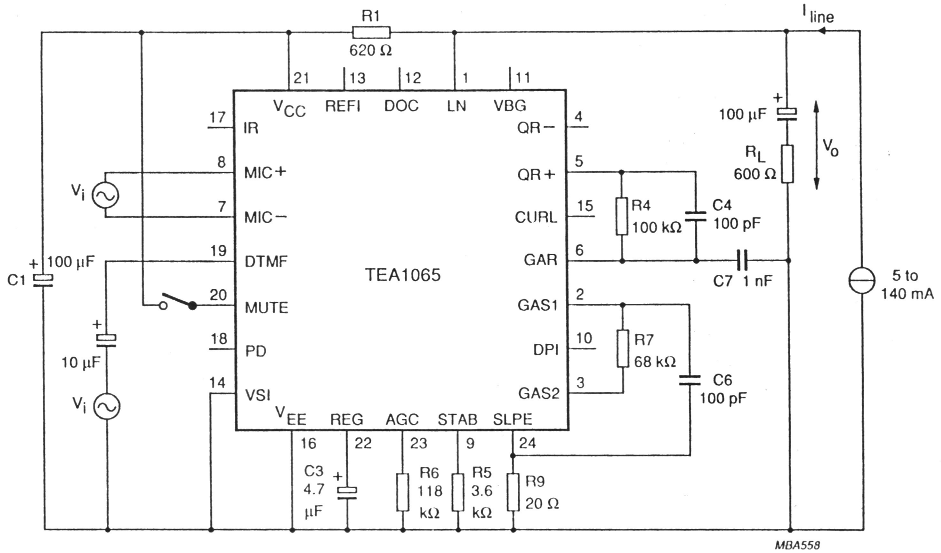

R1
620 Ω
I_{line}
21
13
12
1
11
V_{CC}
REFI
DOC
LN
VBG
17
IR
4
QR−
100 µF
R_L
600 Ω
V_o
8
MIC+
5
QR+
V_i
7
MIC−
15
CURL
R4
100 kΩ
C4
100 pF
C1
100 µF
19
DTMF
TEA1065
6
GAR
C7 1 nF
5 to
140 mA
20
MUTE
2
GAS1
10 µF
18
PD
10
DPI
R7
68 kΩ
V_i
14
VSI
3
GAS2
C6
100 pF
V_{EE}
REG
AGC
STAB
SLPE
16
22
23
9
24
C3
4.7
µF
R6
118
kΩ
R5
3.6
kΩ
R9
20 Ω
MBA558

Fig.16 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as $G_v = 20 \text{ Log}|V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open-circuit, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open-circuit except VSI that should be connected to V_{EE}.

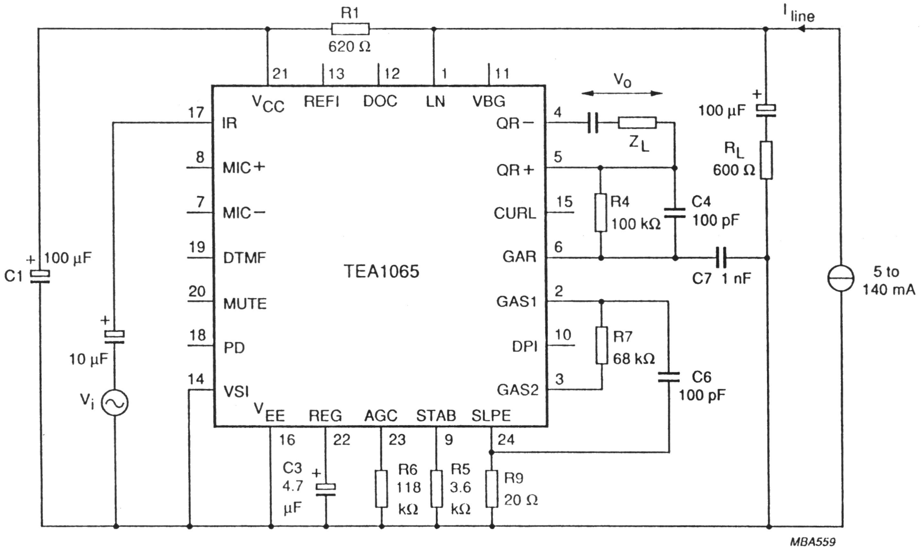

R1
620 Ω
I_{line}
21
13
12
1
11
V_{CC}
REFI
DOC
LN
VBG
V_o
17
IR
4
QR−
Z_L
100 µF
R_L
600 Ω
8
MIC+
5
QR+
7
MIC−
15
CURL
R4
100 kΩ
C4
100 pF
C1
100 µF
19
DTMF
TEA1065
6
GAR
C7 1 nF
5 to
140 mA
20
MUTE
2
GAS1
10 µF
18
PD
10
DPI
R7
68 kΩ
V_i
14
VSI
3
GAS2
C6
100 pF
V_{EE}
REG
AGC
STAB
SLPE
16
22
23
9
24
C3
4.7
µF
R6
118
kΩ
R5
3.6
kΩ
R9
20 Ω
MBA559

Fig.17 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as $G_v = 20 \text{ Log }|V_o/V_i|$.

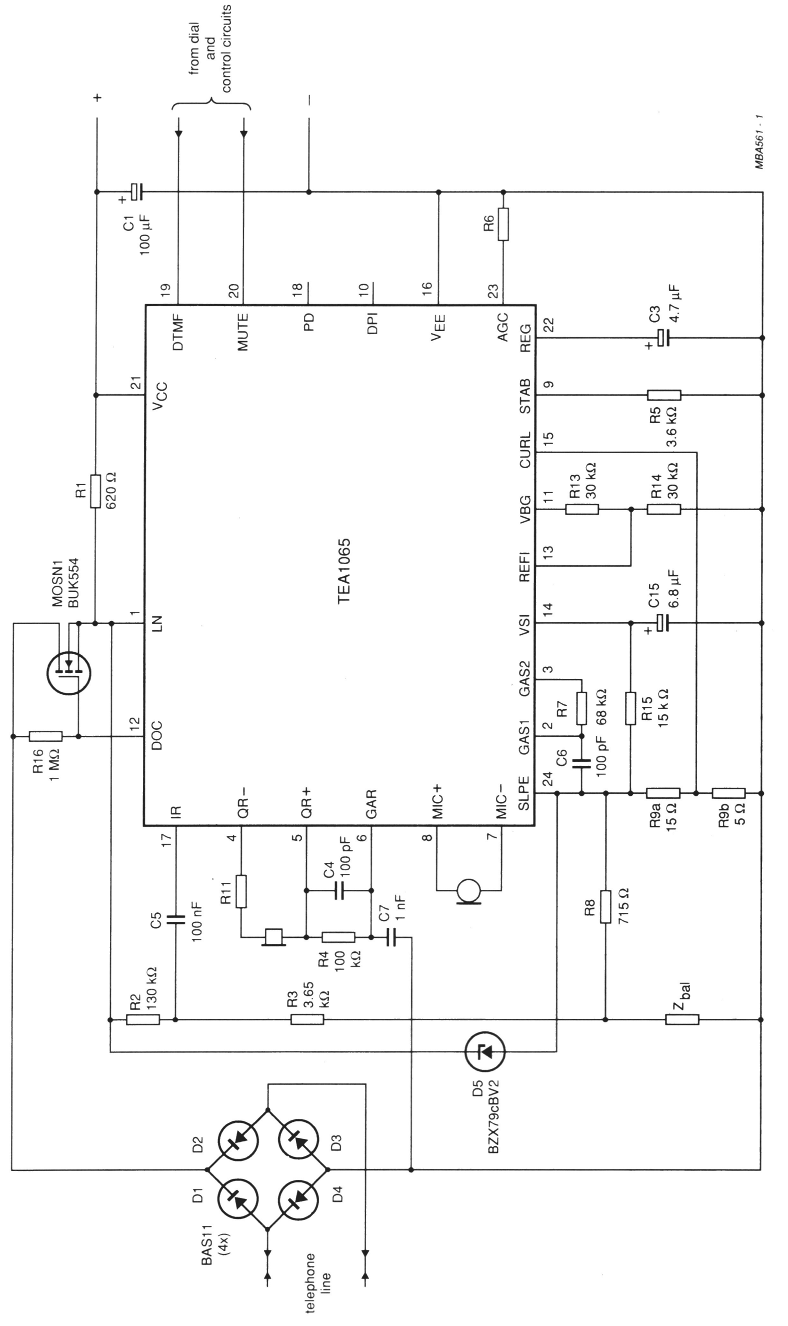

+
from dial
and
control circuits
−
MBA561 - 1
C1
100 µF
R6
19
20
18
10
16
23
DTMF
MUTE
PD
DPI
VEE
AGC
REG
22
C3
4.7 µF
STAB
9
R5
3.6 kΩ
CURL
15
VBG
11
R13
30 kΩ
R14
30 kΩ
REFI
13
VSI
14
C15
6.8 µF
GAS2
3
R7
68 kΩ
GAS1
2
C6
100 pF
R15
15 k Ω
SLPE
24
R9a
15 Ω
R9b
5 Ω
21
VCC
R1
620 Ω
MOSN1
BUK554
1
LN
TEA1065
12
DOC
R16
1 MΩ
IR
17
QR−
4
QR+
5
GAR
6
MIC+
8
MIC−
7
C4
100 pF
R11
C5
100 nF
R4
100
kΩ
C7
1 nF
R8
715 Ω
R2
130 kΩ
R3
3.65
kΩ
Zbal
D5
BZX79cBV2
D1
D2
D3
D4
BAS11
(4x)
telephone
line

Fig.18 Typical application of the TEA1065, with a piezoelectric earpiece and DTMF dialling.

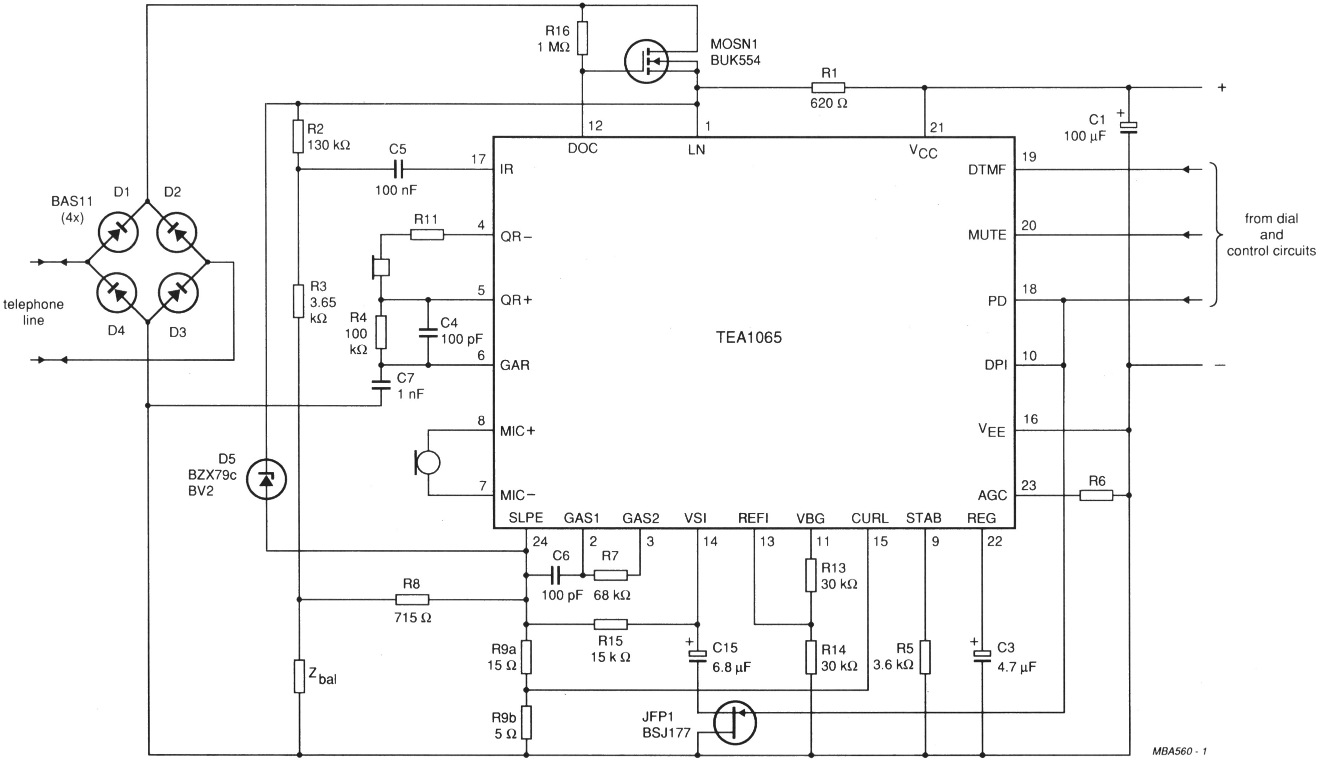

R16
1 MΩ
MOSN1
BUK554
R1
620 Ω
+
C1
100 µF
R2
130 kΩ
C5
100 nF
12
DOC
1
LN
21
VCC
19
DTMF
20
MUTE
18
PD
10
DPI
16
VEE
23
AGC
R6
from dial
and
control circuits
−
BAS11
(4x)
D1
D2
D3
D4
telephone
line
17
IR
R11
4
QR−
5
QR+
R3
3.65
kΩ
R4
100
kΩ
C4
100 pF
6
GAR
C7
1 nF
8
MIC+
7
MIC−
TEA1065
D5
BZX79c
BV2
SLPE
GAS1
GAS2
VSI
REFI
VBG
CURL
STAB
REG
24
2
3
14
13
11
15
9
22
C6
100 pF
R7
68 kΩ
R8
715 Ω
R13
30 kΩ
R15
15 k Ω
C15
6.8 µF
R14
30 kΩ
R5
3.6 kΩ
C3
4.7 µF
R9a
15 Ω
R9b
5 Ω
Zbal
JFP1
BSJ177
MBA560 - 1

Fig.19 Typical application of the TEA1065, with a piezoelectric earpiece and pulse dialling. DTMF dialling requires a different protection arrangement.

Versatile telephone transmission circuit with dialler interface

TEA1066T

FEATURES

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- Dual-tone multi-frequency (DTMF) signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1066T is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. The circuit performs electronic switching between dialling and speech.

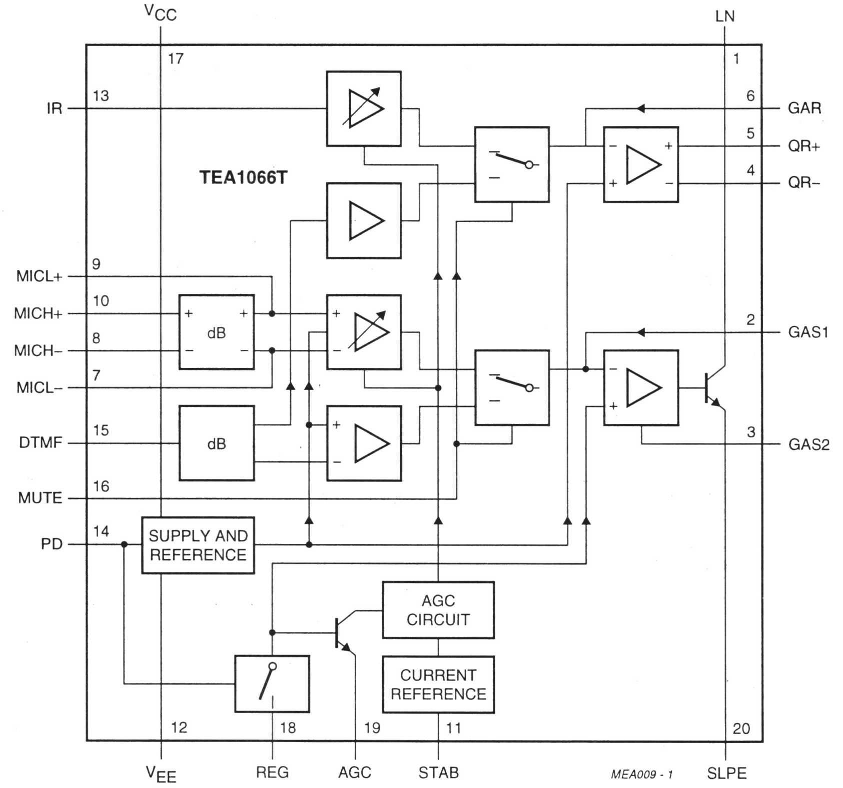
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.25	4.45	4.65	V
I_{line}	line current	normal operation	10	–	140	mA
I_{CC}	internal supply current	power down input LOW	–	0.96	1.3	mA
		power down input HIGH	–	55	82	μA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH; I_p = 1.2 mA	2.8	3.05	–	V
		I_{line} = 15 mA; MUTE input HIGH; I_p = 1.7 mA	2.5	–	–	V
G_v	voltage gain range for microphone amplifier					
	low impedance inputs (pins 7 and 9)		44	–	60	dB
	high impedance inputs (pins 8 and 10)		30	–	46	dB
	receiving amplifier		17	–	39	dB
T_{amb}	operating ambient temperature		–25	–	+75	°C
Line loss compensation						
ΔG_v	gain control		5.5	5.9	6.3	dB
V_{exch}	exchange supply voltage		24	–	60	V
R_{exch}	exchange feeding bridge resistance		400	–	1000	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1066T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM


VCC
LN
17
1
IR
13
6
GAR
5
QR+
4
QR−
TEA1066T
MICL+
9
MICH+
10
dB
MICH−
8
MICL−
7
2
GAS1
DTMF
15
dB
3
GAS2
MUTE
16
PD
14
SUPPLY AND REFERENCE
AGC CIRCUIT
CURRENT REFERENCE
12
18
19
11
20
VEE
REG
AGC
STAB
MEA009 - 1
SLPE

The blocks marked 'dB' are attenuators.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment transmitting amplifier
GAS2	3	gain adjustment transmitting amplifier
QR−	4	inverting output receiving amplifier
QR+	5	non-inverting output receiving amplifier
GAR	6	gain adjustment receiving amplifier
MICL−	7	inverting microphone input, low impedance
MICH−	8	inverting microphone input, high impedance
MICL+	9	non-inverting microphone input, low impedance
MICH+	10	non-inverting microphone input, high impedance
STAB	11	current stabilizer
V_{EE}	12	negative line terminal
IR	13	receiving amplifier input
PD	14	power-down input
DTMF	15	dual-tone multi-frequency input
MUTE	16	mute input
V_{CC}	17	supply voltage decoupling
REG	18	voltage regulator decoupling
AGC	19	automatic gain control input
SLPE	20	slope (DC resistance) adjustment

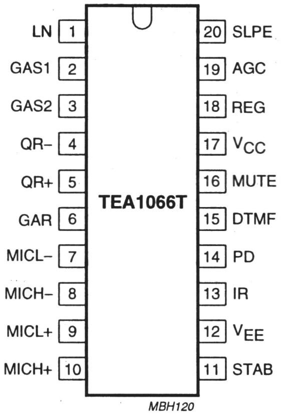


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Supplies: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1066T and its peripheral circuits is usually obtained from the telephone line. The TEA1066T develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the DC voltage on the subscriber set (see Fig.7).

If the line current I_{line} exceeds the current I_{CC} + 0.5 mA required by the circuit itself (approximately 1 mA) plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

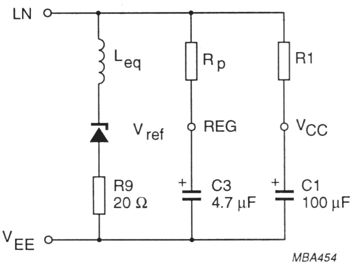
or

$$V_{LN} = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3}A - I_p) \times R9$$

where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}.

The preferred value for R9 is 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level and the maximum output swing on LN.

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range, the dynamic impedance is largely determined by R1 (see Fig.3).



R_p = 17.5 kΩ
$L_{eq} = C3 \times R9 \times R_p$

Fig.3 Equivalent impedance circuit.

The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor, connected between LN and REG (pins 1 and 18), will decrease the internal reference voltage; when connected between REG and SLPE (pins 18 and 20) it will increase the internal reference voltage.

Current I_p, available from V_{CC} for supplying peripheral circuits, depends on external components and on the line current. Figure 8 shows this current for $V_{CC} > 2.2$ V and > 3 V, this being the minimum supply voltage for most CMOS circuits, including voltage drop for an enable diode. If MUTE is LOW, the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MICL+, MICH+, MICL– and MICH– and amplification adjustment connections GAS1 and GAS2

The TEA1066T has symmetrical microphone inputs. The MICL+ and MICL– inputs are intended for low-sensitivity, low-impedance dynamic or magnetic microphones. The input impedance is 8.2 kΩ (2 × 4.1 kΩ) and its voltage gain is typically 52 dB. The MICH+ and MICH– inputs are intended for a piezoelectric microphone or an electret microphone with a built-in FET source follower. Its input impedance is 40.8 kΩ (2 × 20.4 kΩ) and its voltage gain is typical 38 dB.

The arrangements with the microphone types mentioned are shown in Fig.9.

The gain of the microphone amplifier in both types can be adjusted over a range of ±8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 × C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier; a LOW level or an open circuit has the reverse effect. Switching the mute input will cause negligible clicks at the earpiece outputs and on the line.

Dual-tone multi frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–.

These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig.10). Gain from IR to QR+ is typically 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces, which are suited for single-ended drive. By using both outputs (differential drive), the gain is increased by 6 dB and differential drive becomes possible. This feature can be used when the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak to RMS value is higher.

The receiving amplifier gain can be adjusted over a range of ±8 dB to suit the sensitivity of the transducer used. The gain is set by the external resistor R4 connected between GAR and QR+.

Two external capacitors, C4 = 100 pF and C7 = 10 × C4 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The 'cut-off' frequency corresponds with the time constant R4 × C4.

Automatic gain control input AGC

Automatic line loss compensation is obtained by connecting a resistor R6 between AGC and V_{EE}. This automatic gain control varies the microphone amplifier gain and the receiving amplifier gain in accordance with the DC line current.

The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.11 and Table 1). Different values of R6 give the same ratio of line currents for start and end of the control range.

If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typically 1 mA to typically 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig.14). Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1\,(R3 + [R8//Z_{bal}]) \qquad (1)$$

$$Z_{bal} / (Z_{bal} + R8) = Z_{line} / (Z_{line} + R1) \qquad (2)$$

If fixed values are chosen for R1, R2, R3, and R9, then condition (1) will always be fulfilled, provided that $|R8//Z_{bal}| < R3$. To obtain optimum side-tone suppression, condition (2) has to be fulfilled, resulting in:

$Z_{bal} = (R8/R1)\,Z_{line} = k \times Z_{line}$, where k is a scale factor: k = (R8/R1).

Scale factor k (dependent on the value of R8) must be chosen to meet the following criteria:

1. Compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
2. $|Z_{bal}//R8| << R3$
3. $|Z_{bal} + R8| >> R9$.

In practice, Z_{line} varies greatly with line length and cable type; consequently, an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

Example: The balanced line impedance $|Z_{bal}|$ at which the optimum suppression is preset can be calculated by:

Assume Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km). When k = 0.64, then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-side-tone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier.

The attenuation is almost constant over the whole audio frequency range. Figure 5 shows a conventional Wheatstone bridge anti-side-tone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

The anti-side-tone network as used in the standard application (see Fig.13) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.

Instead of the previously-described special TEA1066 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side-tone circuit. Both bridge types can be used with either a resistive set impedance or a complex set impedance.

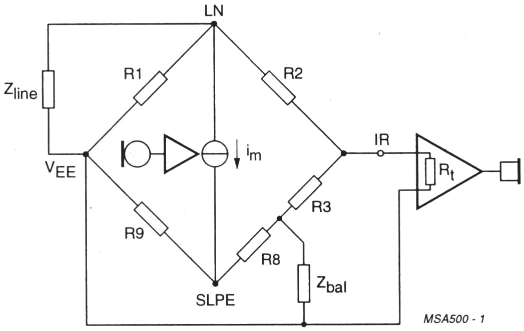


Fig.4 Equivalent circuit of TEA1060 family anti-side-tone bridge.

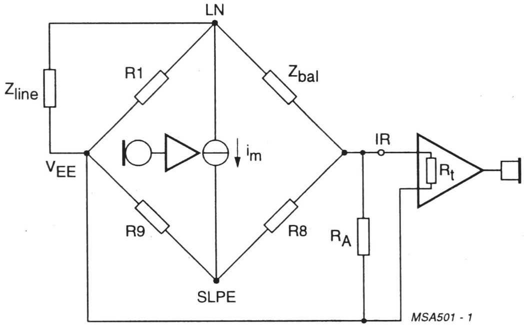


Fig.5 Equivalent circuit of an anti-side-tone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

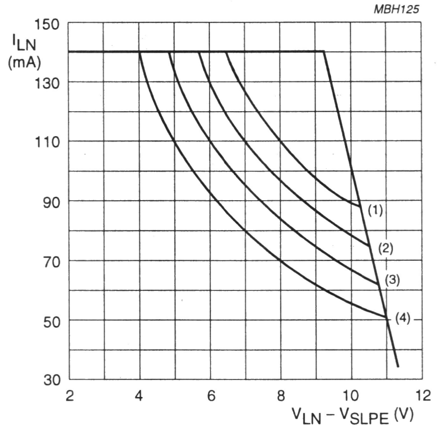
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; (Fig.10)	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1	–	140	mA
V_n	voltage on any other pin		$V_{EE} - 0.7$	$V_{CC} + 0.7$	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2	–	555	mW
T_{stg}	IC storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+75	°C
T_j	junction temperature		–	125	°C

Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Fig.6).
2. Calculated for the maximum ambient temperature specified, T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air mounted on glass epoxy board 41 × 19 × 1.5 mm	90	K/W



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.6 Safe operating area.

CHARACTERISTICS

I_{line} = 10 to 100 mA; V_{EE} = 0 V; f = 800 Hz; R9 = 20 Ω; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: LN and V_{CC} (pins 1 and 17)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.25	4.45	4.65	V
		I_{line} = 100 mA	5.40	6.10	6.70	V
		I_{line} = 140 mA	–	–	7.50	V
$\Delta V_{LN}/\Delta T$	voltage drop variation with temperature	I_{line} = 15 mA	–4	–2	0	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} = R1-18 = 68 kΩ	3.50	3.80	4.05	V
		I_{line} = 15 mA; R_{VA} = R18-20 = 39 kΩ	4.70	5	5.30	V
I_{CC}	supply current	PD = LOW; V_{CC} = 2.8 V	–	0.96	1.30	mA
		PD = HIGH; V_{CC} = 2.8 V	–	55	82	µA
V_{CC}	supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH; I_p = 0 mA	3.50	3.75	–	V
		I_{line} = 15 mA; MUTE = HIGH; I_p = 1.2 mA	2.80	3.05	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone inputs MICL+ and MICL–; MICH+ and MICH–						
$\|Z_i\|$	input impedance					
	MICL+ (pin 9); MICL– (pin 7)		3.3	4.1	4.9	kΩ
	MICH+ (pin 10); MICH– (pin 8)		16.5	20.4	24.5	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 Ω				
	MICL+/MICL– to LN		51	52	53	dB
	MICH+/MICH– to LN		37	38	39	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 800 Hz	–	±0.2	–	dB
Dual-tone multi-frequency input DTMF (pin 15)						
$\|Z_i\|$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7= 68 kΩ	24.5	25.5	26.5	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C	–	±0.2	–	dB
Gain adjustment connections GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	gain variation with R7, transmitting amplifier		–8	–	+8	dB
Transmitting amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA; THD = 2%	1.9	2.3	–	V
		I_{line} = 15 mA; THD = 10%	–	2.6	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; microphone inputs open; psophometrically weighted (P53 curve)	–	–70	–	dBmp
Receiving amplifier input IR (pin 13)						
$\|Z_i\|$	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR+ and QR– (pins 5 and 4)						
$\|Z_o\|$	output impedance	single-ended	–	4	–	Ω
G_v	voltage gain from IR to QR+ or QR–	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; R_L = 300 Ω	24	25	26	dB
		differential; R_L = 600 Ω	30	31	32	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C	–	±0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(rms)}$	output voltage (RMS value)	sine-wave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ				
		single-ended; R_L = 150 Ω	0.30	0.38	–	V
		single-ended; R_L = 450 Ω	0.40	0.52	–	V
		differential; C_L = 47 nF; R_{series} = 100 Ω; f = 3400 Hz	0.80	1.0	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; pin 13 (IR) open; psophometrically weighted (P53 curve)				
		single-ended; R_L = 300 Ω	–	50	–	μV
		differential; R_L = 600 Ω	–	100	–	μV
Gain adjustment GAR (pin 6)						
ΔG_v	gain variation with R4 connected between pin 6 and pin 5 receiving amplifier		–8	–	+8	dB
MUTE input (pin 16)						
V_{IH}	HIGH level input voltage		1.50	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{MUTE}	input current		–	5	10	μA
ΔG_v	voltage gain reduction between MICL+ (pin 9) and MICL– (pin 7) to LN (pin 1)	MUTE = HIGH	–	70	–	dB
G_v	voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	–21	–19	–17	dB
Power-down input PD (pin 14)						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{PD}	input current in power-down condition		–	5	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic gain control input AGC (pin 19)						
ΔG_v	gain control range from IR to QR+/QR− and from MIC+/MIC− to LN	I_{line} = 70 mA; R6 = 110 kΩ between AGC and V_{EE}	−5.5	−5.9	−6.3	dB
$I_{line(H)}$	highest line current for maximum gain	R6 = 110 kΩ between AGC and V_{EE}	−	23	−	mA
$I_{line(L)}$	lowest line current for minimum gain	R6 = 110 kΩ between AGC and V_{EE}	−	61	−	mA
ΔG_v	voltage gain variation	between I_{line} = 15 mA and I_{line} = 35 mA; R6 = 110 kΩ between AGC and V_{EE}	−1.0	−1.5	−2.0	dB

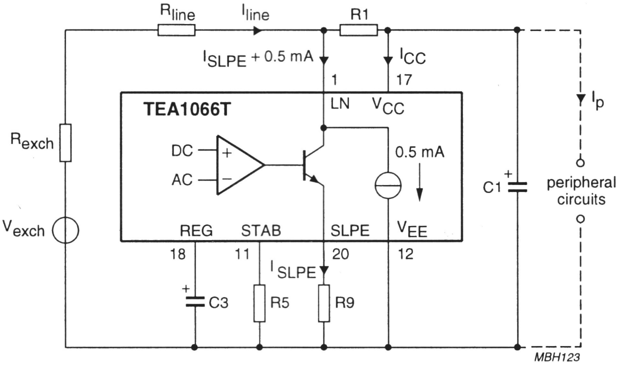
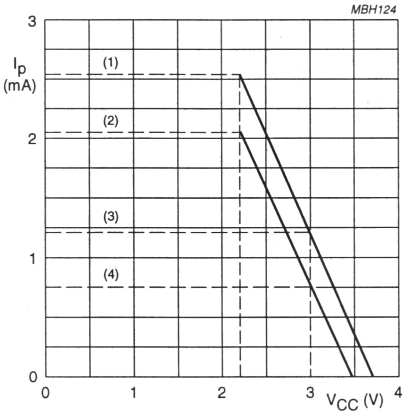

R_{line}
I_{line}
R1
I_{SLPE} + 0.5 mA
I_{CC}
1
17
TEA1066T
LN
V_{CC}
DC
AC
+
−
0.5 mA
R_{exch}
V_{exch}
C1
I_p
peripheral circuits
REG
STAB
SLPE
V_{EE}
18
11
20
12
I_{SLPE}
C3
R5
R9
MBH123

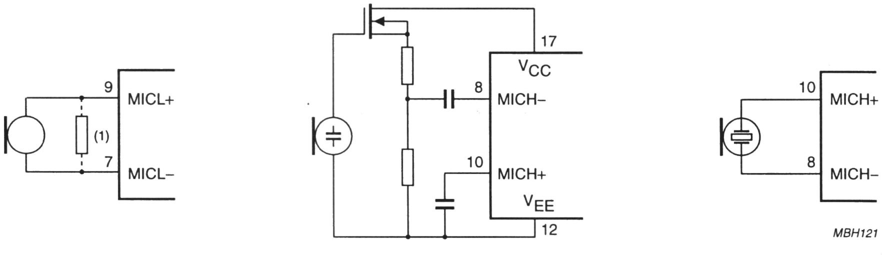
Fig.7 Supply arrangement.



Curves (1) and (3) are valid when the receiving amplifier is not driven or when MUTE = HIGH. Curves (2) and (4) are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical). I_{line} = 15 mA; V_{LN} = 4.45 V; R1 = 620 Ω and R9 = 20 Ω.

(1) I_p = 2.55 mA.
(2) I_p = 2.1 mA.
(3) I_p = 1.2 mA.
(4) I_p = 0.75 mA.

Fig.8 Typical current I_p available from V_{CC} for external (peripheral) circuitry with V_{CC} > 2.2 V and V_{CC} > 3 V.



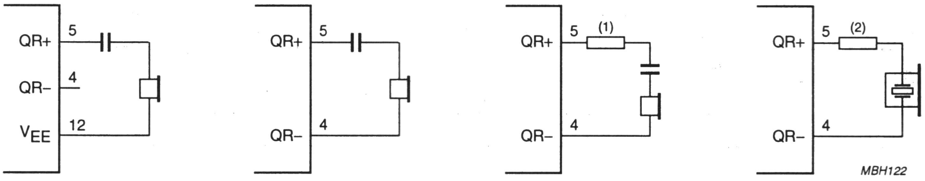
a. Magnetic or dynamic microphone.

b. Electret microphone.

c. piezoelectric microphone.

(1) May be connected to lower the terminating impedance.

Fig.9 Alternative microphone arrangements.



a. Dynamic earpiece with less than 450 Ω impedance.

b. Dynamic earpiece with more than 450 Ω impedance.

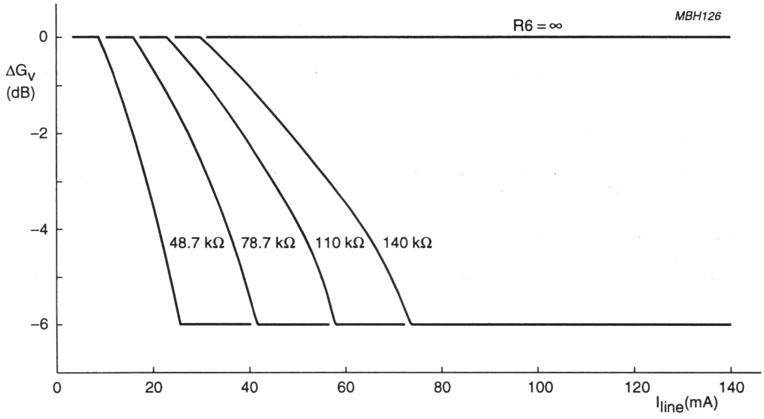
c. Magnetic earpiece with more than 450 Ω impedance.

d. piezoelectric earpiece.

(1) May be connected to prevent distortion (inductive load).

(2) Required to increase the phase margin (capacitive load).

Fig.10 Alternative receiver arrangements.

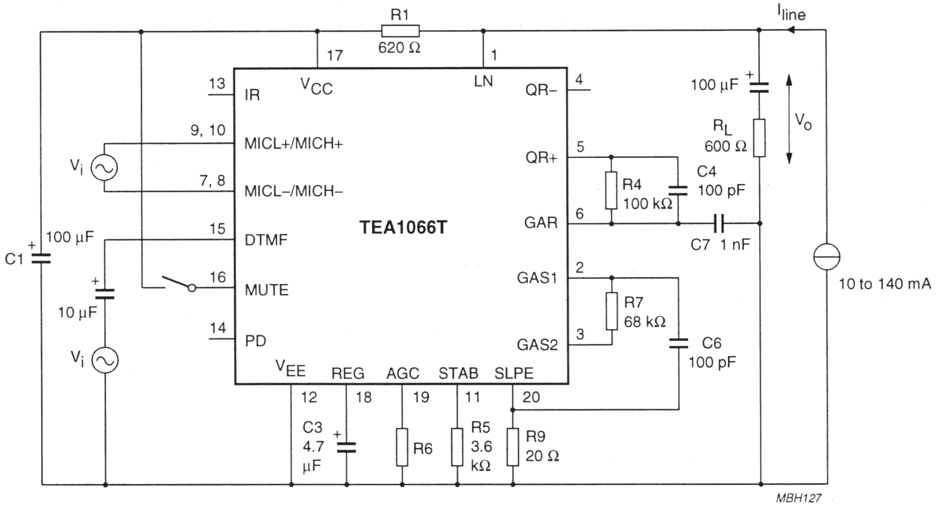


R9 = 20 Ω.

Fig.11 Variation of gain with line current, with R6 as a parameter.

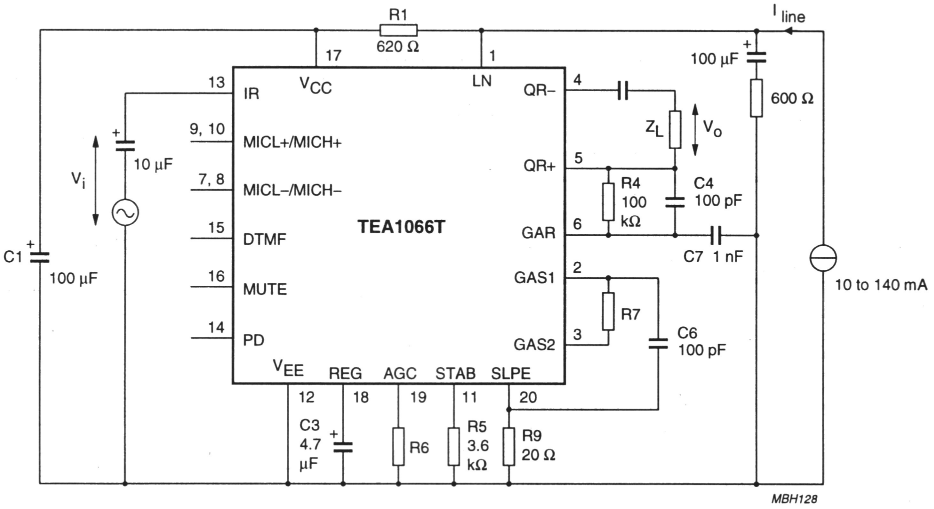
Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
24	61.9	48.7	X	X
36	100	78.7	68	60.4
48	140	110	93.1	82
60	X	X	120	102


R1
620 Ω
17
1
I_{line}
13
IR
V_{CC}
LN
QR−
4
100 µF
R_L
600 Ω
V_o
9, 10
MICL+/MICH+
QR+
5
V_i
7, 8
MICL−/MICH−
R4
100 kΩ
C4
100 pF
C1
100 µF
15
DTMF
TEA1066T
GAR
6
C7 1 nF
10 µF
16
MUTE
GAS1
2
10 to 140 mA
R7
68 kΩ
V_i
14
PD
GAS2
3
C6
100 pF
V_{EE}
REG
AGC
STAB
SLPE
12
18
19
11
20
C3
4.7
µF
R6
R5
3.6
kΩ
R9
20 Ω
MBH127

Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MICL+, MICL− or MICH+ and MICH−, the MUTE input should be LOW or open; for measuring the DTMF input, MUTE should be HIGH. Inputs not under test should be open.

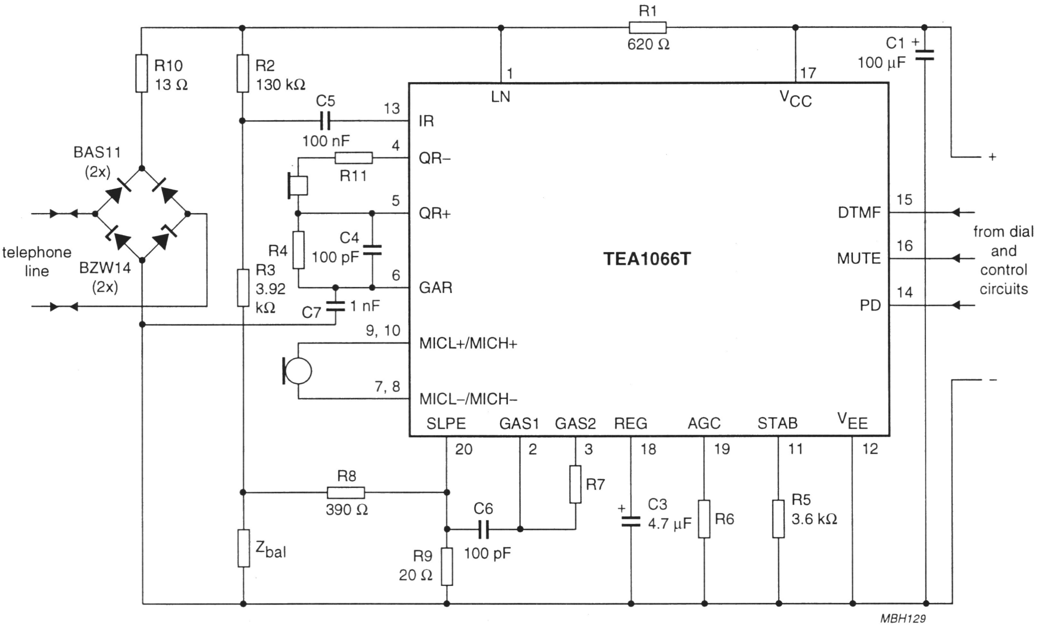
Fig.12 Test circuit for defining voltage gain of MICL+, MICL−, MICH+ and MICH− DTMF inputs.


R1
620 Ω
17
1
13
IR
VCC
LN
QR−
4
9, 10
MICL+/MICH+
7, 8
MICL−/MICH−
15
DTMF
16
MUTE
14
PD
TEA1066T
QR+
5
GAR
6
GAS1
2
GAS2
3
VEE
REG
AGC
STAB
SLPE
12
18
19
11
20
C3
4.7
µF
R6
R5
3.6
kΩ
R9
20 Ω
C1
100 µF
10 µF
Vi
ZL
Vo
R4
100
kΩ
C4
100 pF
C7 1 nF
R7
C6
100 pF
I line
100 µF
600 Ω
10 to 140 mA
MBH128

Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$.

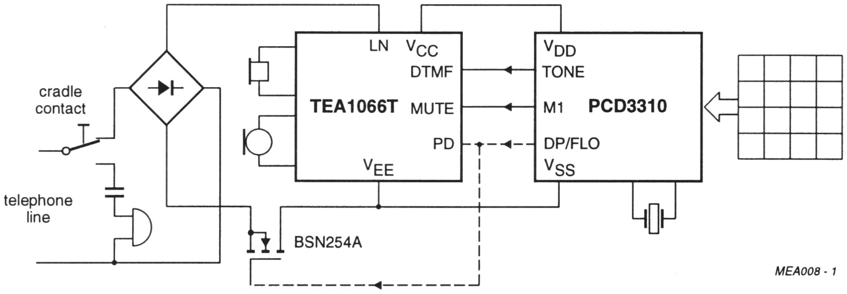
Fig.13 Test circuit for defining voltage gain of the receiving amplifier.

APPLICATION INFORMATION


R1
620 Ω
C1
100 μF
R10
13 Ω
R2
130 kΩ
C5
100 nF
R11
BAS11
(2x)
telephone line
BZW14
(2x)
R4
R3
3.92 kΩ
C4
100 pF
C7
1 nF
13
4
5
6
9, 10
7, 8
1
17
LN
VCC
IR
QR−
QR+
GAR
MICL+/MICH+
MICL−/MICH−
TEA1066T
DTMF
MUTE
PD
15
16
14
from dial and control circuits
+
−
SLPE
GAS1
GAS2
REG
AGC
STAB
VEE
20
2
3
18
19
11
12
R8
390 Ω
C6
100 pF
R7
C3
4.7 μF
R6
R5
3.6 kΩ
Zbal
R9
20 Ω
MBH129

Typical application of the TEA1066, shown with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

Fig.14 Application diagram.


cradle contact
telephone line
LN
VCC
DTMF
TEA1066T
MUTE
PD
VEE
VDD
TONE
M1
PCD3310
DP/FLO
VSS
BSN254A
MEA008 - 1

The dashed lines show an optional flash (register recall by timed loop break).

Fig.15 DTMF pulse set with CMOS PCD3310 dialling circuit.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to a DC line voltage of 1.6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

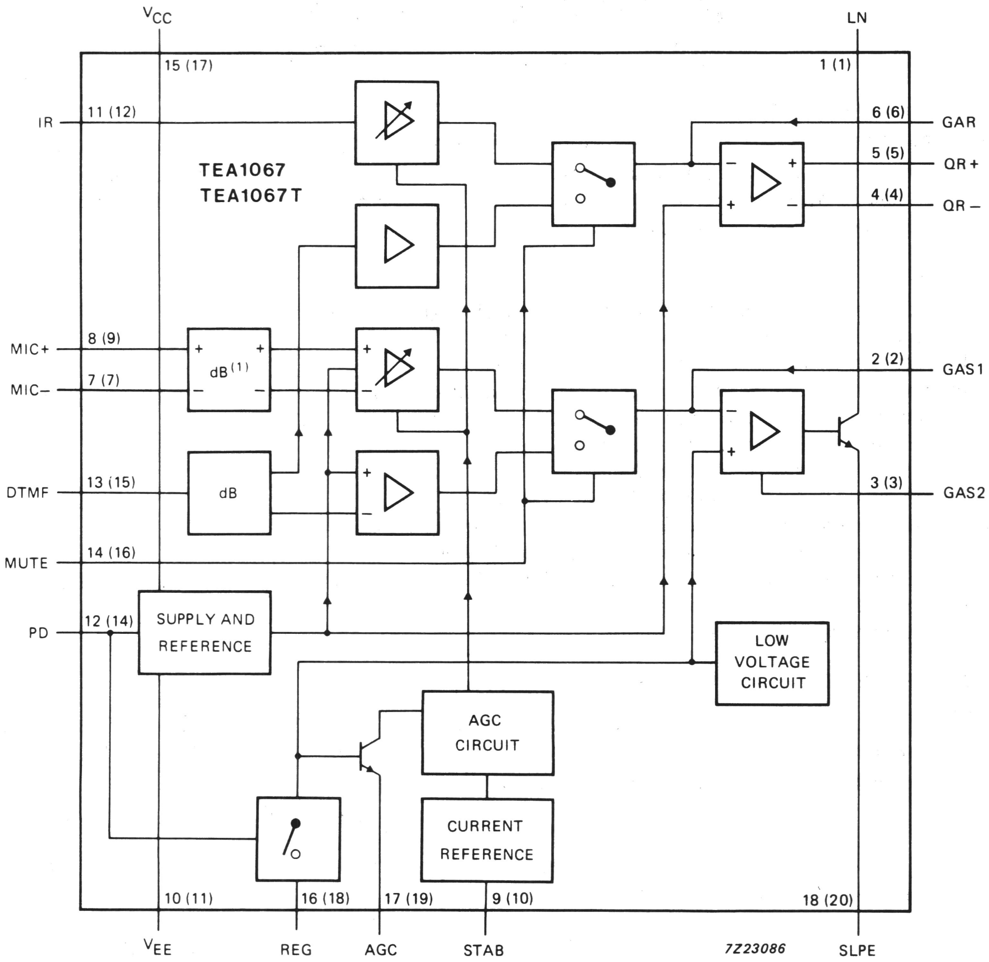
- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
Line current operating range	normal operation					
	TEA1067	I_{line}	11	–	140	mA
	TEA1067T	I_{line}	11	–	140	mA
	with reduced performance	I_{line}	1	–	11	mA
Internal supply current	power down					
	input LOW	I_{CC}	–	1	1.35	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; I_p = 1.4 mA; mute input HIGH	V_{CC}	2.2	2.4	–	V
	I_{line} = 15 mA; I_p = 0.9 mA; mute input HIGH	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	36	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1067: 18-lead DIL; plastic (SOT102).
TEA1067T: 20-lead mini-pack; plastic (SO20; SOT163A).


VCC
LN
15 (17)
1 (1)
IR
11 (12)
6 (6)
GAR
TEA1067
TEA1067T
5 (5)
QR +
4 (4)
QR –
MIC+
8 (9)
MIC–
7 (7)
dB (1)
2 (2)
GAS1
DTMF
13 (15)
dB
3 (3)
GAS2
MUTE
14 (16)
PD
12 (14)
SUPPLY AND
REFERENCE
LOW
VOLTAGE
CIRCUIT
AGC
CIRCUIT
CURRENT
REFERENCE
10 (11)
16 (18)
17 (19)
9 (10)
18 (20)
VEE
REG
AGC
STAB
7Z23086
SLPE

Figures in parenthesis refer to TEA1067T.

Fig. 1 Block diagram.

PINNING

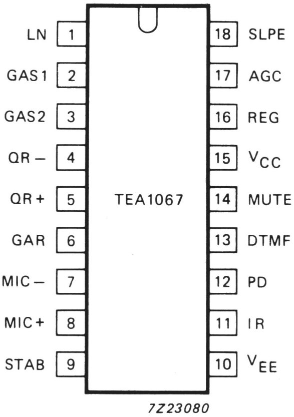

LN 1
GAS1 2
GAS2 3
QR – 4
QR + 5
GAR 6
MIC – 7
MIC + 8
STAB 9
18 SLPE
17 AGC
16 REG
15 V_{CC}
14 MUTE
13 DTMF
12 PD
11 IR
10 V_{EE}
TEA1067
7Z23080

Fig. 2 (a) Pinning diagram for TEA1067 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

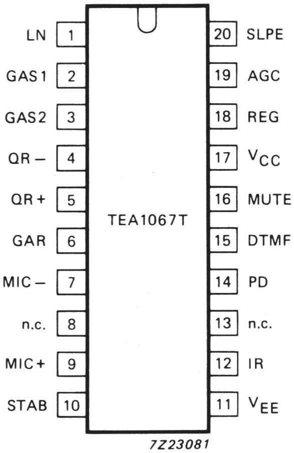

LN 1
GAS1 2
GAS2 3
QR – 4
QR + 5
GAR 6
MIC – 7
n.c. 8
MIC + 9
STAB 10
20 SLPE
19 AGC
18 REG
17 V_{CC}
16 MUTE
15 DTMF
14 PD
13 n.c.
12 IR
11 V_{EE}
TEA1067T
7Z23081

Fig. 2 (b) Pinning diagram for TEA1067T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment, receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1067 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

The TEA1067 has an internal current stabilizer working at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 6). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

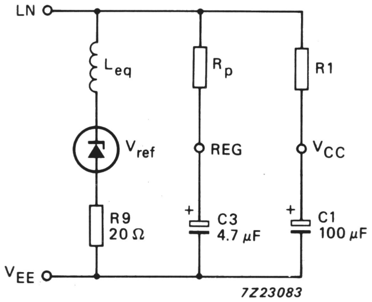
$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}\,A) - I_p] \times R9$$

Where V_{ref} is an internally generated temperature compensated reference voltage of 3.6 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5\text{ mA} + I_p$, the static behaviour of the circuit is that of a 3.6 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that the operation of more sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. With line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig. 9 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1, as shown in Fig. 16 (c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.



R_p = 16.2 kΩ
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC–) and gain adjustment pins (GAS1 and GAS2)

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 10.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the earpiece outputs and line. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier (IR, QR+, QR– and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR–). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 11). IR to QR + gain is typically 31 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single-ended drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω (high-impedance dynamic or piezoelectric types).

FUNCTIONAL DESCRIPTION (continued)

Receiving Amplifier (IR, QR+, QR− and GAR) (continued)

The receiving amplifier gain can be adjusted between 20 and 39 dB with single-ended drive and between 26 and 45 dB with differential drive, to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by substracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.
The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input (AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, R1//Z_{line}, R2, R3, R9 and Z_{bal}, (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in:

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor; $k = (R8/R1)$

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The line balance impedance (Z_{bal}) at which the optimum suppression is present can be calculated by: suppose Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

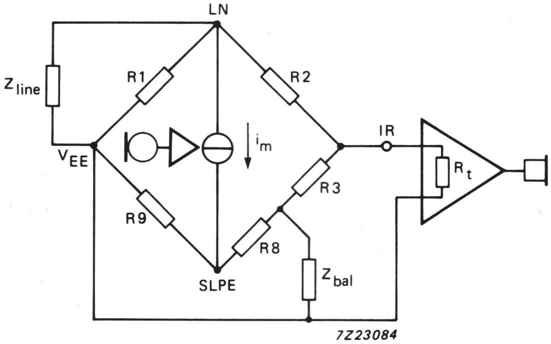


Fig. 4 Equivalent circuit of TEA1060 anti-sidetone bridge.

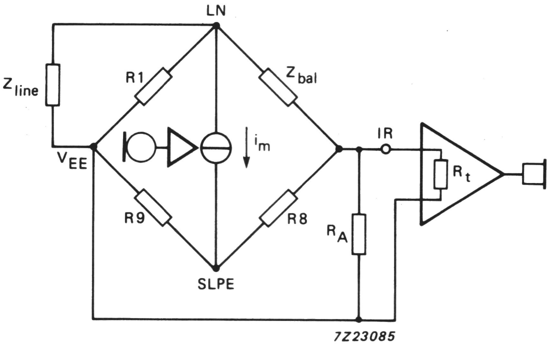


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 15)	V_{LN}	–	28	V
Line current TEA1067(1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1067T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i $-V_i$	– –	V_{CC} + 0.7 0.7	V V
Total power dissipation (2)	R9 = 20 Ω				
TEA1067		P_{tot}	–	769	mW
TEA1067T		P_{tot}	–	550	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

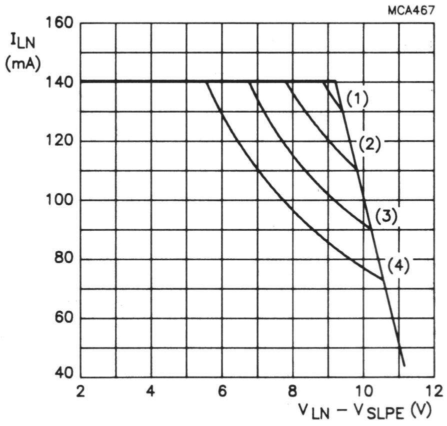
(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 6 and 7 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

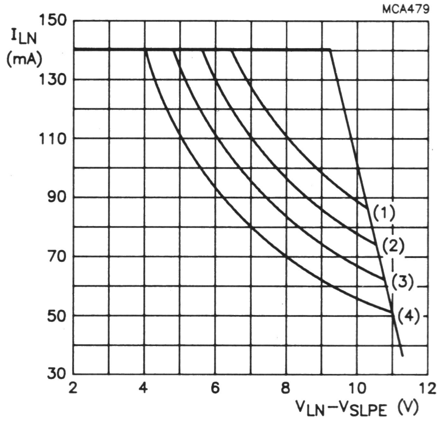
From junction to ambient in free air

TEA1067	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1067T mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig. 6 TEA1067 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig. 7 TEA1067T safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply; LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 1 mA	V_{LN}	–	1.6	–	V
	I_{line} = 4 mA	V_{LN}	1.75	2.0	2.25	V
	I_{line} = 7 mA	V_{LN}	2.25	2.8	3.35	V
	I_{line} = 11 mA	V_{LN}	3.55	3.8	4.05	V
	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
	I_{line} = 100 mA	V_{LN}	4.9	5.6	6.5	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	–3	–1	1	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.1	3.4	3.7	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.2	4.5	4.8	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	1.0	1.35	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.4 mA	V_{CC}	2.2	2.4	–	V
	I_p = 0 mA	V_{CC}	2.95	3.2	–	V
Microphone inputs MIC+ and MIC–						
Input impedance (differential) between MIC– and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC– or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC− (continued)						
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	± 0.2	+ 0.5	dB
Gain variation with temperature at −25 °C and + 75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	−	± 0.2	−	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C I_{line} = 50 mA	ΔG_{vT}	−	±0.2	−	dB
Gain adjustment GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	−8	−	0	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA THD = 2%	$V_{LN(rms)}$	−	1.9	−	V
	THD = 10%	$V_{LN(rms)}$	1.9	2.2	−	V
	I_{line} = 4 mA; THD = 10%	$V_{LN(rms)}$	−	0.8	−	V
	I_{line} = 7 mA; THD = 10%	$V_{LN(rms)}$	−	1.4	−	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−72	−	dBmp

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR−						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA R4 = 100 kΩ					
single-ended	R_L (from QR+ or QR−) = 300 Ω	G_v	30	31	32	dB
differential	R_L (from QR+ or QR−) = 600 Ω	G_v	36	37	38	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	−0.2	0	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Output voltage	sinewave drive I_{line} = 15 mA; I_p = 0 mA; THD = 2% R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.25	0.29	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.45	0.55	–	V

differential	f = 3400 Hz;
	series R = 100 Ω;
	C_L = 47 nF
		$V_{o(rms)}$	0.65	0.80	–	V

Output voltage	THD = 10%; RL = 150 Ω R4 = 100 kΩ					
	I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV

parameter	conditions	symbol	min.	typ.	max.	unit
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−11	–	+8	dB
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC– to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC						
Controlling the gain from IR to QR+/QR– and the gain from MIC+/MIC– to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	−1.0	−1.5	−2.0	dB

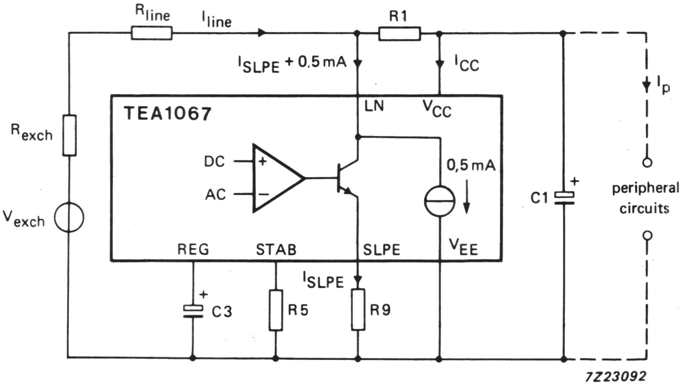
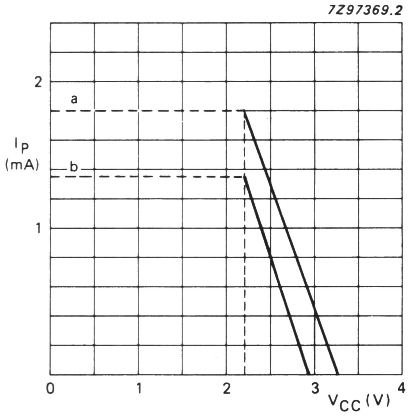

R_{line}
I_{line}
R1
I_{SLPE} + 0.5 mA
I_{CC}
I_p
TEA1067
LN
V_{CC}
R_{exch}
DC
AC
0,5 mA
V_{exch}
C1
peripheral circuits
REG
STAB
SLPE
V_{EE}
I_{SLPE}
C3
R5
R9
7Z23092

Fig. 8 Supply arrangement.



(a) I_p = 1.8 mA

(b) I_p = 1.35 mA

I_{line} = 15 mA at V_{LN} = 3.9 V

R1 = 620 Ω and R9 = 20 Ω.

Fig. 9 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical.
The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

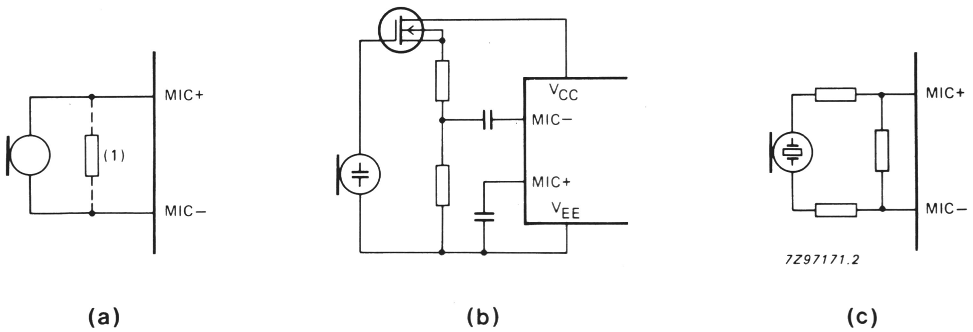

MIC+
MIC−
(1)
VCC
MIC−
MIC+
VEE
MIC+
MIC−
7Z97171.2
(a)
(b)
(c)

Fig. 10 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

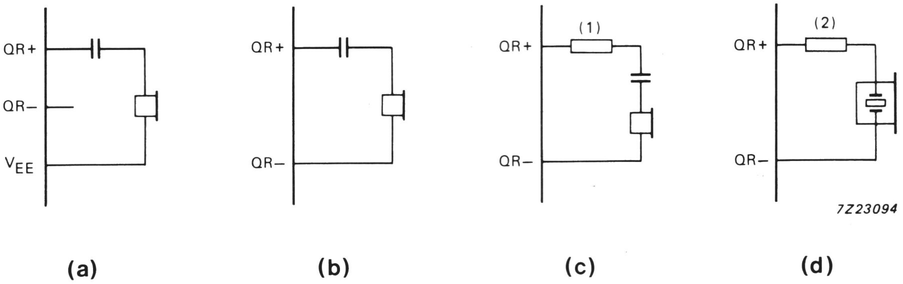

QR+
QR−
VEE
QR+
QR−
(1)
QR+
QR−
(2)
QR+
QR−
7Z23094
(a)
(b)
(c)
(d)

Fig. 11 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

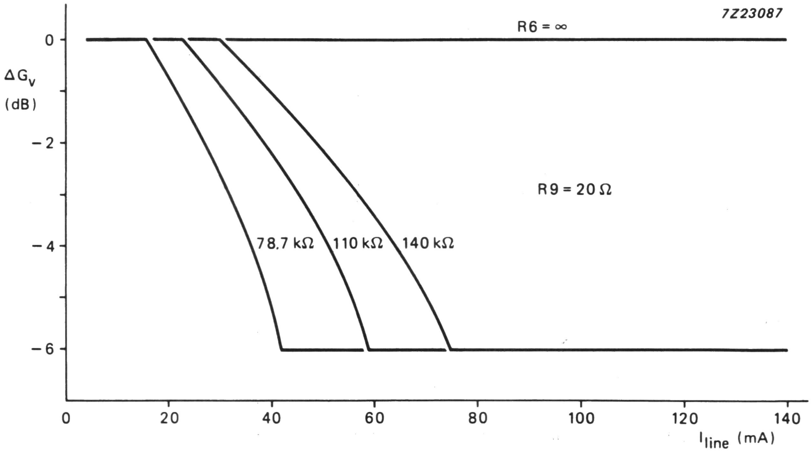


Fig. 12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102

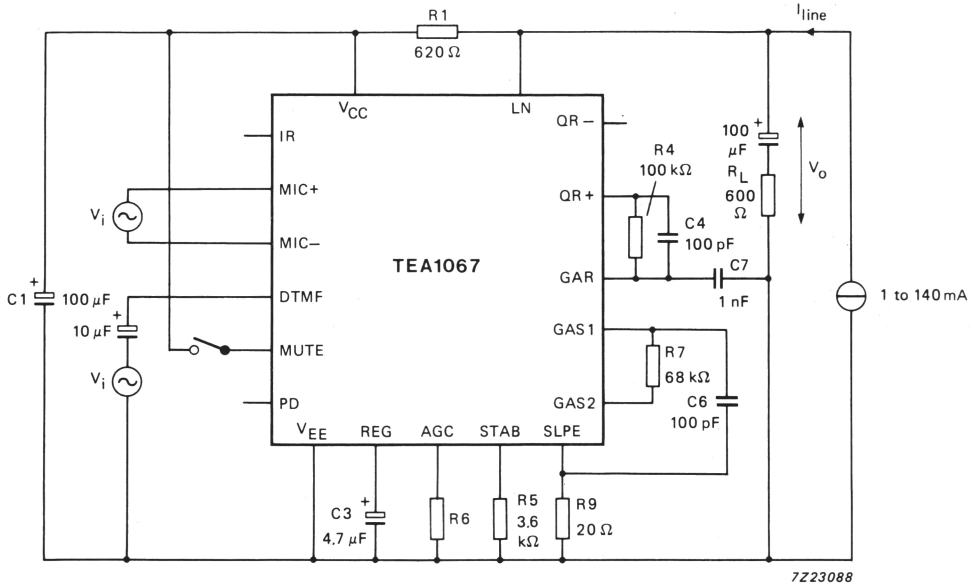

R1
620 Ω
I_{line}
V_{CC}
LN
QR –
IR
MIC+
MIC–
DTMF
MUTE
PD
V_{EE}
REG
AGC
STAB
SLPE
QR +
GAR
GAS 1
GAS2
TEA1067
V_i
V_i
C1
100 μF
10 μF
R4
100 kΩ
C4
100 pF
100 μF
R_L
600 Ω
V_o
C7
1 nF
R7
68 kΩ
C6
100 pF
1 to 140 mA
C3
4,7 μF
R6
R5
3,6 kΩ
R9
20 Ω
7Z23088

Fig. 13 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

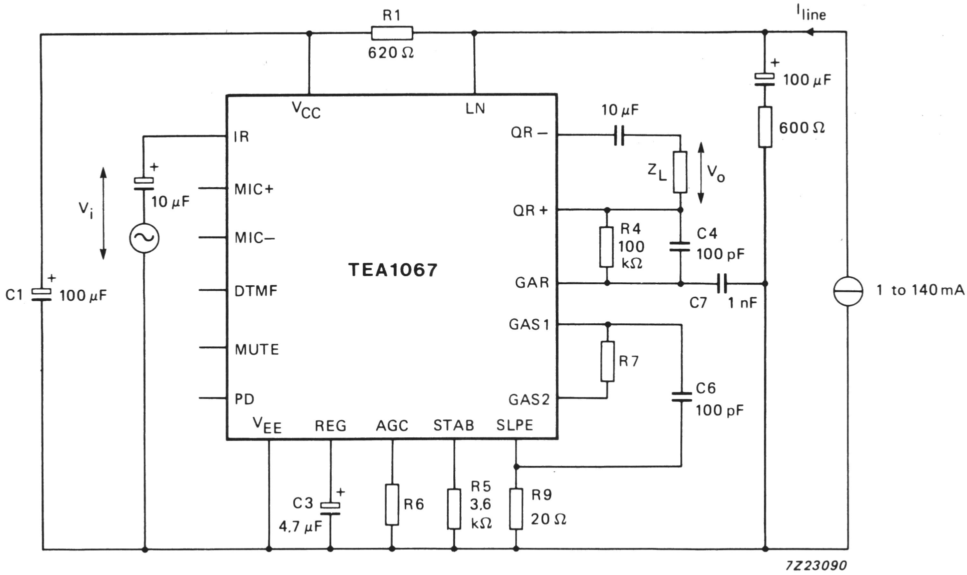

R1
620 Ω
I_{line}
V_{CC}
LN
QR –
IR
MIC+
MIC–
DTMF
MUTE
PD
V_{EE}
REG
AGC
STAB
SLPE
QR +
GAR
GAS 1
GAS2
TEA1067
V_i
10 μF
C1
100 μF
10 μF
Z_L
V_o
R4
100 kΩ
C4
100 pF
100 μF
600 Ω
C7
1 nF
R7
C6
100 pF
1 to 140 mA
C3
4,7 μF
R6
R5
3,6 kΩ
R9
20 Ω
7Z23090

Fig. 14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$.

APPLICATION INFORMATION

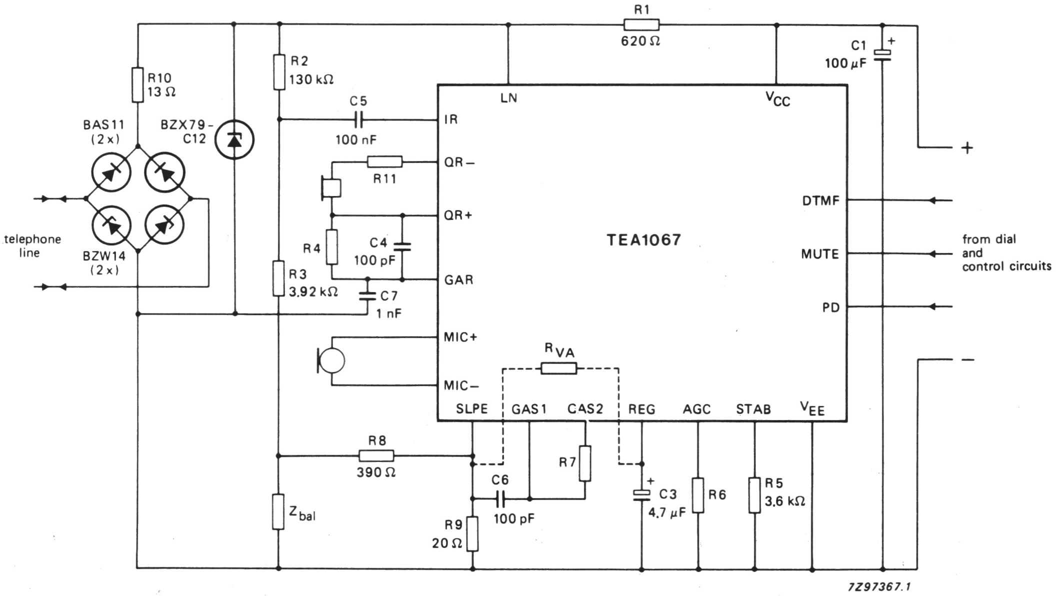

R1
620 Ω
C1
100 µF
R10
13 Ω
R2
130 kΩ
C5
100 nF
BAS11
(2×)
BZX79-
C12
LN
VCC
IR
QR−
R11
QR+
R4
C4
100 pF
TEA1067
telephone
line
BZW14
(2×)
R3
3.92 kΩ
C7
1 nF
GAR
MIC+
MIC−
RVA
SLPE
GAS1
GAS2
REG
AGC
STAB
VEE
DTMF
MUTE
PD
from dial
and
control circuits
+
−
R8
390 Ω
R7
C6
100 pF
C3
4.7 µF
R6
R5
3.6 kΩ
Zbal
R9
20 Ω
7Z97367.1

Fig. 15 Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).

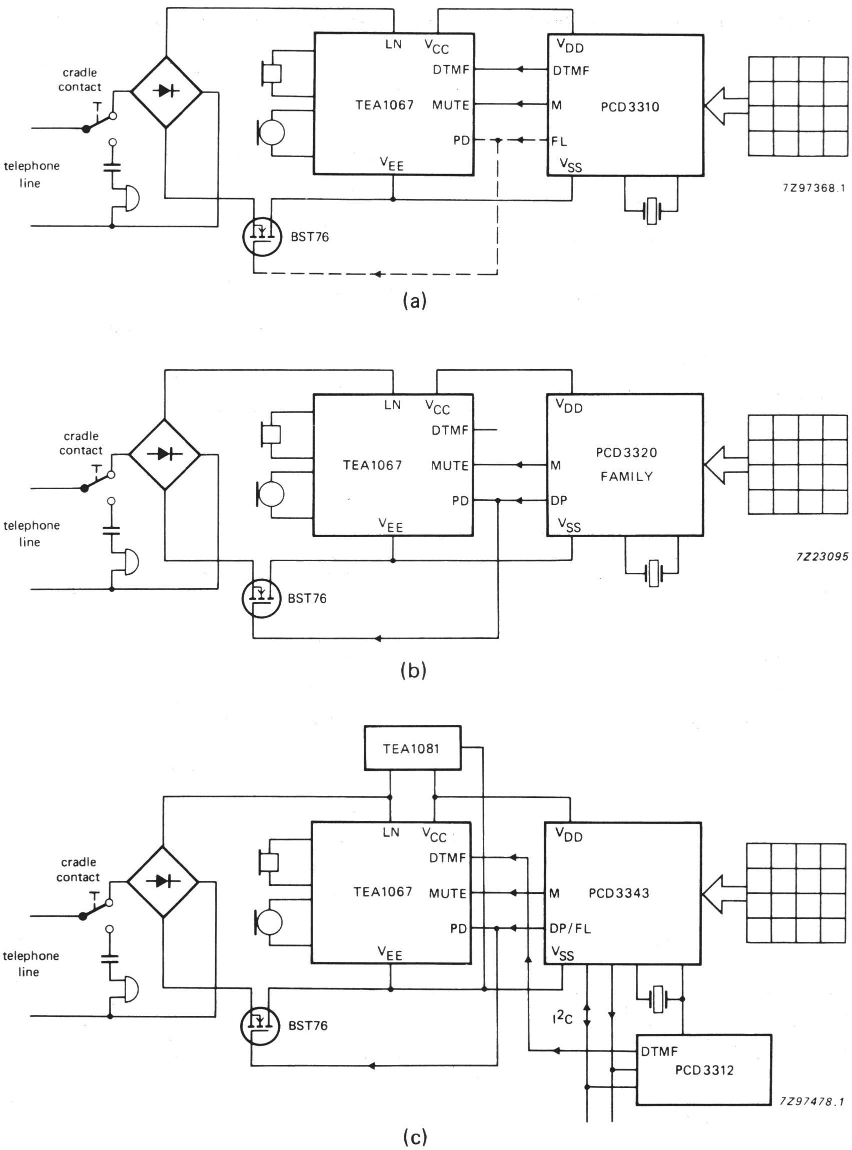

cradle contact
T
telephone line
LN
V_{CC}
DTMF
TEA1067
MUTE
PD
V_{EE}
BST76
V_{DD}
DTMF
M
PCD3310
FL
V_{SS}
7Z97368.1
(a)
cradle contact
T
telephone line
LN
V_{CC}
DTMF
TEA1067
MUTE
PD
V_{EE}
BST76
V_{DD}
PCD3320 FAMILY
M
DP
V_{SS}
7Z23095
(b)
TEA1081
cradle contact
T
telephone line
LN
V_{CC}
DTMF
TEA1067
MUTE
PD
V_{EE}
BST76
V_{DD}
M
PCD3343
DP/FL
V_{SS}
I^2C
DTMF
PCD3312
7Z97478.1
(c)

Fig. 16 Typical applications of the TEA1067 (simplified).

(a) DTMF-Pulse set with CMOS dialling circuit PCD3310.
The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

Versatile telephone transmission circuit with dialler interface

TEA1068

FEATURES

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- Dual-Tone Multi-Frequency (DTMF) signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current-dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech.

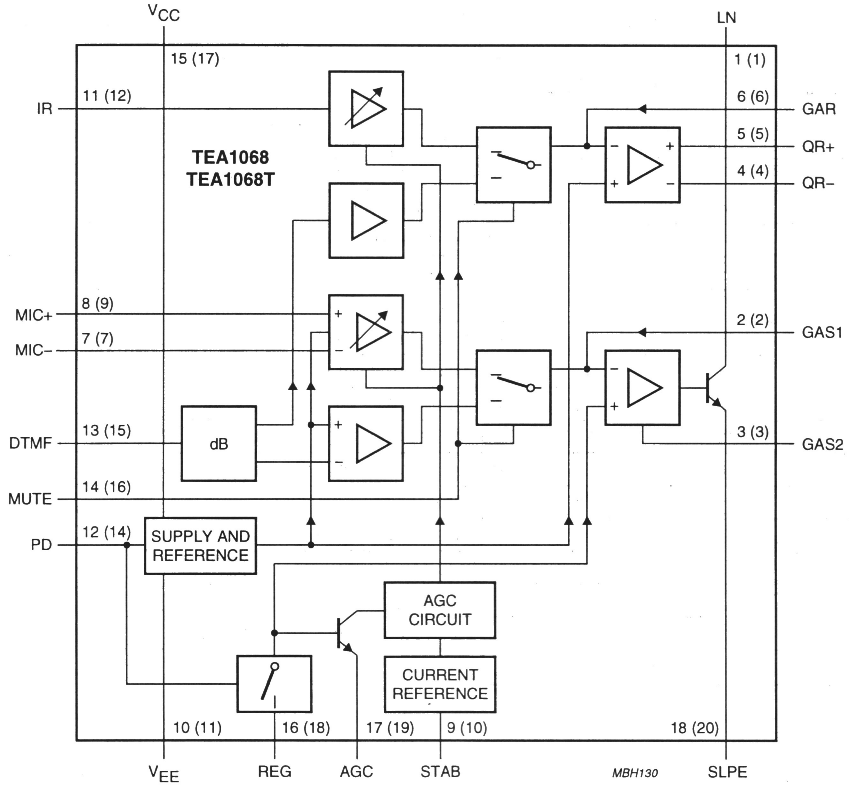
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.2	4.45	4.7	V
I_{line}	line current					
	TEA1068	normal operation	10	–	140	mA
	TEA1068T	normal operation	10	–	100	mA
I_{CC}	internal supply current	power down; input LOW	–	0.96	1.3	mA
		power down; input HIGH	–	55	82	µA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE = HIGH				
		I_p = 1.2 mA	2.8	3.05	–	V
		I_p = 1.7 mA	2.5	–	–	V
G_v	voltage gain					
	microphone amplifier		44	–	60	dB
	receiving amplifier		17	–	39	dB
ΔG_v	line loss compensation gain control range		5.5	5.9	6.3	dB
V_{exch}	exchange supply voltage		24	–	60	V
R_{exch}	exchange feeding bridge resistance range		0.4	–	1	kΩ
T_{amb}	ambient operating temperature		–25		+75	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1068	DIP18	plastic dual in-line package; 18 leads (300 mil)	SOT102-1
TEA1068T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM


VCC
15 (17)
LN
1 (1)
IR
11 (12)
6 (6)
GAR
5 (5)
QR+
4 (4)
QR−
TEA1068
TEA1068T
MIC+
8 (9)
MIC−
7 (7)
2 (2)
GAS1
DTMF
13 (15)
dB
3 (3)
GAS2
MUTE
14 (16)
PD
12 (14)
SUPPLY AND REFERENCE
AGC CIRCUIT
CURRENT REFERENCE
10 (11)
16 (18)
17 (19)
9 (10)
18 (20)
VEE
REG
AGC
STAB
MBH130
SLPE

The figures in parentheses refer to the TEA1068T.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TEA1068	TEA1068T	
LN	1	1	positive line terminal
GAS1	2	2	gain adjustment transmitting amplifier
GAS2	3	3	gain adjustment transmitting amplifier
QR−	4	4	inverting output receiving amplifier
QR+	5	5	non-inverting output receiving amplifier
GAR	6	6	gain adjustment receiving amplifier
MIC−	7	7	inverting microphone input
n.c.	–	8	not connected
MIC+	8	9	non-inverting microphone input
STAB	9	10	current stabilizer
V_{EE}	10	11	negative line terminal
IR	11	12	receiving amplifier input
n.c.	–	13	not connected
PD	12	14	power-down input
DTMF	13	15	dual-tone multi-frequency input
MUTE	14	16	mute input
V_{CC}	15	17	positive supply decoupling
REG	16	18	voltage regulator decoupling
AGC	17	19	automatic gain control input
SLPE	18	20	slope (DC resistance) adjustment

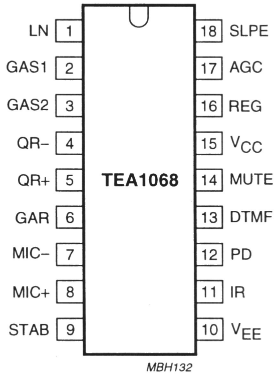

LN
1
GAS1
2
GAS2
3
QR−
4
QR+
5
GAR
6
MIC−
7
MIC+
8
STAB
9
TEA1068
18
SLPE
17
AGC
16
REG
15
V_{CC}
14
MUTE
13
DTMF
12
PD
11
IR
10
V_{EE}
MBH132

Fig.2 Pin configuration TEA1068.

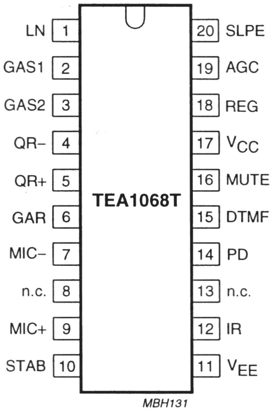

LN
1
GAS1
2
GAS2
3
QR−
4
QR+
5
GAR
6
MIC−
7
n.c.
8
MIC+
9
STAB
10
TEA1068T
20
SLPE
19
AGC
18
REG
17
V_{CC}
16
MUTE
15
DTMF
14
PD
13
n.c.
12
IR
11
V_{EE}
MBH131

Fig.3 Pin configuration TEA1068T.

FUNCTIONAL DESCRIPTION

Supplies: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1068 and its peripheral circuits is usually obtained from the telephone line. The TEA1068 develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits, e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE}; the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current flowing into the set is determined by the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

An internal current stabilizer is set by a resistor of 3.6 kΩ between the current stabilizer pin STAB and V_{EE} (see Fig.9).

If the line current I_{line} exceeds the current I_{CC} + 0.5 mA required by the circuit itself (approximately 1 mA) plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

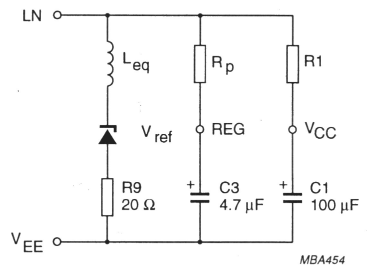
or

$$V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^3) - I_p] \times R9$$

where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level, the maximum output swing on LN and the DC characteristics (especially at lower voltages).

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range, the dynamic impedance is largely determined by R1 (see Fig.4).

The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor, connected between LN and REG, will decrease the internal reference voltage; when connected between REG and SLPE, it will increase the internal reference voltage. Current (I_p) available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Figure 10 shows this current for V_{CC} > 2.2 V and for V_{CC} > 3 V, this being the minimum supply voltage for most CMOS circuits, including voltage drop for an enable diode. If MUTE is LOW, the available current is further reduced when the receiving amplifier is driven.



R_p = 17.5 kΩ
L_{eq} = C3 × R9 × R_p

Fig.4 Equivalent impedance circuit.

Microphone inputs MIC+ and MIC− and gain adjustment pins GAS1 and GAS2

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ; see Fig.14). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used.

The arrangements with the microphone types mentioned are shown in Fig.11.

The gain of the microphone amplifier can be adjusted between 44 dB and 60 dB. The gain is proportional to the value of the external resistor R7 connected between GAS1 and GAS2. An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 × C6.

Mute input (MUTE)

A HIGH level at MUTE enables the DTMF input and inhibits the microphone and the receiving amplifier inputs.

A LOW level or an open circuit has the reverse effect. MUTE switching causes only negligible clicks at the earpiece outputs and on the line.

Dual-Tone Multi Frequency input (DTMF)

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the telephone earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–. These outputs may be used for single-ended or for differential drive depending on the sensitivity and type of earpiece used (see Fig.12). Gain from IR to QR+ is typically 25 dB (when R4 = 100 kΩ). This is sufficient for low-impedance magnetic or dynamic microphones, which are suited for single-ended drive. By using both outputs (differential drive), the gain is increased by 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak to RMS value is higher.

The receiving amplifier gain can be adjusted between 17 dB and 33 dB with single-ended drive and between 26 dB and 39 dB with differential drive to suit the sensitivity of the transducer used. The gain is set by the external resistor R4 connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by subtracting the anti-side-tone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 = 100 pF and C7 = 10 × C4 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The ‘cut-off’ frequency corresponds with the time constant R4 × C4.

Automatic Gain Control input AGC

Automatic line loss compensation is achieved by connecting a resistor R6 between AGC and V_{EE}. This automatic gain control varies the microphone amplifier gain and the receiving amplifier gain in accordance with the DC line current.

The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.13 and Table 1). Different values of R6 give the same ratio of line currents for start and end of the control range. If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-Down input (PD)

During pulse dialling or register recall (timed loop break), the telephone line is interrupted. During these interruptions, the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input, which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator, thus preventing discharge through LN. When PD is HIGH, the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required, PD may be left open-circuit.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3 and Z_{bal} (see Fig.14). Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1\,(R3 + [R8//Z_{bal}]) \qquad (1)$$

$$[Z_{bal} / (Z_{bal} + R8) = Z_{line} / (Z_{line} + R1)] \qquad (2)$$

If fixed values are chosen for R1, R2, R3 and R9, then condition (1) will always be fulfilled, provided that $|R8//Z_{bal}| << R3$. To obtain optimum side-tone suppression, condition (2) has to be fulfilled, resulting in:

$Z_{bal} = (R8/R1)\ Z_{line} = k \times Z_{line}$, where k is a scale factor: $k = (R8/R1)$.

Scale factor k (dependent on the value of R8) must be chosen to meet the following criteria:

1. Compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
2. $|Z_{bal}//R8| << R3$ to fulfil condition (1) and thus ensuring correct anti-side-tone bridge operation
3. $|Z_{bal} + R8| >> R9$ to avoid influencing the transmitter gain.

In practice, Z_{line} varies greatly with the line length and cable type; consequently, an average value has to be chosen for Z_{bal}, thus giving an optimum setting for short or long lines.

Example: the balanced line impedance (Z_{bal}) at which the optimum suppression is preset can be calculated by:

Assume Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km). When k = 0.64, then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-side-tone network for the TEA1060 family shown in Fig.5 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier.
The attenuation is almost constant over the whole audio frequency range.

Figure 6 shows a conventional Wheatstone bridge anti-side-tone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

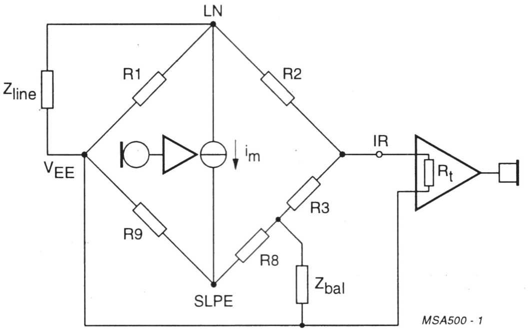


Fig.5 Equivalent circuit of TEA1060 family anti-side-tone bridge.

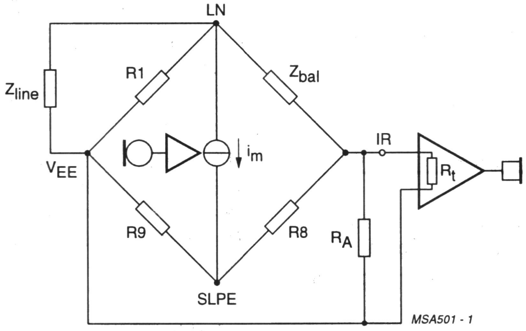


Fig.6 Equivalent circuit of an anti-side-tone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

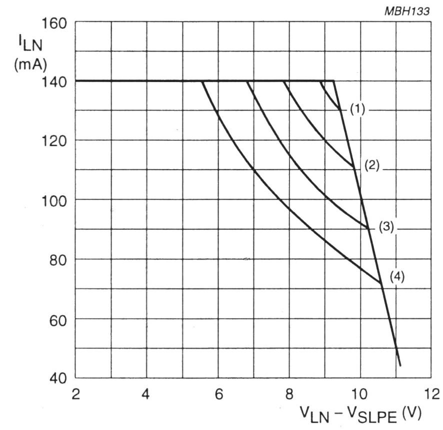
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; (Fig.15)	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1	–	140	mA
V_n	voltage on any other pin		V_{EE} – 0.7	V_{CC} + 0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1068		–	769	mW
	TEA1068T		–	555	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C
T_j	junction temperature		–	125	°C

Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 7 and 8 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

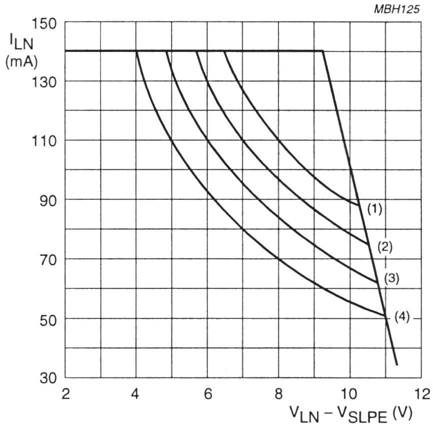
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1068	65	K/W
	TEA1068T	90	K/W



(1) T_{amb} = 45 °C; P_{tot} = 1231 mW.
(2) T_{amb} = 55 °C; P_{tot} = 1077 mW.
(3) T_{amb} = 65 °C; P_{tot} = 923 mW.
(4) T_{amb} = 75 °C; P_{tot} = 769 mW.

Fig.7 Safe operating area TEA1068.



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.8 Safe operating area TEA1068T.

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies: LN and V_{CC}						
V_{LN}	voltage drop over circuit between LN and V_{EE}	microphone inputs open				
		I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.2	4.45	4.7	V
		I_{line} = 100 mA	5.4	6.1	6.7	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	voltage drop variation with temperature	I_{line} = 15 mA	–4	–2	0	mV/K
V_{LN}	voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	3.45	3.8	4.1	V
		R_{VA} (REG to SLPE) = 39 kΩ	4.65	5	5.35	V
I_{CC}	supply current	V_{CC} = 2.8 V				
		PD = LOW	–	0.96	1.3	mA
		PD = HIGH	–	55	82	μA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH				
		I_p = 1.2 mA	2.8	3.05	–	V
		I_p = 0 mA	3.5	3.75	–	V
Microphone inputs MIC+ and MIC–						
$\lvert Z_i \rvert$	input impedance	differential between MIC+ and MIC–	51	64	77	kΩ
		single-ended MIC+ or MIC– to V_{EE}	25.5	32	38.5	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain from MIC+/MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ;	51	52	53	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and f = 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C; without R6	–	±0.2	–	dB
Dual-tone multi-frequency input DTMF						
$\lvert Z_i \rvert$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and f = 3400 Hz	with respect to 800 Hz	–0.5	±0.2	+0.5	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C	–	±0.5	–	dB
Gain adjustment connections GAS1 and GAS2						
ΔG_v	gain variation with R7, transmitting amplifier		–8	–	+8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmitting amplifier output LN						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA				
		THD = 2%	1.9	2.3	–	V
		THD = 10%	–	2.6	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	–	–72	–	dBmp
Receiving amplifier input IR						
$\|Z_i\|$	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR+ and QR–						
$\|Z_o\|$	output impedance	single ended	–	4	–	Ω
G_v	voltage gain from IR to QR+ or QR–	I_{line} = 15 mA				
		R_L (from QR+ or QR–) = 300 Ω; single-ended	24	25	26	dB
		R_L (from QR+ or QR–) = 600 Ω; differential	30	31	32	dB
ΔG_{vf}	gain variation with frequency at f = 300 Hz and f = 3400 Hz	with respect to 800 Hz	–0.5	–0.2	0	dB
ΔG_{vT}	gain variation with temperature at T_{amb} = –25 °C and +75 °C	I_{line} = 50 mA; with respect to 25 °C; without R6	–	±0.2	–	dB
$V_{o(rms)}$	output voltage (RMS value)	sine wave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ				
		single-ended; R_L = 150 Ω	0.3	0.38	–	V
		single-ended; R_L = 450 Ω	0.4	0.52	–	V
		differential; f = 3400 Hz; R_{series} = 100 Ω; C_L = 47 nF	0.8	1.0	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve)				
		single-ended; R_L = 300 Ω	–	50	–	μV
		differential; R_L = 600 Ω	–	100	–	μV
Gain adjustment GAR						
ΔG_v	gain variation of receiving amplifier achievable by varying R4 between GAR and QR		–8	–	+8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE input						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{MUTE}	input current		–	8	15	μA
ΔG_v	voltage gain reduction between MIC+ and MIC– to LN	MUTE = HIGH	–	70	–	dB
G_v	voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	–21	–19	–17	dB
Power-Down input PD						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{pd}	input current in power-down condition		–	5	10	μA
Automatic Gain Control input AGC						
ΔG_v	gain control range from IR to QR+/QR– and from MIC+/MIC– to LN	I_{line} = 70 mA; R6 = 110 kΩ between AGC and V_{EE}	–5.5	–5.9	–6.3	dB
$I_{line(H)}$	highest line current for maximum gain	R6 = 110 kΩ between AGC and V_{EE}	–	23	–	mA
$I_{line(L)}$	lowest line current for minimum gain	R6 = 110 kΩ between AGC and V_{EE}	–	61	–	mA
ΔG_v	voltage gain variation	between I_{line} = 15 mA and I_{line} = 35 mA; R6 = 110 kΩ between AGC and V_{EE}	–1.0	–1.5	–2.0	dB

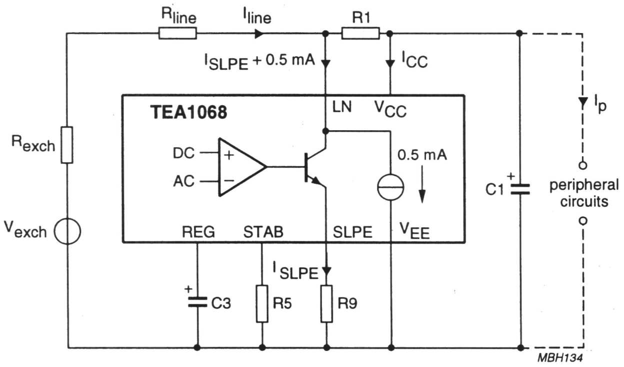
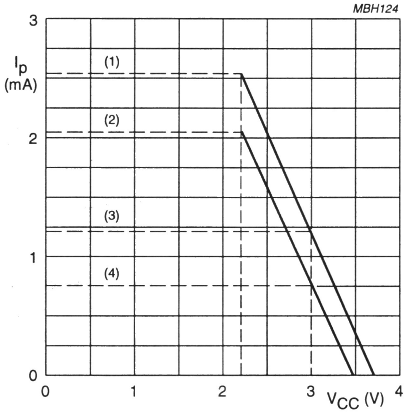

Rline
Iline
R1
ISLPE + 0.5 mA
ICC
TEA1068
LN
VCC
Ip
Rexch
DC
AC
0.5 mA
C1
peripheral circuits
Vexch
REG
STAB
SLPE
VEE
ISLPE
C3
R5
R9
MBH134

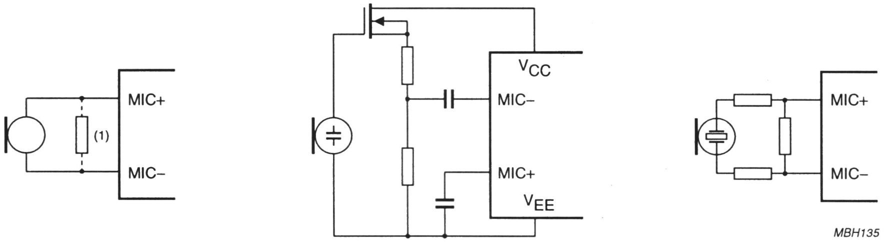
Fig.9 Supply arrangement.



Curve (1) is valid when the receiving amplifier is not driven or when MUTE = HIGH. Curve (2) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV; R_L = 150 Ω asymmetrical.

The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

Fig.10 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} \geq 2.2$ V.



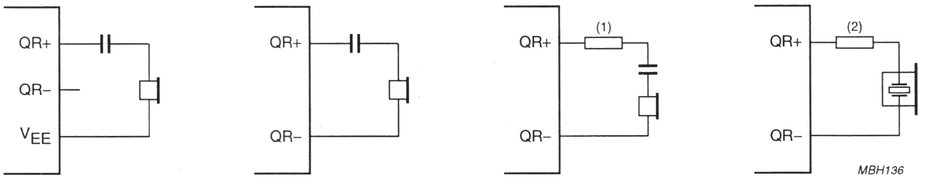
a. Magnetic or dynamic microphone.

b. Electret microphone.

c. Piezoelectric microphone.

(1) May be connected to decrease the terminating impedance.

Fig.11 Alternative microphone arrangements.



a. Dynamic earpiece with less than 450 Ω impedance.

b. Dynamic earpiece with more than 450 Ω impedance.

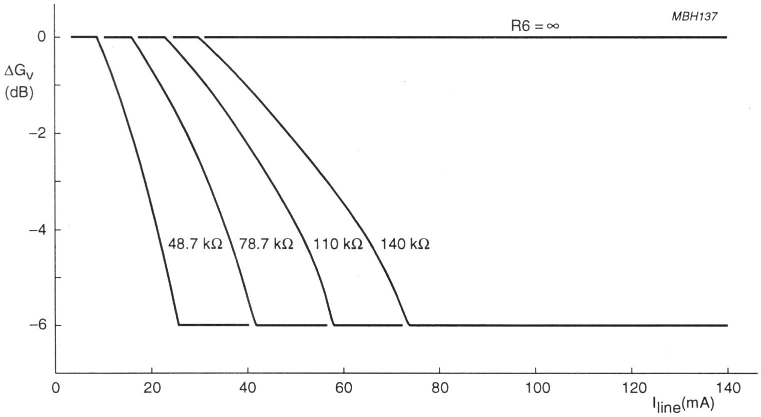
c. Magnetic earpiece with more than 450 Ω impedance.

d. Piezoelectric earpiece.

(1) May be connected to prevent distortion (inductive load).

(2) Required to increase the phase margin (capacitive load).

Fig.12 Alternative receiver arrangements.

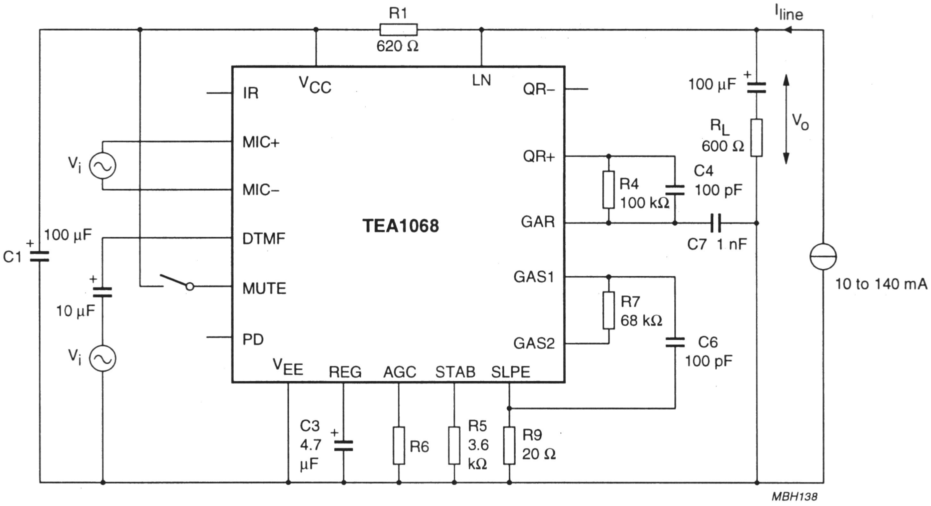


R9 = 20 Ω.

Fig.13 Variation of gain with line current, with R6 as a parameter.

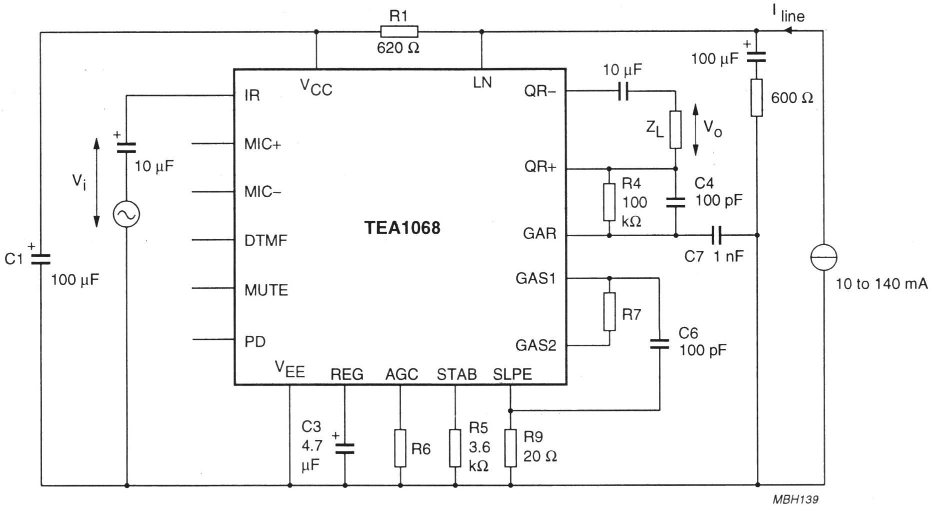
Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
24	61.9	48.7	X	X
36	100	78.7	68	60.4
48	140	110	93.1	82
60	X	X	120	102


R1
620 Ω
I_{line}
IR
V_{CC}
LN
QR−
MIC+
MIC−
DTMF
MUTE
PD
TEA1068
QR+
GAR
GAS1
GAS2
V_{EE}
REG
AGC
STAB
SLPE
V_i
V_i
C1
100 μF
10 μF
100 μF
R_L
600 Ω
V_o
R4
100 kΩ
C4
100 pF
C7 1 nF
10 to 140 mA
R7
68 kΩ
C6
100 pF
C3
4.7
μF
R6
R5
3.6
kΩ
R9
20 Ω
MBH138

Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC−, the MUTE input should be LOW or open, for measuring the DTMF input, MUTE should be HIGH. Inputs not under test should be open.

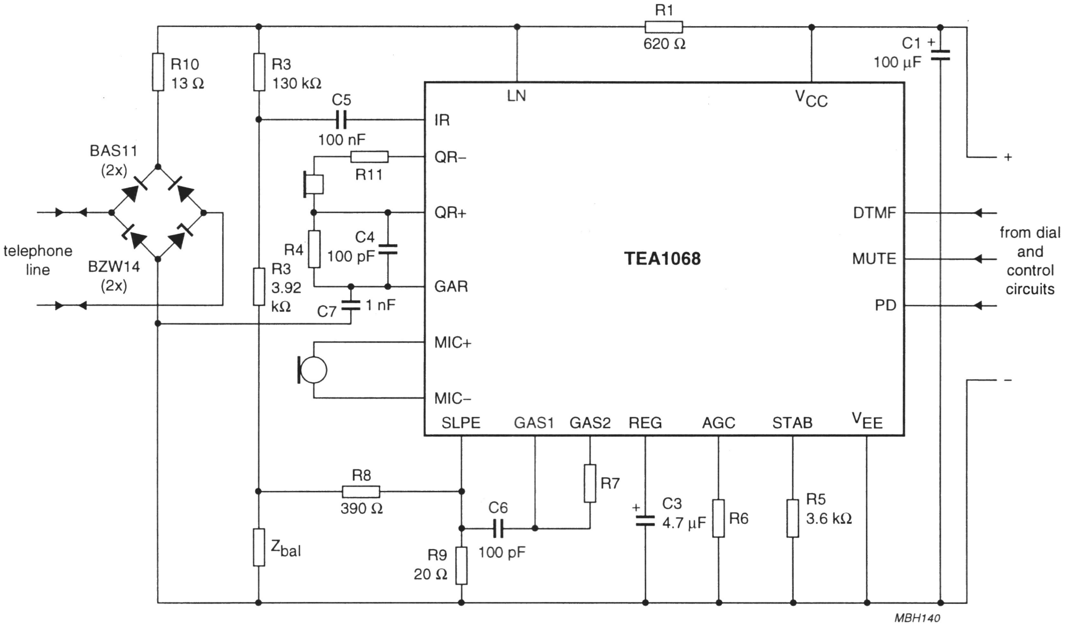
Fig.14 Test circuit for defining voltage gain of MIC+, MIC− and DTMF inputs.


R1
620 Ω
I line
+
100 µF
600 Ω
10 µF
IR
VCC
LN
QR−
ZL
Vo
+
10 µF
Vi
MIC+
MIC−
QR+
R4
100
kΩ
C4
100 pF
TEA1068
DTMF
GAR
C7 1 nF
C1
+
100 µF
MUTE
GAS1
R7
10 to 140 mA
C6
100 pF
PD
GAS2
VEE
REG
AGC
STAB
SLPE
C3
4.7
µF
+
R6
R5
3.6
kΩ
R9
20 Ω
MBH139

Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$.

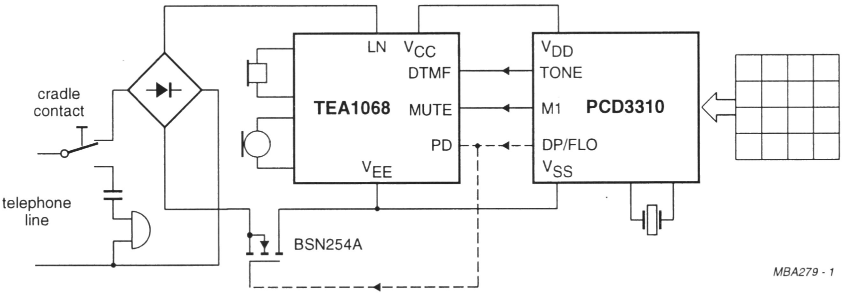
Fig.15 Test circuit for defining voltage gain of the receiving amplifier.

APPLICATION INFORMATION


R1
620 Ω
R10
13 Ω
R3
130 kΩ
C5
100 nF
C1 +
100 μF
LN
VCC
IR
QR−
R11
BAS11
(2x)
QR+
C4
100 pF
R4
telephone
line
BZW14
(2x)
R3
3.92
kΩ
C7
1 nF
GAR
TEA1068
DTMF
MUTE
PD
from dial
and
control
circuits
+
−
MIC+
MIC−
SLPE
GAS1
GAS2
REG
AGC
STAB
VEE
R8
390 Ω
R7
C6
100 pF
C3
4.7 μF
R6
R5
3.6 kΩ
Zbal
R9
20 Ω
MBH140

Typical application of the TEA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

Fig.16 Application diagram.


cradle contact
telephone line
LN
V_{CC}
DTMF
TEA1068
MUTE
PD
V_{EE}
V_{DD}
TONE
M1
PCD3310
DP/FLO
V_{SS}
BSN254A
MBA279 - 1

The dashed lines show an optional flash (register recall by timed loop break).

Fig.17 DTMF set with a CMOS DTMF dialling circuit.

Versatile speech/dialler/ringer with music-on-hold

TEA1069N

FEATURES

Speech part

- Voltage regulator with adjustable static resistance
- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Supply for dialler part and peripherals (not stabilized)
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic, or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- Asymmetrical earpiece output for dynamic, magnetic, or piezoelectric earpieces
- Internal mute to disable speech during dialling
- Confidence tone during DTMF dialling
- Line-loss compensation (line-current dependent) for microphone and earpiece amplifiers
- Gain-control curve adaptable to the exchange supply.

Dialler part

- Pulse/DTMF and mixed mode dialling
- Last Number Redial (LNR), up to 32 digits
- 13 repertory numbers (3 direct and 10 indirect) or 10 repertory numbers (10 direct), up to 32 digits, with a maximum of 224 digits in total
- Repertory and redial memory integrity check (memory contents check)
- Notepad memory function
- Flash and earth register recall
- Dial mode output
- Access pause generation and termination
- Function keys for: store, memory recall, register recall, LNR, pause, hold, mute, hook
- Keytone generation
- Handsfree control
- Volume control in handsfree mode (VOL+/VOL–)
- Hold function
- Mute function
- Music-on-hold
- Diode options:
  - DTMF tone burst/pause time
  - make/break ratio
  - access pause time
  - pulse or DTMF mode selection
  - register recall (earth and flash times)
  - keyboard layout selection
  - selection for german requirements
  - hold/mute mode selection.

Ringer part

- Ringer input frequency discrimination
- Ringer melody generation (3-tone)
- Ringer melody selection/volume control via keyboard
- Diode option: ringer frequency selection.

GENERAL DESCRIPTION

The TEA1069N contains all the functions needed to build a highly featured, high-performance fully electronic telephone set.

The device incorporates a speech/transmission part, a dialler part and a ringer part. By offering a wide range of possible adaptations for each part, the TEA1069N application can be easily adapted to meet different requirements.

Speech part

The speech/transmission part performs all speech and line interface functions required in electronic sets. It operates at line voltages down to 1.6 V DC to facilitate the use of more telephones connected in parallel.

Dialler part

The dialler part offers a 32-digit Last Number Redial (LNR) and 13 memories. Handsfree control is included allowing the TEA1069N to be used not only in basic telephones, but also in feature phones offering handsfree dialling via the TEA1083 call-progress monitor IC and/or full handsfree operation via the TEA1093 handsfree IC. The hold function allows the user to suspend the conversation and resume the call either on the same phone or on a parallel phone. Additionally through the music-on-hold function a melody is transmitted while the set is put on hold.
The keytones provide in a buzzer an audible feedback of a valid key pressed.

Ringer part

The ringer part offers a discriminator input which enables the tone output as soon as a valid ring frequency is detected. It offers a melody based on 3 tones with programmable melody and volume via keyboard.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1069N	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1

BLOCK DIAGRAM

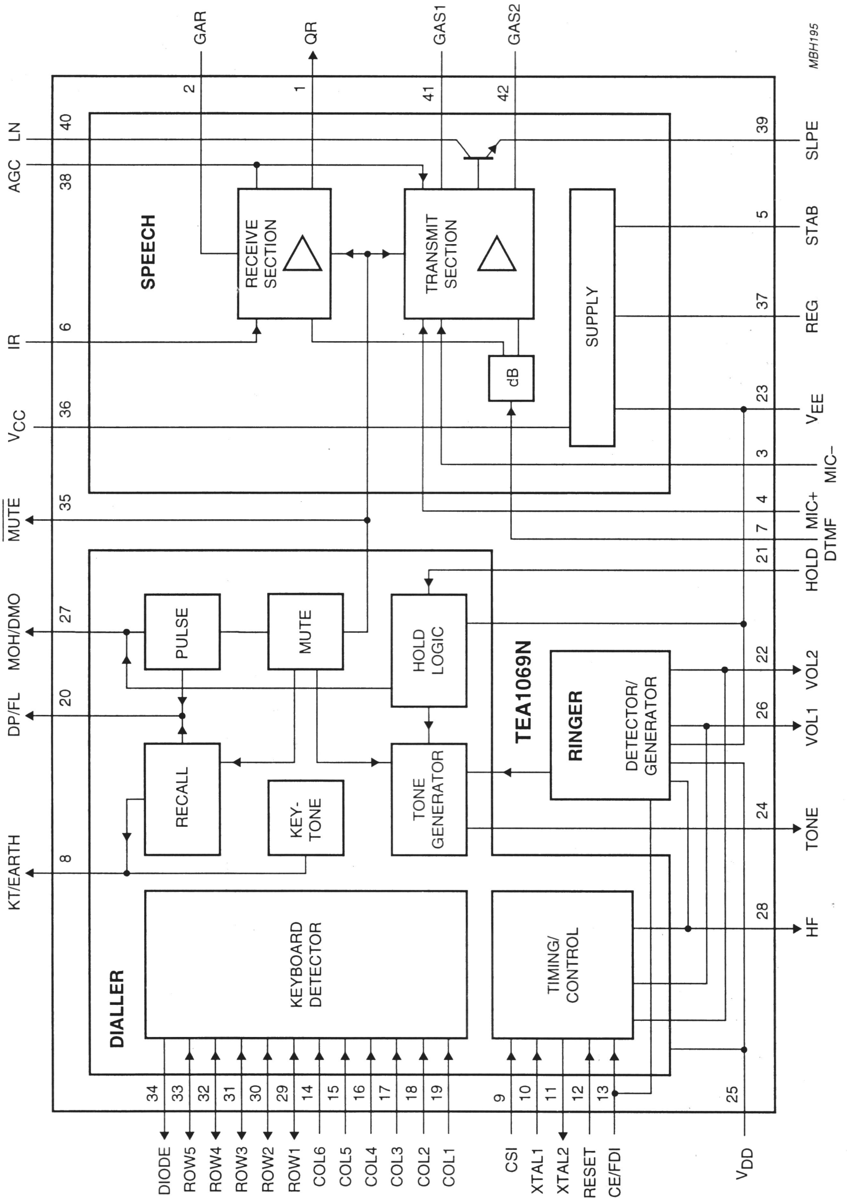

GAR
QR
GAS1
GAS2
MBH195
LN
AGC
IR
V_{CC}
$\overline{\text{MUTE}}$
MOH/DMO
DP/FL
KT/EARTH
SLPE
STAB
REG
V_{EE}
MIC−
MIC+
DTMF
HOLD
VOL2
VOL1
TONE
HF
V_{DD}
DIODE
ROW5
ROW4
ROW3
ROW2
ROW1
COL6
COL5
COL4
COL3
COL2
COL1
CSI
XTAL1
XTAL2
RESET
CE/FDI
40
38
6
36
35
27
20
8
2
1
41
42
39
5
37
23
3
4
7
21
22
26
24
28
25
34
33
32
31
30
29
14
15
16
17
18
19
9
10
11
12
13
SPEECH
RECEIVE SECTION
TRANSMIT SECTION
SUPPLY
dB
DIALLER
PULSE
MUTE
HOLD LOGIC
RECALL
KEY-TONE
TONE GENERATOR
KEYBOARD DETECTOR
TIMING/CONTROL
TEA1069N
RINGER
DETECTOR/GENERATOR

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
QR	1	receiving amplifier output
GAR	2	gain adjustment; receiving amplifier
MIC−	3	inverting microphone input
MIC+	4	non-inverting microphone input
STAB	5	current stabilizer
IR	6	receiving amplifier input
DTMF	7	dual-tone multi-frequency input
KT/EARTH	8	keytone/earth recall output
CSI	9	cradle switch input
XTAL1	10	oscillator input
XTAL2	11	oscillator output
RESET	12	reset input
CE/FDI	13	chip enable/frequency discrimination input
COL6	14	keyboard column input
COL5	15	keyboard column input
COL4	16	keyboard column input
COL3	17	keyboard column input
COL2	18	keyboard column input
COL1	19	keyboard column input
DP/FL	20	dial pulse/flash output
HOLD	21	hold control input
VOL2	22	volume 2 output
V_{EE}	23	negative line terminal
TONE	24	tone generator output
V_{DD}	25	dialler/ringer part supply voltage
VOL1	26	volume 1 output
MOH/DMO	27	music on hold/dial mode output
HF	28	handsfree control output
ROW1	29	keyboard row input/output
ROW2	30	keyboard row input/output
ROW3	31	keyboard row input/output
ROW4	32	keyboard row input/output
ROW5	33	keyboard row input/output
DIODE	34	diode option output
$\overline{\text{MUTE}}$	35	mute output, active LOW
V_{CC}	36	speech part supply voltage
REG	37	(DC) line voltage regulator decoupling
AGC	38	automatic gain control input
SLPE	39	slope (DC resistance) adjustment
LN	40	positive line terminal
GAS1	41	gain adjustment; transmitting amplifier
GAS2	42	gain adjustment; transmitting amplifier

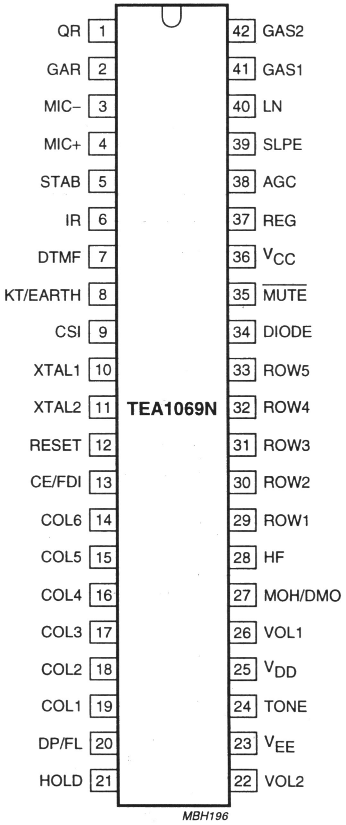

TEA1069N
QR 1
GAR 2
MIC− 3
MIC+ 4
STAB 5
IR 6
DTMF 7
KT/EARTH 8
CSI 9
XTAL1 10
XTAL2 11
RESET 12
CE/FDI 13
COL6 14
COL5 15
COL4 16
COL3 17
COL2 18
COL1 19
DP/FL 20
HOLD 21
42 GAS2
41 GAS1
40 LN
39 SLPE
38 AGC
37 REG
36 V_CC
35 MUTE
34 DIODE
33 ROW5
32 ROW4
31 ROW3
30 ROW2
29 ROW1
28 HF
27 MOH/DMO
26 VOL1
25 V_DD
24 TONE
23 V_EE
22 VOL2
MBH196

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Speech part

For numbering of components refer to Figs 26 and 27.

SUPPLIES V_{CC}, LN, SLPE, REG AND STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line (see Fig.3).

The circuit creates a stabilized voltage (V_{ref} = 3.7 V) between LN and SLPE. This reference voltage is temperature compensated and can be adjusted by means of an external resistor R_{VA}. It can be increased by connecting an R_{VA} resistor (R60) between REG and SLPE or decreased by connecting an R_{VA} resistor (R61) between REG and LN. This internal voltage reference is decoupled by capacitor C3 between REG and V_{EE}. This decoupling capacitor realises the set impedance conversion from its DC value to its AC value in the audio frequency range.

The internal transmission part of the circuitry (including the earpiece amplifier) is supplied from V_{CC}. This voltage supply is derived from the LN voltage via a dropping resistor (R1) and must be decoupled by a capacitor (C1) between V_{CC} and V_{EE}. This supply point may also be used to supply the dialler/ringer (V_{DD}) part or external circuit e.g. electret microphone.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch} and the DC resistance of the telephone line R_{line}. When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p), the excess current is shunted to SLPE via LN.

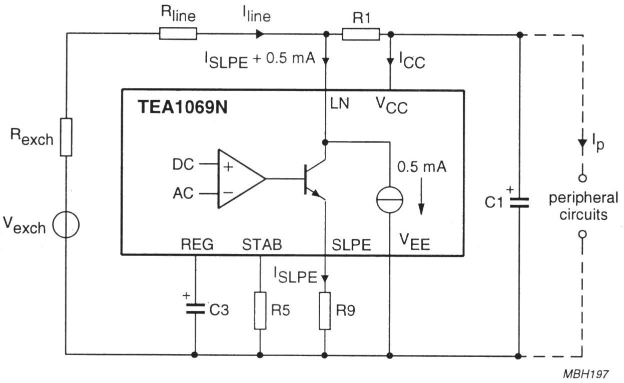


Fig.3 Supply arrangement.

Thus, the regulated voltage on the line terminal (V_{LN}) can be calculated as:

$V_{LN} = V_{ref} + I_{SLPE} \times R9$, where

$I_{SLPE} = I_{line} - \left(I_{CC} + I_p + 0.5 \times 10^{-3} A\right)$

V_{ref} is the internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}.

The circuit has an internal current stabilizer operating at a level determined by resistor R5 connected between STAB and V_{EE}.

In normal use the value of R5 would be 3.6 kΩ and the value of R9 would be 20 Ω.

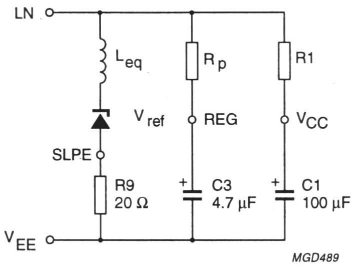
Changing the value of R5 or R9 will affect microphone gain, DTMF gain, gain control characteristics, sidetone level, maximum output swing on LN and the DC characteristics (especially at low line current).

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V.

At line currents below 9 mA the circuit has limited sending and receiving levels.

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5$ mA + I_p, the static behaviour of the circuit is that of a 3.7 V regulator diode (V_{ref}) with an internal resistance equal to that of R9.

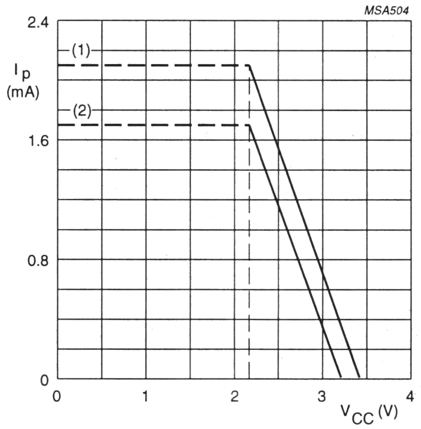
In the audio frequency range the dynamic impedance is largely determined by R1. Fig.4 shows the equivalent impedance of the circuit.



$L_{eq} = C3 \times R9 \times R_p$.
$R_p = 16.2$ kΩ.

Fig.4 Equivalent impedance circuit.

Current (I_p) available from V_{CC} for the dialler part and peripheral circuits depends on the external components used. Figure 5 shows this current for $V_{CC} > 2.2$ V. When $\overline{\text{MUTE}}$ is HIGH i.e. when the receiving amplifier (supplied from V_{CC}) is driven, the available current is further reduced. Current availability can be increased by connecting the supply IC TEA1081 in parallel with R1, or by increasing the DC line voltage by means of an external resistor (R_{VA} = R60) connected between REG and SLPE.



$V_{CC} > 2.2$ V; $I_{line} = 15$ mA at $V_{LN} = 4$ V; R1 = 620 Ω; R9 = 20 Ω.

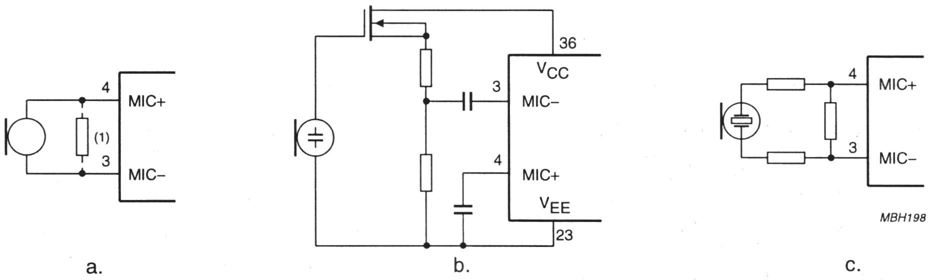
(1) $I_P = 2.1$ mA. The curve is valid when the receiving amplifier is not driven or when $\overline{\text{MUTE}}$ = LOW.

(2) $I_P = 1.7$ mA. The curve is valid when $\overline{\text{MUTE}}$ = HIGH and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150$ Ω.

Fig.5 Typical current I_P available from V_{CC} for peripheral circuitry.

MICROPHONE INPUTS MIC+ AND MIC– AND GAIN PINS GAS1 AND GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are illustrated in Fig.6.



a. Magnetic or dynamic microphone.
b. Electret microphone.
c. Piezoelectric microphone.

(1) Resistor may be connected to reduce the terminating impedance.

Fig.6 Alternative microphone arrangements.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by two external capacitors, C6 connected between GAS1 and SLPE and C17 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C17 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 × C6.

RECEIVING AMPLIFIER IR, QR AND GAR

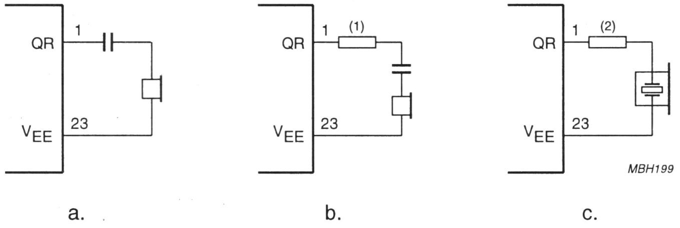
The receiving amplifier has one input (IR) and one output (QR). Earpiece arrangements are illustrated in Fig.7. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use.

The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by subtracting the anti-sidetone network attenuation (32 dB) from the amplifier gain.

Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4.

The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 × C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.



a. Dynamic earpiece.
b. Magnetic earpiece.
c. Piezoelectric earpiece.

(1) Resistor may be connected to prevent distortion (inductive load).
(2) Resistor is required to increase the phase margin (capacitive load).

Fig.7 Alternative receiver arrangements.

DUAL TONE MULTI-FREQUENCY INPUT DTMF

When the DTMF input is enabled ($\overline{\text{MUTE}}$ is LOW) dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The tones can be heard in the earpiece at a low level (confidence tone).

AUTOMATIC GAIN CONTROL INPUT AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current.

The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.8 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line-loss compensation is required the AGC pin may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

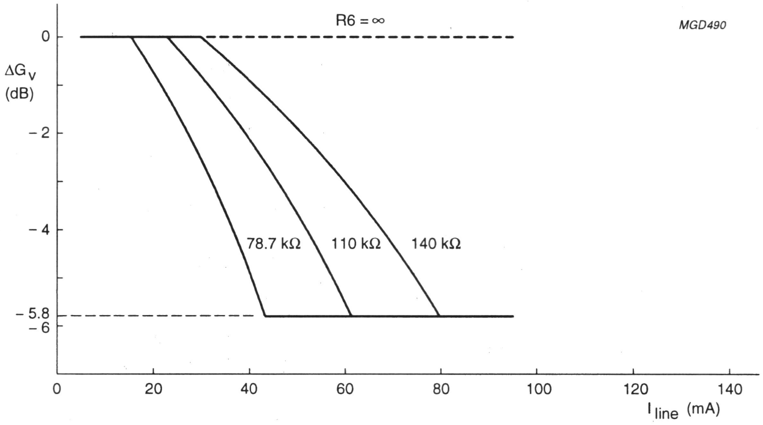


Fig.8 Variation of gain as function of line current with R6 as parameter.

Table 1 Values of resistor R6 for optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω

V_{exch} (V)	R6 (kΩ)			
	R_{exch} = 400 Ω	R_{exch} = 600 Ω	R_{exch} = 800 Ω	R_{exch} = 1000 Ω
36	100	78.7	–	–
48	140	110	93.1	82
60	–	–	120	102

SIDETONE SUPPRESSION

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line}, R2, R3, R8, R9 and Z_{bal} (see Fig.9). The maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1 \times (R3 + R8) \quad (1)$$

$$k = R3 \times \frac{(R8 + R9)}{(R2 \times R9)} \quad (2)$$

$$Z_{bal} = k \times Z_{line} \quad (3)$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 series for Z_{line}. In practice, Z_{line} varies considerably with the line type and length. Therefore, the value chosen for Z_{bal} should be for an average line length thus giving optimum setting for short or long lines.

Example: the balance impedance Z_{bal} at which the optimum suppression is present can be calculated as follows:
suppose Z_{line} = 210 Ω + (1265 Ω//140 nF) representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω;
Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1069N shown in Fig.9 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range. Figure 10 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances. More information on the balancing of anti-sidetone bridges can be found in our publication *"Wirebound telecom Applications Handbook"*.

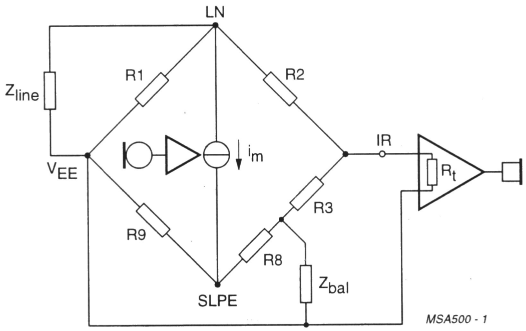


Fig.9 Equivalent circuit of TEA1069N anti-sidetone bridge.

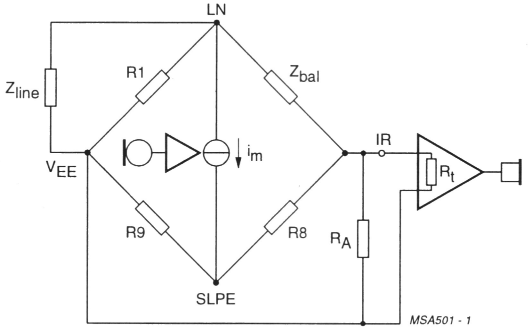


Fig.10 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

Dialler and ringer part

SUPPLY VOLTAGE: PINS V_{DD} AND V_{EE}

The power supply must be maintained for data storage. The RAM retention voltage (standby supply voltage) may drop down to 1.0 V. Applying a large capacitor across the supply terminals can retain the memory if power connections are broken. The minimum operation voltage is 2.5 V. The internal power-on reset is enabled for a voltage below this minimum operation voltage.

OSCILLATOR INPUT/OUTPUT: PINS XTAL1 AND XTAL2

Time base for the TEA1069N is a crystal-controlled on-chip oscillator which is completed by connecting a 3.579545 MHz crystal or ceramic resonator between XTAL1 and XTAL2. The oscillator starts when V_{DD} reaches the operation voltage level and CE/FDI = HIGH. The following types of ceramic resonators are recommended:

- Kyocera PBRC3.58ARPC10 (wired)
- Kyocera KBR3.58MSATRPC10 (SMD)
- Murata CSA3.58MG310VA (wired).

RESET INPUT: PIN RESET

Pin RESET is an input to the internal reset circuit. When RESET = HIGH, it can be used to initialize the TEA1069N which is normally done by the CE/FDI input. The on-chip power-on reset generates a reset pulse if V_{DD} drops below 2.5 V. In this event a proper start-up occurs after the supply voltage rises above the minimum operation voltage level again. During and directly after reset pins 14 to 19, 21, 29 to 32, 34 and 35 are set HIGH; pins 8, 20, 22, 26 to 28 and 33 are set to LOW.

The reset pin can be connected to V_{EE}, preferably via a resistor of 100 kΩ to 1 MΩ, which will save leakage current. A capacitor to V_{DD} can be used to extend the reset time, in case a longer reset is desirable.

To prevent the dialler from reacting on voltage disturbances on the telephone line a timeout is active. The dialler returns to standby state if the voltage on the line has disappeared for more than this reset-delay time (t_{rd}).

CHIP ENABLE/FREQUENCY DISCRIMINATOR INPUT: PIN CE/FDI

This active HIGH input is used to initialize part of the system, to select the on-line, standby, or ringer mode and to detect line power breaks. CE/FDI = HIGH as long as the TEA1069N must be in the on-line mode.

In the exchange, several AC signals can be superimposed on the DC signal, e.g. dialling tone, busy tone, disturbances (like line power breaks), and the ringer signal. The ringer signal is evaluated, and checked if its frequency is within the limits of the frequency interval as set by the diode option RFS. It is assumed that the ringer frequency at pin CE/FDI is the double of the frequency present on the telephone line.

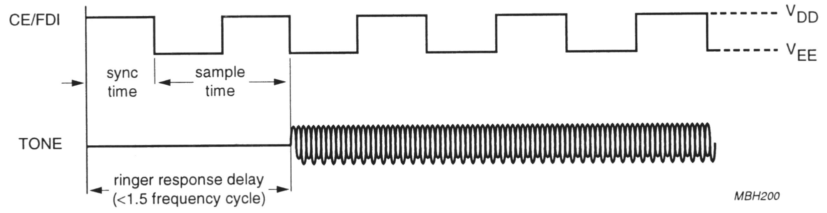


Fig.11 Ringer frequency detection.

In case of a valid ringer signal the user is alerted through a melody at the TONE output, generated by the ringer part of the TEA1069N. This melody follows the cadence of the ringer signal. Both the melody and the volume can be selected. The melody frequency and duration are given in Table 2.

Table 2 Ringer melodies

NAME	FREQUENCY (Hz)	DURATION (ms)
Bell 1	800 + 1066 + 1333	28 + 28 + 28
Bell 2	826 + 925 + 1027	28 + 28 + 28
Bell 3	1037 + 1161 + 1297	28 + 28 + 28
Bell 4	1297 + 1455 + 1621	28 + 28 + 28

CRADLE SWITCH INPUT: PIN CSI

To distinguish among different operating states after CE/FDI is activated, input CSI is used. The basic states are shown in Table 3.

Table 3 TEA1069N basic states

INPUT CSI	INPUT CE/FDI	STATE
LOW	LOW	standby
HIGH	LOW	not applicable
LOW	HIGH	ringer
HIGH	HIGH	on-line

For the handsfree state refer to Fig.22.

PULSE DIALLER: PINS DP/FL, MOH/DMO AND $\overline{\text{MUTE}}$

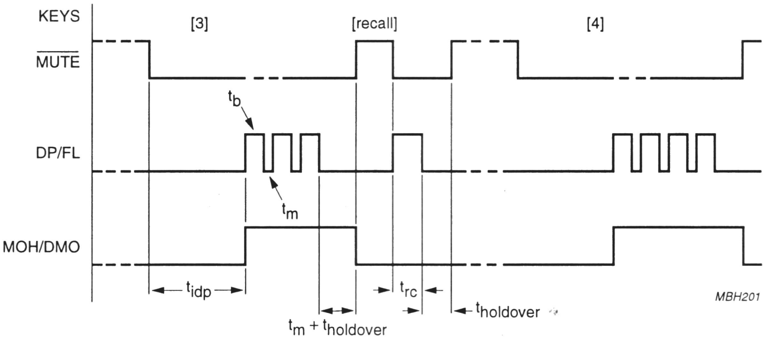
The pulse dialling system uses line current interruptions to signal the digits dialled to the exchange. The number of line current interruptions corresponds with the digit dialled except for the digit [0] which is characterized by 10 interruptions. Before each digit there is an inter-digit pause.

Valid keys are the digits [0] to [9] and [PAUSE].

The pulse dialling mode, the make/break ratio and the access pause time depend on the diode options: PTS, M/B and APT. DP/FL is LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

The MOH/DMO pin (diode GOS = **on**) is used to reduce the voltage swing over the a/b terminals during pulse dialling. Several countries require this feature. The $\overline{\text{MUTE}}$ pin is an open drain output which requires a pull-up resistor. $\overline{\text{MUTE}}$ is HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

Figure 12 shows the timing diagram in pulse dialling mode when keys [3], [RECALL] and [4] are pressed.



t_b = break time.
t_m = make time.
t_{idp} = interdigit pause time.
t_{rc} = recall time.
$t_{holdover}$ = holdover time.

Fig.12 Timing diagram in pulse dialling mode.

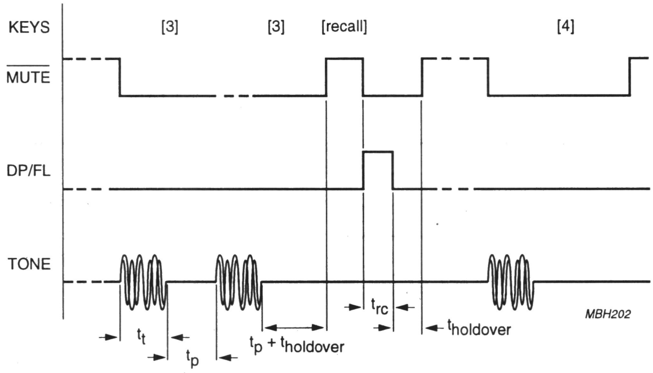
TONE DIALLER: PINS TONE AND $\overline{\text{MUTE}}$

In this system digits are transmitted as two tones simultaneously, the so called Dual-Tone Multi-Frequency (DTMF) system. Tone digits are separated by a pause time. Valid keys are the digits [0] to [9], [∗], [#] and [PAUSE].

The DTMF dialling mode, the tone burst/pause times and the access pause time depend on the diode options: PTS, TBT and APT.

The $\overline{\text{MUTE}}$ pin is an open drain output which requires a pull-up resistor. $\overline{\text{MUTE}}$ is HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

Figure 13 shows the timing diagram in tone dialling mode when successively keys [3], [3], [RECALL] and [4] are dialled.



t_t = burst time.
t_p = pause time.
$t_{holdover}$ = holdover time.
t_{rc} = recall time.

Note: in case of manual dialling only the minimum tone burst and pause time values depend on the chosen diode option, the maximum tone burst/pause times are equal to the real key press/release time.

Fig.13 Timing diagram in tone dialling mode.

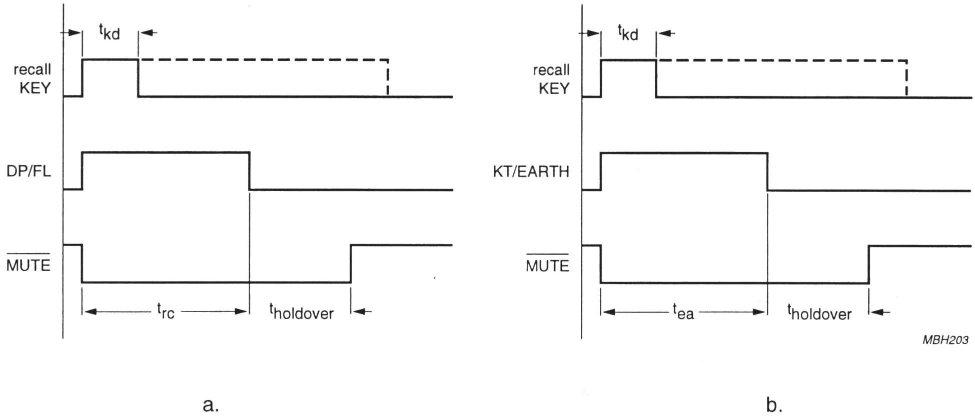
The DC-level at the TONE output measures ½V_{DD} and the impedance is typically 100 Ω. DTMF frequencies are composed by transmitting 2 tones simultaneously at pin TONE. The frequency tolerance for the tones at output TONE is shown in Table 4.

Table 4 DTMF frequency tolerances

DTMF FREQUENCY	FREQUENCY AT TONE	DEVIATION (%)	DEVIATION (Hz)
697	697.90	+0.13	+0.90
770	770.46	+0.06	+0.46
852	852.45	−0.18	−1.55
941	943.23	+0.24	+2.23
1209	1206.45	−0.21	−2.55
1336	1341.66	+0.42	+5.66
1477	1482.21	+0.35	+5.21

REGISTER RECALL: PINS DP/FL AND KT/EARTH

The RECALL function results in a calibrated pulse which drives the electronic line current interrupter via pin DP/FL or KT/EARTH. Flash or earth selection and various flash interruption times depend on the diode options: FES A and FES B (diode GOS = **on;** see Fig.14).



a. Recall using flash; t_{rc} = recall time using flash.
b. Recall using earth; t_{ea} = recall time using earth.

t_{kd} = key pressed time (depends on user).
$t_{holdover}$ = holdover time.

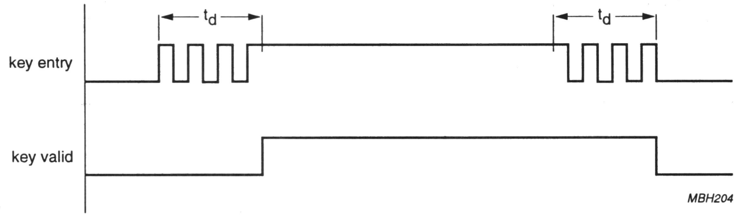
Fig.14 Recall mode timing diagram.

KEYBOARD: PINS ROW1 TO ROW5 AND COL1 TO COL6

The sense columns inputs and scanning rows outputs are directly connected to a single contact keyboard matrix. A second key entry will be valid after having released the first button and after having pressed the second button. Simultaneously pressing 2 buttons will disable the first entered key. A key entry becomes valid when the debounce time t_d has elapsed.

The column and row pins (except ROW5) are HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

ROW5 is an open-drain input/output; this configuration is used to avoid current flowing in the on-line or standby state. A pull-up resistor should be connected to ROW5. ROW5 is LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.


key entry
key valid
t_d
t_d
MBH204

t_d = debounce time.

Fig.15 Timing diagram debouncing.

Keyboard layout

The TEA1069N supports three different keyboard layouts:

- with 10 direct accessible repertory numbers
- with 10 indirect accessible repertory numbers
- with 3 direct accessible repertory numbers and 10 indirect numbers.

For layouts see Figs 16 to 18; the keyboard layout can be selected by diode option KBS.

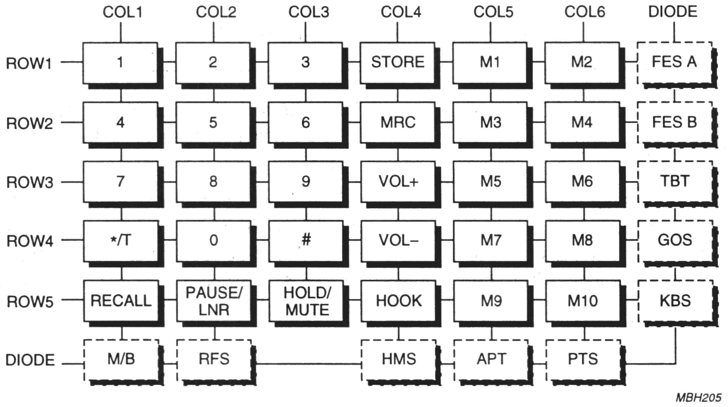

COL1
COL2
COL3
COL4
COL5
COL6
DIODE
ROW1
1
2
3
STORE
M1
M2
FES A
ROW2
4
5
6
MRC
M3
M4
FES B
ROW3
7
8
9
VOL+
M5
M6
TBT
ROW4
*/T
0
#
VOL−
M7
M8
GOS
ROW5
RECALL
PAUSE/ LNR
HOLD/ MUTE
HOOK
M9
M10
KBS
DIODE
M/B
RFS
HMS
APT
PTS
MBH205

Fig.16 Keyboard and diodes with 10 direct accessible repertory numbers.

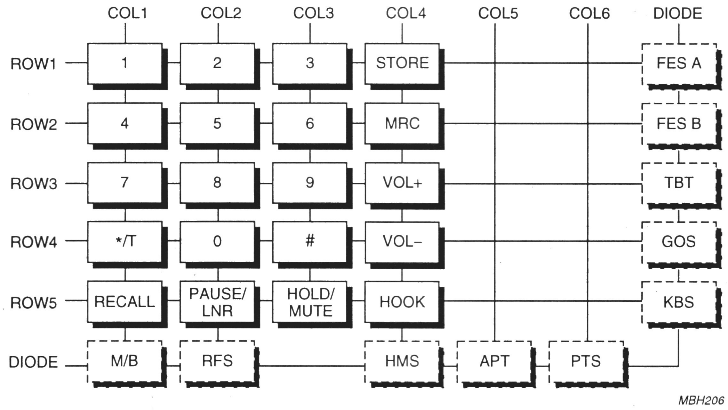

COL1
COL2
COL3
COL4
COL5
COL6
DIODE
ROW1
ROW2
ROW3
ROW4
ROW5
DIODE
1
2
3
STORE
FES A
4
5
6
MRC
FES B
7
8
9
VOL+
TBT
*/T
0
#
VOL−
GOS
RECALL
PAUSE/ LNR
HOLD/ MUTE
HOOK
KBS
M/B
RFS
HMS
APT
PTS
MBH206

Fig.17 Keyboard and diodes with 10 indirect accessible repertory numbers.

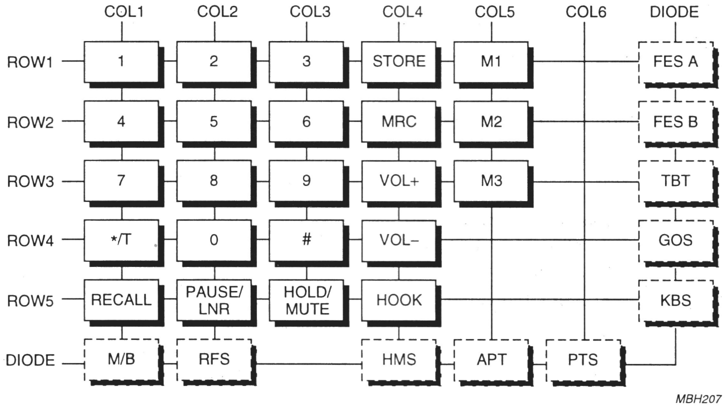

COL1
COL2
COL3
COL4
COL5
COL6
DIODE
ROW1
ROW2
ROW3
ROW4
ROW5
DIODE
1
2
3
STORE
M1
FES A
4
5
6
MRC
M2
FES B
7
8
9
VOL+
M3
TBT
*/T
0
#
VOL−
GOS
RECALL
PAUSE/ LNR
HOLD/ MUTE
HOOK
KBS
M/B
RFS
HMS
APT
PTS
MBH207

Fig.18 Keyboard and diodes with 3 direct and 10 indirect accessible repertory numbers.

DIODE OPTIONS: PIN DIODE

The DIODE pin is connected to the keyboard matrix as shown in Fig.19.

The diode options are read after each reset of the dialler.

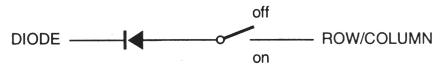


Fig.19 Diode connection.

Table 5 DIODE functions

DIODE	FUNCTION	CONDITION	ON(1)	OFF(1)
FES A	flash/earth time select	FES B = **off**	flash of 270 ms	flash of 100 ms
FES B	flash/earth time select	FES B = **on**	earth of 400 ms	flash of 600 ms
TBT	tone burst/pause time		85/85 ms	100/100 ms
GOS	german output select		pin 8 = earth; pin 27 = DMO	pin 8 = keytone; pin 27 = MOH
KBS	keyboard select		keyboard layout; see Figs 16 and 17	keyboard layout; see Fig.18
PTS	pulse/tone selection		pulse mode	DTMF mode
APT	access pause time		4 s	2 s
HMS	hold/mute select		hold mode	mute mode
RFS	ringer frequency select		29 to 146 Hz	40 to 120 Hz
M/B	make/break ratio		3 : 2	2 : 1

Note

1. **on** means option diode present; **off** means option diode not present.

KEY TONE: PIN KT/EARTH

Every time a valid key is pressed a keytone is generated with a frequency of 606 Hz and a duration of 30 ms. This function is selected by the diode GOS = **off**. KT/EARTH is LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

VOLUME CONTROL: PINS VOL1 AND VOL2

Both pins can control the volume of the ringer and/or the handsfree circuit. The state of VOL1/VOL2 is controlled by a state machine as depicted in Fig.23.

VOL1 and VOL2 are push-pull outputs. Both are set LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

MUSIC-ON-HOLD: PIN MOH/DMO

When the dialler is in the hold state (see Fig.22) a melody is generated via pin TONE. In this state pin MOH/DMO can be used via diode GOS = **off** as an enable signal for the hardware to indicate that the tone should be switched to the telephone line.

MOH/DMO is a push-pull output. It is set LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

HANDSFREE: PIN HF

During the on-line state, the handsfree output pin HF is used for enabling the handsfree hardware. The pin will change state depending on specific key-sequences (see Fig.22).

HF is a push-pull output. It is set LOW when V_{DD} is below power-on reset trip level and when RESET is HIGH.

HOLD MODE: PIN HOLD

One way to terminate the hold state (see Fig.22) is a change in state of the signal at pin HOLD. This input should reflect the line current. If current is flowing the signal at pin HOLD should be HIGH, if not it should be LOW.

This pin is not debounced. The signal applied should be filtered by the hardware. HOLD is HIGH when V_{DD} is below power-on reset trip level and when RESET is HIGH.

Key sequences

The behaviour of the TEA1069N can be modelled as a State Transition Diagram (STD) shown in Fig.20.

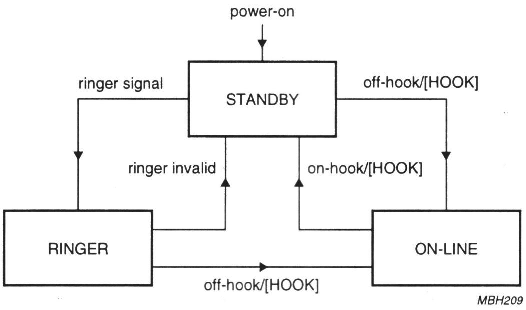


Fig.20 TEA1069N dialler/ringer states.

The STD contains the states (rectangles in the figure) and state transitions (arrows) of the set. The upper arrow in the figure pointing to the standby state means that the set is initially in the standby state. When for instance an incoming call is detected, the set enters the ringer state, waiting for a reaction of the user. If the user answers the call on a handset, the set enters the on-line state.

The TEA1069N has 3 basic states:

- standby state
- ringer state
- on-line state.

Each state with its own functional requirements is described in the following sections.

STANDBY STATE

In standby state the TEA1069N is inactive. The current drawn is for memory retention and depends on the loads of the inputs/outputs of the dialler. In this state output DP/FL is HIGH so that the line is disconnected.

The TEA1069N leaves the standby state if:

- the set goes off-hook (lift handset or press [HOOK])
- a ringer-signal is available on the line.

The TEA1069N goes to the standby state if:

- the set goes on-hook
  (handset on the cradle or press [HOOK])
- a line-break occurs for at least the reset delay time (t_{rd})
- the ringer-signal becomes invalid.

RINGER STATE

If the set is in standby mode, a ringer signal can be received from the line. After evaluating the incoming ringer signal (and ringer signal is valid), the TEA1069N starts a melody via the TONE output ringer hardware, and stops this melody if the ringer signal is not valid any more. After going off-hook, the ringer signal stops and the set is in conversation (on-line) state.

During a ringer burst the ringer volume can be changed according to Fig.23 and melodies can be changed according to Table 6.

Table 6 Melody selection

MELODY	KEY
Bell 1	[1]
Bell 2	[2]
Bell 3	[3]
Bell 4	[4]

ON-LINE STATE

In this paragraph all the actions of the TEA1069N during on-line state are described. The on-line mode starts with making output DP/FL LOW, which makes line current flow possible. The on-line state contains a number of sub-states (see Fig.21):

- conversation state
- dialling state
- memory recall state
- program state.

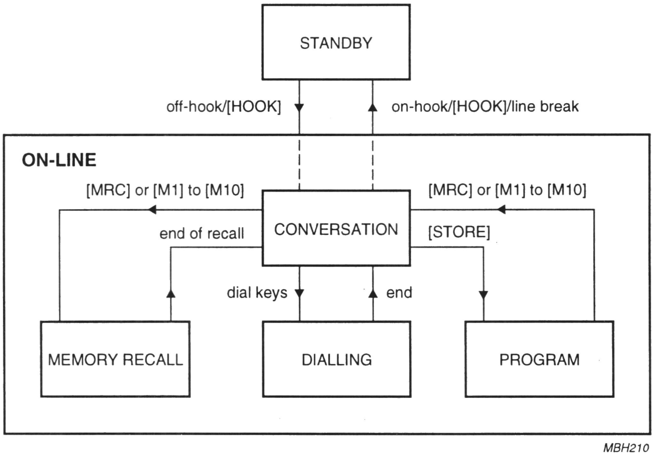

STANDBY
off-hook/[HOOK]
on-hook/[HOOK]/line break
ON-LINE
[MRC] or [M1] to [M10]
CONVERSATION
[MRC] or [M1] to [M10]
end of recall
[STORE]
dial keys
end
MEMORY RECALL
DIALLING
PROGRAM
MBH210

Fig.21 On-line states.

Conversation state

In this state conversation is possible.
A number of sub-states (see Fig.22) exist:

- handset state
- handsfree state
- hold state
- mute state.

Depending on the diode option HMS the hold or the mute state is selected.

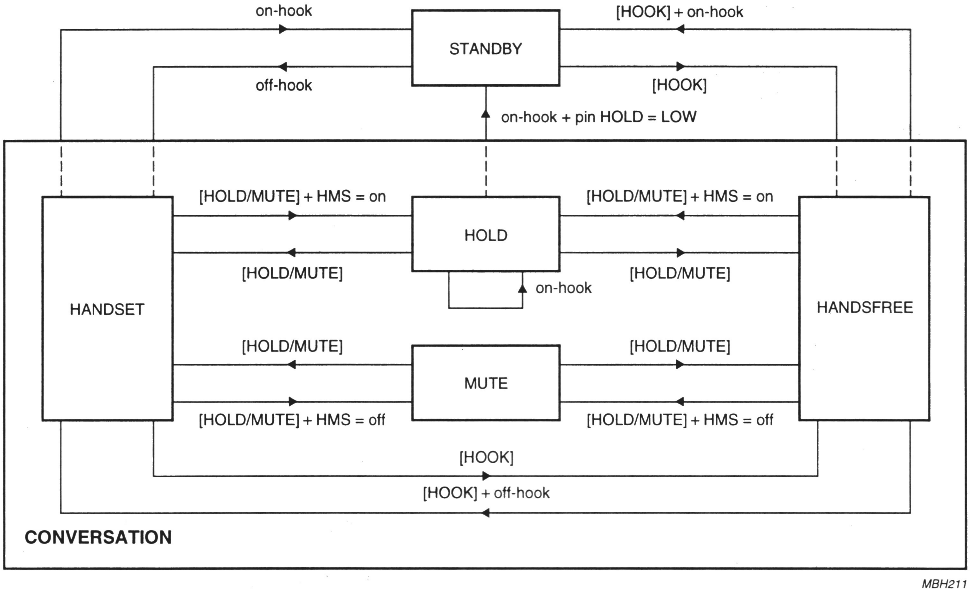

on-hook
STANDBY
[HOOK] + on-hook
off-hook
[HOOK]
on-hook + pin HOLD = LOW
[HOLD/MUTE] + HMS = on
HOLD
[HOLD/MUTE] + HMS = on
[HOLD/MUTE]
on-hook
[HOLD/MUTE]
HANDSET
HANDSFREE
[HOLD/MUTE]
[HOLD/MUTE]
MUTE
[HOLD/MUTE] + HMS = off
[HOLD/MUTE] + HMS = off
[HOOK]
[HOOK] + off-hook
CONVERSATION
MBH211

Fig.22 Conversation states.

- Handset state.

  See Fig.22.

- Handsfree state.

  In handsfree mode output HF becomes HIGH which activates a TEA1093/1094 handsfree IC. This state can be reached from standby state and from the handset state as follows:

  - the [HOOK] key is pressed during standby mode
  - the [HOOK] key is pressed during handset state is lifted, then when the handset is put on the cradle the set stays in the handsfree mode.

  The set leaves the handsfree mode and output HF becomes LOW when:

  - the [HOOK] key is pressed and the handset is on the cradle, the set goes to the standby mode
  - the [HOOK] key is pressed and the handset is lifted, the set goes to the handset state.

  The volume on the loudspeaker or buzzer, in handsfree and ringer mode, can be controlled in four levels using the [VOL+] and [VOL–] keys.

  The handsfree volume can be changed according to Fig.23.

- Hold state.

  The hold state is entered when the [HOLD/MUTE] key is pressed (diode HMS = **on**). This state can be entered either from handset state or from handsfree state. Upon entering this state outputs HF and $\overline{\text{MUTE}}$ become LOW.

  In hold state a music-on-hold melody is generated by output TONE. Pin MOH/DMO is HIGH (diode GOS = **off**) during this state. This signal can be used to adjust the volume of the TONE pin. Since $\overline{\text{MUTE}}$ is LOW the TONE output is transmitted to the telephone line. As long as the TEA1069N is in this state the HOLD input pin is tested.

  The set leaves the hold state when:

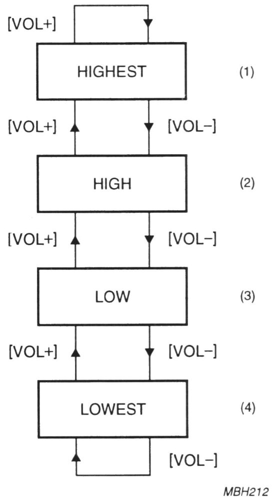
  - [HOLD/MUTE] is pressed, the set returns to either the handset or handsfree state
  - The HOLD input becomes LOW, now the TEA1069N returns to the standby state.

- Mute state.

  When the [HOLD/MUTE] key is pressed (HMS = **off**) the mute state is entered and $\overline{\text{MUTE}}$ becomes LOW.

  In mute state a music-on-hold melody is generated by output TONE. Pin MOH/DMO is HIGH (diode GOS = **off**) during this state. This signal can be used to adjust the volume of the TONE pin. Since $\overline{\text{MUTE}}$ is LOW the TONE output is transmitted to the telephone line. The mute state is left when:

- [HOLD/MUTE] is pressed, set returns to either handset- or handsfree state
- a dial action is started.



(1) VOL1 = HIGH, VOL2 = HIGH.
(2) VOL1 = LOW, VOL2 = HIGH.
(3) VOL1 = HIGH, VOL2 = LOW.
(4) VOL1 = LOW, VOL2 = LOW.

Fig.23 Volume control state machine.

Dialling state

During the dial-keys entries the TEA1069N starts immediately with transmission of the digit(s); the minimum transmission time is unaffected by the speed of the entry. Transmission continues as long as further dial-keys entries have to be processed.

However when keying-in is much faster then dialling-out, then the 32 digit dialling register will overflow. When this occurs the dialling is stopped and the error beep will be generated.

There are two dial modes: pulse dialling and tone dialling. The initial dialling mode is determined by option PTS. The state machine which controls the dial mode is described in Fig.24.

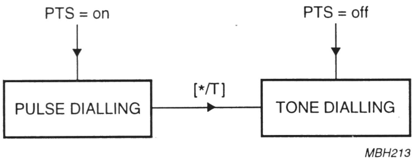


Fig.24 Dialling mode state machine.

- Pulse dialling.

  In this mode all valid keys are dialled by the pulse dialler. When during pulse dialling key [∗/T] is pressed, the TEA1069N switches over to tone dialling (mixed mode dialling). After the switch-over, valid keys are dialled by the tone dialler. The temporary tone mode is terminated by going on-hook or recall.
- Tone dialling.

  The TEA1069N converts valid keys into data for the on-chip DTMF generator. Tones are transmitted via output TONE with minimum tone burst/pause duration. The maximum tone burst/pause duration is equal to the key pressing/release time.
- Register recall (flash/earth).

  The [RECALL] key will result in a flash or earth action.
- Access pause.

  When the [PAUSE/LNR] button is not the first key pressed, an access pause is entered for repertory or redialling procedures. When an access pause is executed $\overline{\text{MUTE}}$ is HIGH. During manual dialling no access pauses are dialled.
- Last Number Redial (LNR).

  If the first key pressed is the [PAUSE/LNR] button, the number stored in the redial register is recalled and transmitted. A maximum number of 32 digits can be accepted for last number redial. If this maximum is reached the redial function is inhibited. During LNR programmed access pauses are also dialled. The [RECALL] key and the (in pulse dialling mode allowed) tone switch key [∗/T] are also stored in LNR memory.

- Notepad function.

  In conversation state it is possible to store a number into the LNR register, which may be dialled after an on-hook/off-hook action. The procedure is as follows:

  - press [STORE]
  - press to-be-stored sequence of the digits [0] to [9], [PAUSE/LNR], [∗/T] or [RECALL]
  - press [STORE]
  - press [PAUSE/LNR].

Memory recall state

Repertory numbers can be dialled-out after or before entering manual dialling, last number redial and by entering the memory locations in successive order.

The stored numbers can be dialled by the following procedures:

- press [MRC]
- press one of the numeric keys [0] to [9], corresponding to the memory location

or

- press one of the direct memory keys ([M1] to [M10]).

Program state

The program mode can be entered from the conversation (on-line) mode.

Pressing the [STORE] key in this state puts the TEA1069N in the program mode. The program state can be left by going on-hook (by putting the handset on the cradle or pressing the [HOOK] key), the program mode is interrupted and nothing is stored, or by ending the store procedures resulting in a proper store of the programmed item.

- Programming repertory numbers.

  Storing of a new repertory number including access pauses, tone switch and register recall can be done by the following procedures:

  - press [STORE]
  - press to-be-stored sequence of the digits [0] to [9], [PAUSE/LNR], [∗/T] or [RECALL]
  - press [MRC]
  - press one of the numeric keys [0] to [9], corresponding to the memory location

  or

  - press [STORE]
  - press to-be-stored sequence of the digits [0] to [9], [PAUSE/LNR], [∗/T] or [RECALL]
  - press [M1] to [M10].

  For storing the redial number in repertory use:

  - press [STORE]
  - press [PAUSE/LNR]
  - press [MRC]
  - press one of the numeric keys [0] to [9], corresponding to the memory location

  or

  - press [STORE]
  - press [PAUSE/LNR]
  - press [M1] to [M10].

  If the keyboard described in Fig.16 is selected by the KBS diode option, repertory memory place [M1] = [MRC] + [1] to [M10] = [MRC] + [0], thus the set has 10 repertory numbers which can be selected via two different ways.

  If the keyboard described in Fig.18 is selected by the KBS diode option repertory memory place [MRC] + [0] to [MRC] + [9] and [M1], [M2] and [M3] are different repertory numbers, thus this set has in total 13 repertory numbers.

- Memory overflow.

  A maximum of 224 digits can be stored in the repertory memories. When the maximum is reached, no keytone is generated when trying to store more digits. The store procedure is cancelled automatically.

- Clear repertory number.

  Clearing a memory location is possible via the same procedure as for storing a number, except no telephone number is entered, thus one of the following sequences must be used:

  - press [STORE]
  - press [MRC]
  - press one of the numeric keys [0] to [9], corresponding to the memory location

  or

  - press [STORE]
  - press [M1] to [M10].

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

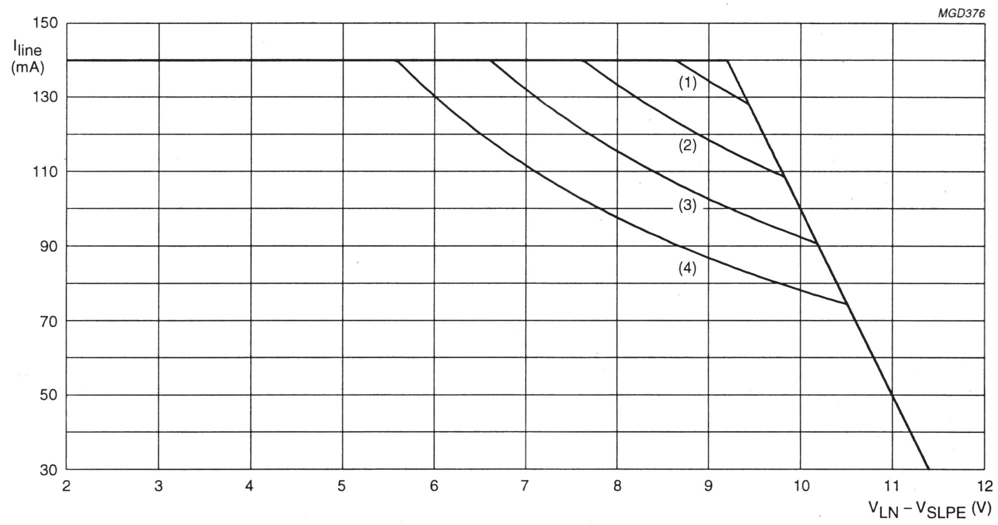
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{line}	line current	R9 = 20 Ω; note 1	–	140	mA
I_{EE}	ground supply current through V_{EE}		–	50	mA
P_{tot}	total power dissipation	R9 = 20 Ω; note 2	–	400	mW
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	IC storage temperature		–40	+125	°C
T_j	junction temperature		–	+90	°C
Speech part					
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
V_{CC}	input voltage on pin V_{CC}		–	12	V
V_i	input voltage on pins 1 to 7, 37, 38, 39, 41, 42		$V_{EE} - 0.7$	$V_{CC} + 0.7$	V
Dialler/ringer part					
V_{DD}	supply voltage		–0.7	+7	V
V_i	input voltages on pins 8 to 22, 24, 26 to 35		$V_{EE} - 0.7$	$V_{DD} + 0.7$	V
I_i	DC input current on pins 8 to 22, 24, 26 to 35		–10	+10	mA
I_o	DC output current on pins 8 to 22, 24, 26 to 35		–10	+10	mA
P_o	power dissipation per output on pins 8 to 22, 24, 26 to 35		–	30	mW

Notes

1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Fig.25).
2. Calculated for the maximum ambient temperature specified (T_{amb} = 70 °C) and a maximum junction temperature of 90 °C.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air mounted on glass epoxy board 28.5 × 19.1 × 1.5 mm	42 (typical)	K/W



(1) T_{amb} = 40 °C; P_{tot} = 1000 mW.
(2) T_{amb} = 50 °C; P_{tot} = 800 mW.
(3) T_{amb} = 60 °C; P_{tot} = 600 mW.
(4) T_{amb} = 70 °C; P_{tot} = 400 mW.

Note: calculations based upon negligible dialler and ringer parts output power (null port sink current).

Fig.25 Safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 1 kHz; V_{DD} = 3 V; f_{xtal} = 3.579545 MHz; T_{amb} = 25 °C; unless otherwise specified.

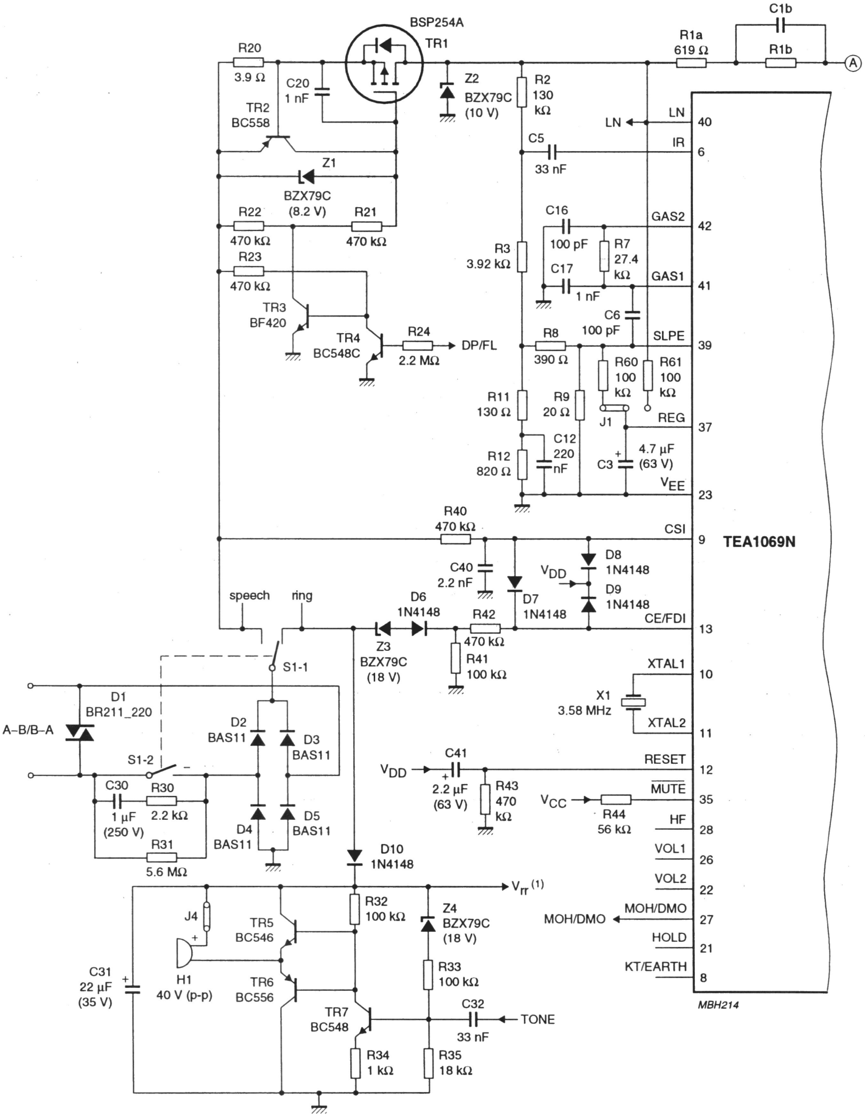
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Speech part						
SUPPLIES LN AND V_{CC} (PINS 40 AND 36)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	MIC inputs open-circuit				
		I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	1.9	–	V
		I_{line} = 15 mA	3.55	4.0	4.25	V
		I_{line} = 100 mA	4.9	5.7	6.5	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–	−0.3	–	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	–	3.5	–	V
		R_{VA} (REG to SLPE) = 39 kΩ	–	4.5	–	V
I_{CC}	supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; $\overline{MUTE}$ = LOW				
		I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
MICROPHONE INPUTS MIC– AND MIC+ (PINS 3 AND 4)						
$\lvert Z_i \rvert$	input impedance					
	differential	between MIC– and MIC+	–	64	–	kΩ
	single-ended	MIC– or MIC+ to V_{EE}	–	32	–	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain MIC+ or MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	50.5	52.0	53.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +70 °C	–	±0.2	–	dB
DTMF INPUT (PIN 7)						
$\lvert Z_i \rvert$	input impedance		–	20.7	–	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.0	25.5	27.0	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +70 °C	–	±0.2	–	dB
GAIN ADJUSTMENT INPUTS GAS1 AND GAS2 (PINS 41 AND 42)						
ΔG_v	transmitting amplifier gain variation by adjustment of R7 between GAS1and GAS2		−8	–	0	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SENDING AMPLIFIER OUTPUT LN (PIN 40)						
$V_{LN(rms)}$	output voltage (RMS value)	THD = 10%				
		I_{line} = 4 mA	–	0.8	–	V
		I_{line} = 15 mA	1.7	2.3	–	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	–	–69	–	dBmp
RECEIVING AMPLIFIER INPUT IR (PIN 6)						
$\lvert Z_i \rvert$	input impedance		–	21	–	kΩ
RECEIVING AMPLIFIER OUTPUT QR (PIN 1)						
$\lvert Z_o \rvert$	output impedance		–	4	–	Ω
G_v	voltage gain from IR to QR	I_{line} = 15 mA; R_L = 300 Ω (from pin 9 to pin 4)	29.5	31	32.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +70 °C	–	±0.2	–	dB
$V_{o(rms)}$	output voltage (RMS value)	THD = 2%; sine wave drive; R4 = 100 kΩ; I_{line} = 15 mA; I_p = 0 mA				
		R_L = 150 Ω	0.22	0.33	–	V
		R_L = 450 Ω	0.3	0.48	–	V
		THD = 10%; R4 = 100 kΩ; R_L = 150 Ω; I_{line} = 4 mA	–	15	–	mV
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve); R_L = 300 Ω	–	50	–	µV
GAIN ADJUSTMENT INPUT GAR (PIN 2)						
ΔG_v	receiving amplifier gain variation by adjustment of R4 between GAR and QR		–11	–	0	dB
$\overline{\text{MUTE}}$ (PIN 35) GAIN REDUCTION						
ΔG_v	MIC+ or MIC– to LN	$\overline{\text{MUTE}}$ = LOW	–	70	–	dB
G_v	voltage gain from DTMF to QR	R4 = 100 kΩ; R_L = 300 Ω	–	–17	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AUTOMATIC GAIN CONTROL INPUT AGC (PIN 38)						
ΔG_v	gain control range (controlling the gain from IR to QR and the gain from MIC+, MIC− to LN)	R6 = 110 kΩ (between AGC and V_{EE}); I_{line} = 70 mA	–	−5.8	–	dB
I_{lineH}	highest line current for maximum gain	R6 = 110 kΩ	–	23	–	mA
I_{lineL}	lowest line current for minimum gain	R6 = 110 kΩ	–	61	–	mA
Dialler part						
V_{DD} (PIN 25)						
V_{DD}	supply voltage		2.5	–	6.0	V
$V_{DD(MR)}$	memory retention voltage		1.0	–	6.0	V
I_{DD}	supply current	DTMF generator **off**	–	0.3	0.6	mA
		DTMF generator **on**	–	0.9	1.8	mA
$I_{DD(MR)}$	memory retention current	standby state, V_{DD} = 1.8 V	–	1.2	–	µA
V_{POR}	power-on reset trip level		1.5	2.0	2.5	V
INPUTS/OUTPUTS (PINS 9, 12 TO 21, 29 TO 34)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage	$V_{EE} < V_I < V_{DD}$	−1	–	+1	µA
I_{OL}	port sink current LOW	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
I_{OH}	port pull-up source current HIGH (not valid for pin 33)	V_{DD} = 3 V; V_O = 2.7 V	10	20	–	µA
		V_{DD} = 3 V; V_O = 0 V	–	100	300	µA
$\overline{\text{MUTE}}$ (PIN 35)						
I_{OL}	port sink current LOW	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
OUTPUTS (PINS 8, 22, 26 TO 28)						
I_{OL}	port sink current LOW	V_{DD} = 3 V; V_O = 0.4 V	0.7	8	–	mA
I_{OH}	port push-pull source current HIGH	V_{DD} = 3 V; V_O = 2.6 V	0.7	4	–	mA
OSCILLATOR (PINS 10 AND 11)						
g_m	transconductance		0.2	0.4	1.0	mA/V
R_f	feedback resistor		0.3	1.0	3.0	MΩ
CE/FDI (PIN 13)						
t_{rd}	reset delay time		–	280	–	ms
KEYBOARD (PINS 14 TO 19 AND 29 TO 33)						
t_d	keyboard debounce time		–	20	–	ms
t_{ap}	access pause time	diode APT **off**	–	2	–	s
		diode APT **on**	–	4	–	s

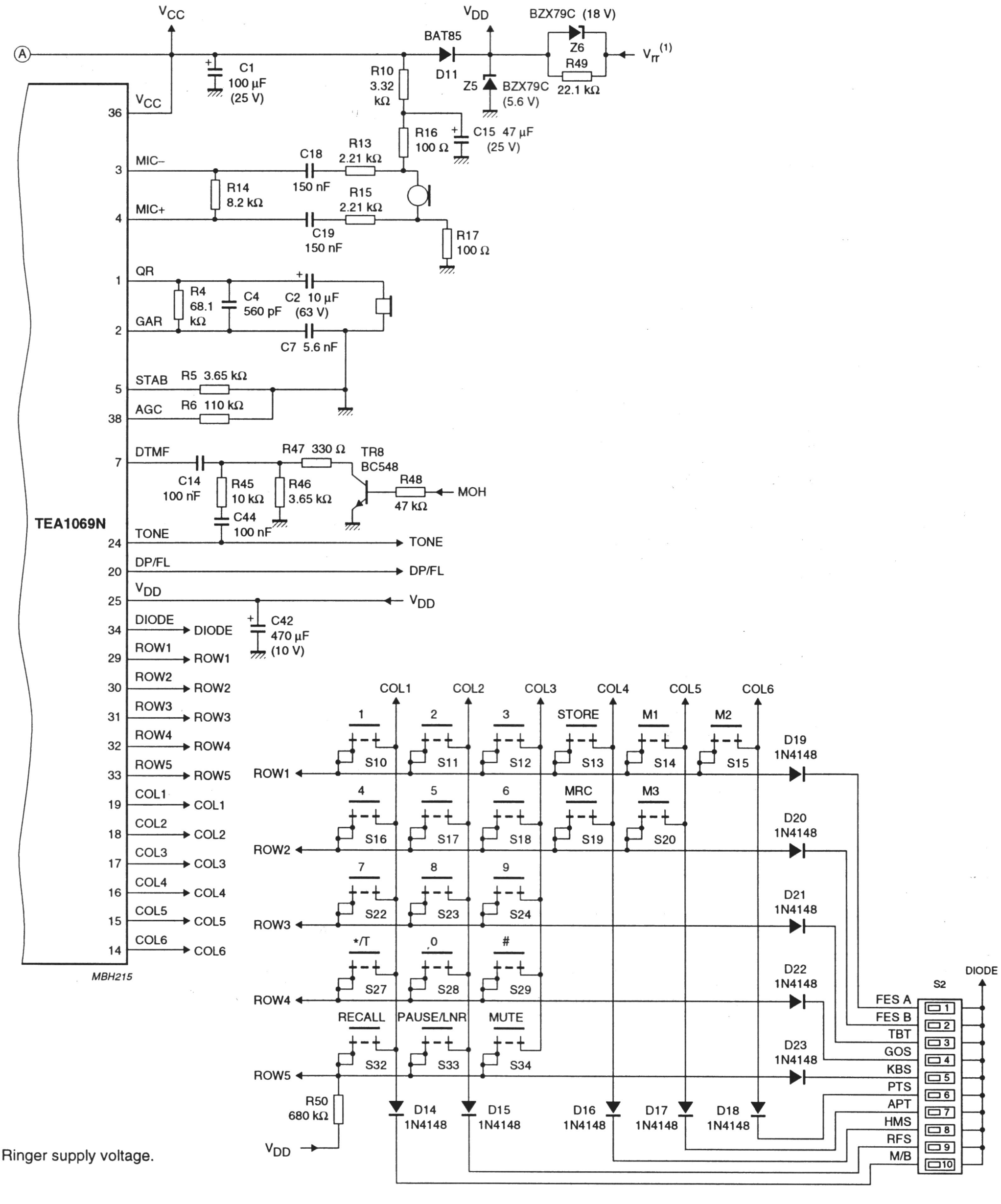
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DP/FL OUTPUT (PIN 20)						
t_{idp}	interdigit pause time		–	840	–	ms
$t_{holdover}$	mute hold-over time		–	40	–	ms
t_m	make time	diode M/S **off**	–	40	–	ms
		diode M/S **on**	–	33	–	ms
t_b	break time	diode M/S **off**	–	60	–	ms
		diode M/S **on**	–	66	–	ms
t_{rc}	recall time using flash	diode FES A **off**, FES B **off**	–	100	–	ms
		diode FES A **on**, FES B **off**	–	270	–	ms
		diode FES A **off**, FES B **on**	–	600	–	ms
t_{ea}	recall time using earth	diode FES A **on**, FES B **on**	–	400	–	ms
TONE OUTPUT (PIN 24)						
t_t	burst time	diode TBT **off**	–	85	–	ms
		diode TBT **on**	–	100	–	ms
t_p	pause time	diode TBT **off**	–	85	–	ms
		diode TBT **on**	–	100	–	ms
$\Delta f/f$	frequency deviation		–0.6		+0.6	%
$V_{HG(rms)}$	HGF voltage (RMS value)		158	181	205	mV
$V_{LG(rms)}$	LGF voltage (RMS value)		125	142	160	mV
V_{DC}	DC voltage level		–	$\frac{1}{2}V_{DD}$	–	V
$\lvert Z_o \rvert$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion		–	–25	–	dB
Ringer part						
f_{ringL}	ringer detection LOW frequency	diode RFS **off**	–	40	–	Hz
		diode RFS **on**	–	29	–	Hz
f_{ringH}	ringer detection HIGH frequency	diode RFS **off**	–	120	–	Hz
		diode RFS **on**	–	146	–	Hz
t_{rrd}	ringer response delay	<1.5 frequency cycle	–	–	150	ms

APPLICATION INFORMATION


BSP254A
TR1
R20
3.9 Ω
C20
1 nF
TR2
BC558
Z2
BZX79C
(10 V)
R2
130 kΩ
C1b
R1a
619 Ω
R1b
Ⓐ
LN
LN
40
IR
6
C5
33 nF
Z1
BZX79C
(8.2 V)
R22
470 kΩ
R21
470 kΩ
R23
470 kΩ
C16
100 pF
R7
27.4 kΩ
GAS2
42
R3
3.92 kΩ
C17
1 nF
GAS1
41
TR3
BF420
TR4
BC548C
R24
2.2 MΩ
DP/FL
C6
100 pF
R8
390 Ω
SLPE
39
R60
100 kΩ
R61
100 kΩ
R11
130 Ω
R9
20 Ω
J1
REG
37
C12
220 nF
R12
820 Ω
C3
4.7 µF
(63 V)
V_{EE}
23
R40
470 kΩ
CSI
9
TEA1069N
C40
2.2 nF
V_{DD}
D8
1N4148
D9
1N4148
speech
ring
D6
1N4148
R42
470 kΩ
D7
1N4148
CE/FDI
13
Z3
BZX79C
(18 V)
R41
100 kΩ
S1-1
XTAL1
10
X1
3.58 MHz
XTAL2
11
D1
BR211_220
A-B/B-A
D2
BAS11
D3
BAS11
S1-2
C41
V_{DD}
2.2 µF
(63 V)
R43
470 kΩ
RESET
12
MUTE
35
V_{CC}
R44
56 kΩ
HF
28
C30
1 µF
(250 V)
R30
2.2 kΩ
D4
BAS11
D5
BAS11
R31
5.6 MΩ
D10
1N4148
VOL1
26
VOL2
22
V_{rr} (1)
J4
TR5
BC546
R32
100 kΩ
Z4
BZX79C
(18 V)
MOH/DMO
MOH/DMO
27
HOLD
21
KT/EARTH
8
C31
22 µF
(35 V)
H1
40 V (p-p)
TR6
BC556
R33
100 kΩ
MBH214
TR7
BC548
C32
33 nF
TONE
R34
1 kΩ
R35
18 kΩ

(1) Ringer supply voltage.

Fig.26 Basic application diagram (continued in Fig.27).


A
VCC
C1
100 μF
(25 V)
VDD
BAT85
D11
BZX79C (18 V)
Z6
R49
22.1 kΩ
Vrr(1)
Z5
BZX79C
(5.6 V)
R10
3.32
kΩ
R16
100 Ω
C15 47 μF
(25 V)
VCC
36
MIC–
3
C18
150 nF
R13
2.21 kΩ
R14
8.2 kΩ
MIC+
4
R15
2.21 kΩ
C19
150 nF
R17
100 Ω
QR
1
R4
68.1
kΩ
C4
560 pF
C2 10 μF
(63 V)
GAR
2
C7 5.6 nF
STAB
5
R5 3.65 kΩ
AGC
38
R6 110 kΩ
DTMF
7
C14
100 nF
R45
10 kΩ
R46
3.65 kΩ
R47 330 Ω
TR8
BC548
R48
47 kΩ
MOH
C44
100 nF
TEA1069N
TONE
24
TONE
DP/FL
20
DP/FL
VDD
25
VDD
C42
470 μF
(10 V)
DIODE
34
DIODE
ROW1
29
ROW1
ROW2
30
ROW2
ROW3
31
ROW3
ROW4
32
ROW4
ROW5
33
ROW5
COL1
19
COL1
COL2
18
COL2
COL3
17
COL3
COL4
16
COL4
COL5
15
COL5
COL6
14
COL6
MBH215
COL1
COL2
COL3
COL4
COL5
COL6
1
2
3
STORE
M1
M2
S10
S11
S12
S13
S14
S15
ROW1
D19
1N4148
4
5
6
MRC
M3
S16
S17
S18
S19
S20
ROW2
D20
1N4148
7
8
9
S22
S23
S24
ROW3
D21
1N4148
*/T
0
#
S27
S28
S29
ROW4
D22
1N4148
RECALL
PAUSE/LNR
MUTE
S32
S33
S34
ROW5
D23
1N4148
R50
680 kΩ
VDD
D14
1N4148
D15
1N4148
D16
1N4148
D17
1N4148
D18
1N4148
DIODE
S2
FES A
FES B
TBT
GOS
KBS
PTS
APT
HMS
RFS
M/B
1
2
3
4
5
6
7
8
9
10

(1) Ringer supply voltage.

Fig.27 Basic application diagram (continued from Fig.26).

Supply circuit with power-down for telephone set peripherals

TEA1081

FEATURES

- High input impedance for audio signals
- Low DC series resistance
- High output current
- Large audio signal handling capability
- Low distortion
- Two modes of operation:
  - output voltage that follows the DC line voltage
  - regulated output voltage
- Power-down input
- Low number of external components.

GENERAL DESCRIPTION

The TEA1081 is an integrated circuit for use in line-powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaker facilities.

The IC uses a part of the surplus line current normally drawn by the voltage regulator of the speech/transmission circuit. A power-down function isolates the IC from its load and reduces the input current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_O	DC output voltage		2.0	–	10.0	V
$\Delta V_{LN\text{-}O}$	voltage drop from line to output	$I_O = 0$ mA	–	0.5	–	V
R_S	internal series resistance		–	20	–	Ω
I_O	output current (pin 7)	$V_{LN} = 4$ V				
	TEA1081		–	–	30	mA
	TEA1081T		–	–	20	mA
$V_{LN(rms)}$	AC line voltage (RMS value)	$V_{LN} = 4$ V; $I_O = 15$ mA; THD = 2%	–	1.5	–	V
I_{INT}	internal supply current	$V_{LN} = 4$ V; $I_O = 0$ mA; PD = LOW; $V_{SP} = V_O$	–	0.8	1.4	mA
T_{amb}	operating ambient temperature		–25	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1081	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1081T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

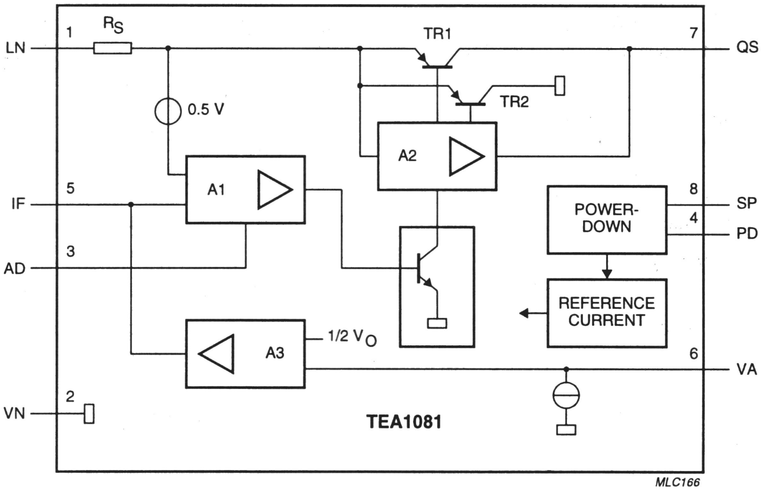

LN
IF
AD
VN
1
5
3
2
RS
0.5 V
A1
A3
1/2 VO
TR1
TR2
A2
POWER-DOWN
REFERENCE CURRENT
TEA1081
7
8
4
6
QS
SP
PD
VA
MLC166

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
VN	2	negative line terminal
AD	3	amplifier decoupling
PD	4	power-down input
IF	5	low-pass filter input
VA	6	output voltage adjustment
QS	7	power supply output
SP	8	supply input; power-down circuit

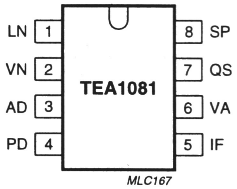

LN 1
VN 2
AD 3
PD 4
TEA1081
8 SP
7 QS
6 VA
5 IF
MLC167

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TEA1081 is a supply interface between telephone line and peripheral devices in the telephone set. The high input impedance of the circuit allows direct connection to the telephone line (via a diode bridge). An inductor function is obtained by amplifier A1, resistor R_S (see Fig.1) and an external low-pass RC filter.

Under the control of amplifier A2, transistor TR1 supplies peripheral devices and transistor TR2 minimizes line signal distortion by momentarily diverting input current to ground whenever the instantaneous value of the line voltage drops below the output voltage.

Internal circuits are biased by a temperature and line voltage compensated reference current source.

The power-down circuit isolates the supply circuit from external circuitry.

Line terminals: LN and VN (pins 1 and 2)

The input terminals LN and VN can be connected directly to the line. The minimum DC line voltage required at the input is expressed by formula (1); see also Table 1.

$$V_{LN} = I_1 \times R_S + V_{LNmin} + V_{LN(P)} \text{ (V)} \qquad (1)$$

Table 1 Explanation of formula (1).

SYMBOL	DESCRIPTION
I_1	input current
R_S	internal series resistance
V_{LNmin}	minimum instantaneous line voltage (1.4 V at I_O = 5 mA)
$V_{LN(P)}$	required peak level of AC line voltage

The internal current (I_{INT}) at I_O = 0 mA is typically 0.8 mA at V_{LN} = 4 V and reaches a maximum of 1.4 mA at V_{LN} = 12 V.

Supply terminals: QS and VA (pins 7 and 6)

Peripheral devices are supplied from QS (pin 7). Two modes of output voltage regulation are available.

OUTPUT VOLTAGE FOLLOWS LINE VOLTAGE (SEE FIG.3)

The TEA1081 operates in this mode when there is no external resistor (R_V) between QS and VA (see Fig.6).

The output voltage follows the line voltage and is expressed by formula (2); see also Table 2.

$$V_O = V_{LN} - (I_1 \times R_S + 0.5) \text{ (V)} \qquad (2)$$

Table 2 Explanation of formula (2).

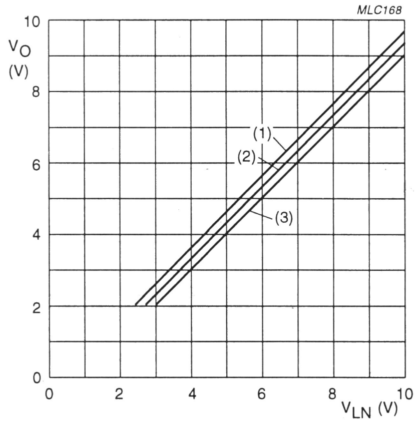
SYMBOL	DESCRIPTION
V_{LN}	line voltage
I_1	input current
R_S	internal series resistance

REGULATED OUTPUT VOLTAGE (SEE FIG.4)

The circuit operates in this mode when an external resistor (R_V) is connected between QS and VA (see Fig.6).

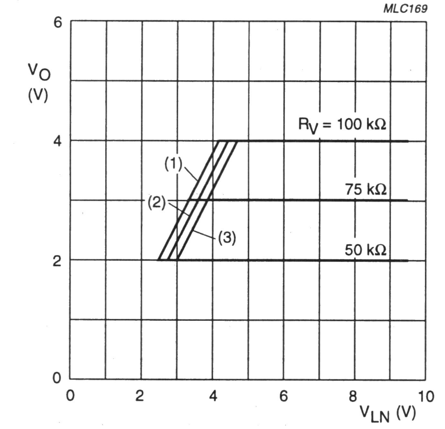
The output voltage is held constant at $V_O = 2 \times I_6 \times R_V$ (V) as soon as the line voltage $V_{LN} > (2 \times I_6 \times R_V + I_1 \times R_S + 0.5)$ (V)

The control current I6 is typically 20 μA.



Application without R_V.
(1) I_1 = 5 mA.
(2) I_1 = 20 mA.
(3) I_1 = 30 mA; not valid for TEA1081T.

Fig.3 Output voltage as a function of line voltage.



R_V connected between QS and VA.
(1) I_1 = 5 mA.
(2) I_1 = 20 mA.
(3) I_1 = 30 mA; not valid for TEA1081T.

Fig.4 Output voltage as a function of line voltage.

Input and output currents I_1 and I_O (pins 1 and 7)

The maximum available current into pin 1 (I_1) is determined by:

- The minimum line current ($I_{LINEmin}$) that is available for the telephone set
- The specified minimum input current (I_{LNmin}) for the speech/transmission circuit.

That is $I_{1max} = I_{LINEmin} - I_{LNmin}$.

At $V_{LN(rms)}$ < 150 mV, the input current I_1 is approximately:

$I_1 = I_{INT} + k \times I_O$ (mA)

Where:

I_{INT} = internal supply current (0.8 mA at V_{LN} = 4 V);

k = correction factor (k < 1.1 for the specified output current range).

With large line signals the instantaneous line voltage may drop below V_O + 0.4 V. Normally (when $V_{LN} > V_O + 0.4$ V), instantaneous current flows from LN to QS (pin 1 to pin 7) to the output load.

When $V_{LN} < V_O + 0.4$ V, the instantaneous current is diverted to pin 2 to prevent distortion of the line signal.

Input current at $V_{LN(rms)}$ = 1 V and without R_V approximates to:

$I_1 = I_{INT} + 2 \times I_O$ (mA)

The maximum supply current (within the specified output current limits) available for peripheral devices is shown by:

$$I_{Omax} = \frac{I_{LINEmin} - I_{LNmin} - I_{INT}}{2}$$

Where:

$I_{LINEmin}$ is the minimum line current of the telephone set;

I_{LNmin} is the specified minimum input current of the speech/transmission circuit.

Input low-pass filter: IF (pin 5)

The input impedance between LN and VN at audio frequencies is determined by the filter elements C_L (between pins 1 and 5), R_L (between pins 5 and 7) and the internal resistor R_S (typical value 20 Ω).

At audio frequencies the TEA1081 behaves as an inductor of the value $L_I = C_L \times R_L \times R_S$ (H). The typical value of L_I at C_L = 2.2 µF and R_L = 100 kΩ is 4.4 H.

Amplifier decoupling: AD (pin 3)

To ensure stability, a 68 pF decoupling capacitor is required between AD (pin 3) and LN (pin 1).
If I_{Omin} < 1.5 mA, a 47 pF capacitor has to be added between AD (pin 3) and VA (pin 6).

Power-down inputs: PD and SP (pins 4 and 8)

During pulse dialling or register recall, or if the input current to pin 1 is insufficient to maintain the output current, the supply to peripheral devices can be switched off by activating the PD input at pin 4. With PD = HIGH, the input current is reduced to 40 µA (typ.) at V_{LN} = 4 V and the internal circuits are isolated from the load at QS (pin 7).

The power-down circuit is supplied via the SP input (pin 8). SP can be wired to QS in conditions where $V_O > V_{SPmin}$ during line interruptions. When $V_O < V_{SPmin}$, SP should be wired to an external supply point (e.g. to V_{CC} of the TEA1060 family circuit).

When power-down is not required, the PD and SP inputs can be left open-circuit.

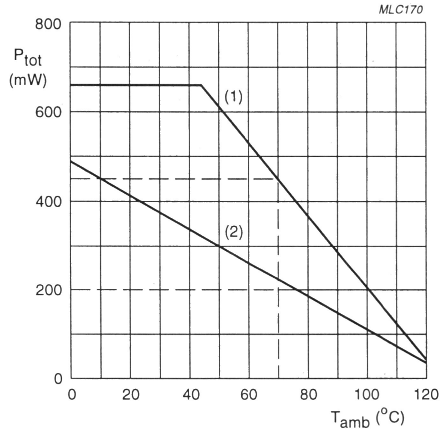
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage	continuous	–	12	V
		during switch-on or line interruptions	–	12.5	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	12 Ω resistor in series with pin 1	–	28	V
V_I	input voltage (all other terminals)		$V_{VN} - 0.5$	$V_{LN} + 0.5$	V
I_1	DC input current				
	TEA1081		–	120	mA
	TEA1081T		–	80	mA
I_I	input current (all other terminals)		–1	+1	mA
P_{tot}	total power dissipation		see Fig.5		
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1081	120	K/W
	TEA1081T (mounted on a printed-circuit board of 50 × 50 × 1.5 mm)	260	K/W



(1) TEA1081.
(2) TEA1081T.

Fig.5 Power derating curves.

CHARACTERISTICS

V_{LN} = 4 V; $V_{LN(rms)}$ = 100 mV; I_O = 5 mA; f = 300 to 3400 Hz; R_L = 100 kΩ; C_L = 2.2 μF; R_V = 75 kΩ; T_{amb} = 25 °C; unless otherwise specified; see Fig.6.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_{LNmin}	minimum instantaneous line voltage		–	–	1.4	V
V_{LNmax}	maximum instantaneous line voltage		12.0	–	–	V
Characteristics with R_V = 75 kΩ connected between pins 6 and 7 and C_L = 10 μF						
I_1	input current (pin 1)	$V_{LN(rms)}$ = 0 V	–	5.8	–	mA
		$V_{LN(rms)}$ = 1.5 V; I_O = 15 mA	–	30	–	mA
V_O	output voltage (pin 7)		–	3.0	–	V
ΔV_O	variation of output voltage over the ranges of:					
	line voltage	V_{LN} = 4 to 6 V	–	100	–	mV
	temperature	T_{amb} = +25 to −25 °C	–	−100	–	mV
	temperature	T_{amb} = +25 to +75 °C	–	−100	–	mV
	output current	I_O = 5 to 20 mA	–	−100	–	mV
I_6	control current (pin 6)		–	20	–	μA
Characteristics without R_V						
I_1	input current (pin 1)	$V_{LN(rms)}$ = 0 V	–	6.0	–	mA
		$V_{LN(rms)}$ = 1.5 V; I_O = 15 mA	–	31	–	mA
ΔV_{LN-O}	voltage drop from line to output	I_O = 0 mA	–	0.5	–	V
		I_O = 15 mA; $V_{LN(rms)}$ = 1.5 V	–	1.1	–	V
I_O	output current (pin 7)					
	TEA1081		–	–	30	mA
	TEA1081T		–	–	20	mA
R_S	internal series resistance		–	20	–	Ω
I_{INT}	internal supply current	I_O = 0 mA; PD = LOW; V_{SP} = V_O	–	0.8	1.4	mA
		I_O = 0 mA; PD = HIGH (note 1); V_{SP} > 2 V	–	40	60	μA
THD	total harmonic distortion	$V_{LN(rms)}$ = 1.5 V	–	–	2	%
BRL	balance return loss	600 Ω reference	25	–	–	dB
$V_{LN(2H)}$	second harmonic level of line voltage	f = 500 Hz; V_{LN} = 0 dBm; Z_{line} = 600 Ω	–	−58	–	dBm
$V_{LN(3H)}$	third harmonic level of line voltage	f = 500 Hz; V_{LN} = 0 dBm; Z_{line} = 600 Ω	–	−60	–	dBm
$V_{ni(rms)}$	noise voltage on input terminal (RMS value)	$V_{LN(rms)}$ = 0 V; R_L = 600 Ω; P53 curve	–	−83	–	dBmp
Power-down input (pin 4)						
V_{IL}	LOW level input voltage		–	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{SP}	V
I_4	input current		–	–	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (pin 8)						
V_8	supply voltage for power-down		2	–	V_{LN}	V
I_8	supply current to power-down circuit	$V_8 = 3$ V	–	–	70	μA

Note

1. Power-down circuit supplied via external source.

APPLICATION INFORMATION

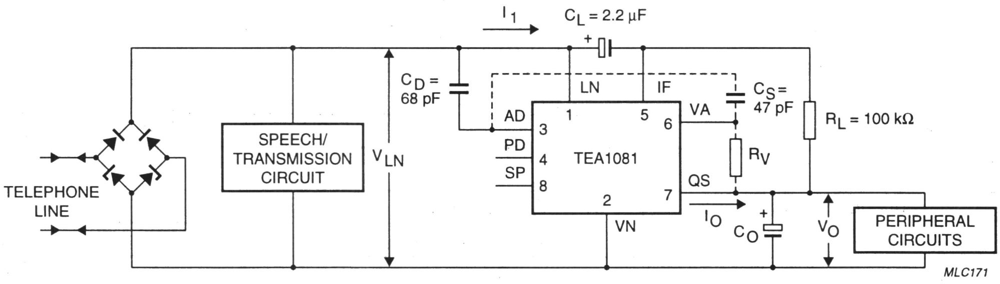

I1
CL = 2.2 μF
+
CD = 68 pF
LN
IF
CS = 47 pF
RL = 100 kΩ
AD
PD
SP
3
4
8
1
5
6
7
2
TEA1081
VA
QS
VN
RV
IO
CO
+
VO
VLN
SPEECH/ TRANSMISSION CIRCUIT
TELEPHONE LINE
PERIPHERAL CIRCUITS
MLC171

Fig.6 Application diagram.

Call progress monitor for line powered telephone sets

TEA1083/TEA1083A

FEATURES

- Internal supply
  - Optimum current split-up
    - . Low constant current (adjustable) in transmission IC
    - . Nearly all line current available for monitoring
  - Stabilized supply voltage
- Loudspeaker amplifier with a fixed gain of 35 dB
- Volume controled by potentiometer
- Power-down input (TEA1083A only)
- Loudspeaker enable input.

GENERAL DESCRIPTION

The TEA1083/83A is a bipolar IC which has been designed for use in line powered telephone sets. It is intended to offer a monitoring facility of the line signal via a loudspeaker during on-hook dialling. The TEA1083/83A is intended for use in conjunction with a transmission circuit of the TEA1060 family.

The device uses a part of the available line current via the internal supply circuit.

The loudspeaker amplifier, which consists of a preamplifier and a power amplifier, amplifies the received line signals from the transmission circuit when enabled via the LSE input. The loudspeaker amplifier can also be used to amplify dialling tones from the dialler IC.

The power amplifier contains a push-pull output stage to drive the loudspeaker in a Single Ended Load (SEL) configuration.

The internal voltage stabilizer can be used to supply external devices.

By activating the power-down (PD) input of the TEA1083A, the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		3.0	–	120	mA
V_{BB}	stabilized supply current		–	2.95	–	V
I_{SUP}	current consumption	PD = HIGH; TEA1083A only	–	50	–	µA
G_v	voltage gain of loudspeaker amplifier		–	35	–	dB
I_{SUP}	minimum input current	P_O = 10 mW (typ) into 50 Ω	–	10	–	mA
T_{amb}	operating ambient temperature range		–25	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1083	8	DIL	plastic	SOT97D
TEA1083A	16	DIL	plastic	SOT38
TEA1083AT	16	SOL	plastic	SOT162AG

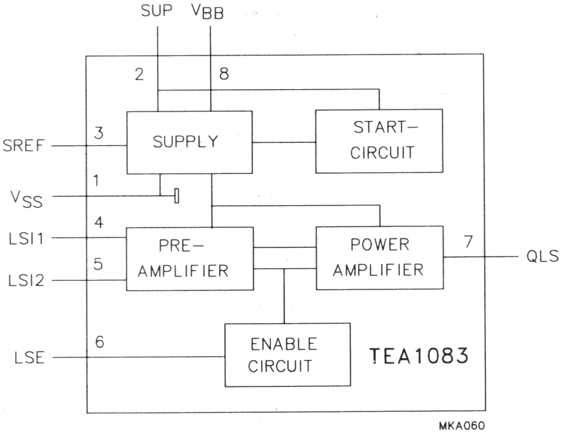

SUP
VBB
2
8
SUPPLY
START–
CIRCUIT
SREF
3
1
VSS
4
LSI1
PRE–
AMPLIFIER
POWER
AMPLIFIER
7
QLS
5
LSI2
6
LSE
ENABLE
CIRCUIT
TEA1083
MKA060

Fig.1 Block diagram (TEA1083).

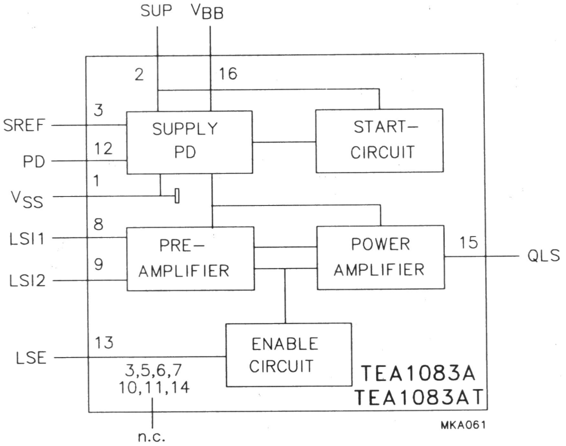

SUP
VBB
2
16
3
SREF
SUPPLY
PD
START–
CIRCUIT
12
PD
1
VSS
8
LSI1
PRE–
AMPLIFIER
POWER
AMPLIFIER
15
QLS
9
LSI2
13
LSE
ENABLE
CIRCUIT
3,5,6,7
10,11,14
TEA1083A
TEA1083AT
n.c.
MKA061

Fig.2 Block diagram (TEA1083A/AT).

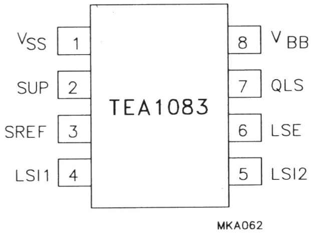

V_SS
1
SUP
2
SREF
3
LSI1
4
TEA1083
8
V BB
7
QLS
6
LSE
5
LSI2
MKA062

Fig.3 Pin configuration (TEA1083).

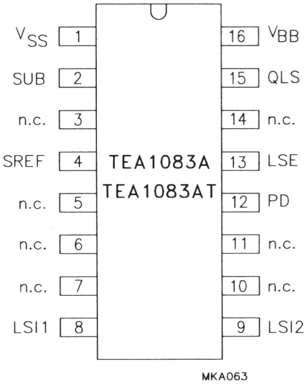

V_SS
1
SUB
2
n.c.
3
SREF
4
n.c.
5
n.c.
6
n.c.
7
LSI1
8
TEA1083A
TEA1083AT
16
V_BB
15
QLS
14
n.c.
13
LSE
12
PD
11
n.c.
10
n.c.
9
LSI2
MKA063

Fig.4 Pin configuration (TEA1083A/AT).

PINNING

SYMBOL	PIN DIL16	PIN DIL8	DESCRIPTION
V_{SS}	1	1	negative supply terminal
SUP	2	2	positive supply terminal
n.c.	3	–	not connected
SREF	4	3	supply reference input
n.c.	5	–	not connected
n.c.	6	–	not connected
n.c.	7	–	not connected
LSI1	8	4	loudspeaker amplifier input 1
LSI2	9	5	loudspeaker amplifier input 2
n.c.	10	–	not connected
n.c.	11	–	not connected
PD	12	–	power-down input
LSE	13	6	loudspeaker enable input
n.c.	14	–	not connected
QLS	15	7	loudspeaker amplifier output
V_{BB}	16	8	stabilized supply voltage

Table 1 Comparison of the TEA108X family.

PRODUCT	CONDITIONS	TEA1083	TEA1083A	TEA1085/85A
Application area	note 1	call progress monitoring		listening-in
PD facility		–	X	X
MUTE or LSE facility	note 2	X	X	X
Dynamic limiter		–	–	X
Howling limiter		–	–	X
V_{BB} setting		–	–	X
SEL	note 3	X	X	X
BTL	note 3	–	–	X
Number of pins	note 4	8	16	24

Notes to Table 1

1. A call progress monitor is recommended by the European Telecommunications Standards Institute (ETSI) for telephone sets with automatic on-hook dialling facilities so that audible, or visual, progress of a call attempt can be monitored. In accordance with the ETSI (at a frequency of 440 Hz and a line level of 20 dBm (600 Ω)), a minimum level of 50 dBA shall be guaranteed at a distance of 50 cm from the set. This corresponds to a minimum level of approximately 100 mV (RMS) ($P_O \geq 0.2$ mW) across a loudspeaker; Philips type AD2071/Z50.

   A listening-in set has to offer the user more facilities e.g. howling limiting to reduce annoying loudspeaker and line signals. Dynamic limiting of the loudspeaker signal, with respect to supply conditions, can also be required. Acoustic output levels for listening-in sets are approximately 70 to 75 dBA. This corresponds to a loudspeaker level of approximately 1 mV (RMS) ($P_O \approx 20$ mW).
2. The MUTE function of the TEA1085A has a logic input; the MUTE function of the TEA1085 has a toggle input.
3. SEL: loudspeaker connected in a single-ended-load configuration

   BTL: loudspeaker connected in a bridge-tied-load configuration
4. Consult the product specification for the package outline/s.

FUNCTIONAL DESCRIPTION

The TEA1083/83A is normally used in conjunction with a transmission circuit of the TEA1060 family. The circuit must be connected between the positive line terminal (pin 2) and pin SLPE of the transmission IC. The transmission characteristics (impedance, gain settings etc) are not affected.
An interconnection between the TEA1083/83A and a member of the TEA1060 family is illustrated in Fig.5.

Supplies SUP, SREF, V_{BB} and V_{SS}

In Fig.6 the line current is divided into I_{TR} for the transmission IC and I_{SUP} for the monitoring circuit TEA1083/83A.

I_{TR} is constant:

$$I_{TR} = V_{int}/R20$$

$$I_{SUP} = I_{line} - I_{CC} - I_{TR}$$

Where:

- V_{int} is an internal temperature compensated reference voltage of 500 mV(typ) between pins SUP and SREF
- R20 is a resistor connected between SUP and SREF
- I_{CC} is the internal current consumption of the TEA106X (approximately 1 mA).

A practical value for resistor R20 is 150 Ω; this produces a current of approximately 3.3 mA(typ) for I_{TR} and I_{SUP} is approximately equal to I_{line} − 4.3 mA.

The circuit stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. Transistor TR2 is used to minimize signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage at V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 2.95 V.
The supply at V_{BB} is decoupled with respect to V_{SS} by a 220 µF capacitor (C20).

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC and V_{int}; thus $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$. The reference voltage of the transmission IC has to be adjusted to a level where $V_{SUP} - V_{BB(max)}$ is greater than 400 mV. The minimum voltage space between SUP and V_{BB} (400 mV) is required to maintain a 'high' efficiency of the internal supply for mean speech levels. $V_{BB(max)}$ is the specified maximum level.

The internal current consumption of the TEA1083/83A (I_{SUPo}) is typically 2.5 mA (where $V_{SUP} - V_{SS} = 3.6$ V). The current I_{SUPo} consists of currents I_{BIAS} (approximately 0.4 mA) for the circuitry connected to SUP and I_{BBo} (approximately 2.1 mA) for the internal circuitry connected to V_{BB} (see Fig.6).

LOUDSPEAKER AMPLIFIER (LSI1/LSI2 and QLS)

The TEA1083/83A has symmetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit (see Fig.5) and/or from the signal output of the DTMF generator via a resistive attenuator.
The attenuation factor must be chosen in accordance with the output levels from the transmission IC and/or DTMF generator and, in accordance with the required output power and permitted signal distortion from the loudspeaker signal.

The output QLS drives the loudspeaker as a single-ended load. The output stage has been optimised for use with a 50 Ω loudspeaker (e.g. Philips type AD2071). The loudspeaker amplifier is enabled when the LSE input goes HIGH. The gain of the amplifier is fixed at 35 dB.

Volume control of the loudspeaker signal can be obtained by using a level control at the input (see Fig.5).

The maximum voltage swing at the QLS output is $V_{O(p-p)} = 2.5$ V (typical with 50 Ω load). The input level V_{LSI} is approximately 16 mV(rms) and the supply current $I_{SUP} > 11$ mA. In this condition the signal is limited by the available voltage space (V_{BB}). Higher input levels and/or lower supply currents will result in an increase of the harmonic distortion due to signal clipping.

With a limit of 2.5 V(p-p), the maximum output swing is dependent on the supply current and loudspeaker impedance. It can be approximated, for low distortions, by the following equation:

$$V_{O(p-p)} = 2 \times (I_{SUP} - I_{SUPO}) \times \pi \times R_{LS}$$

Where;

- $V_{O(p-p)}$ = the peak-to-peak level of the loudspeaker
- R_{LS} = the loudspeaker impedance
- I_{SUPO} = 2.5 mA (typ.)

POWER-DOWN INPUT (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply current to the transmission IC. The capacitor connected to V_{BB} provides the supply for the TEA1083/83A during the supply breaks.

By making the PD input HIGH during the loop break, the requirement on the capacitor is eased and, consequently, the internal current consumption I_{BBO} (see Fig.5) is reduced from 2.1 mA to 400 µA typically. Transistors TR1 and TR2 are inhibited during power-down and the bias current is reduced from approximately 400 µA to approximately 50 µA with V_{SUP} =3.6 V in the following equation:

$$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$$

Where $3.6 < V_{SUP} < V_{BB} + 3$ V

$2V_d$ is the voltage drop across 2 internal diodes (approximately 1.3 V)

Ra is an internal resistor (typical 50 kΩ)

LOUDSPEAKER ENABLE INPUT (LSE)

The LSE input has a pull-down structure. It switches the loudspeaker amplifier, in the monitoring condition, by applying a HIGH level at the input. The amplifier is in the standby condition when LSE is LOW (input open-circuit or connected to V_{SS}.

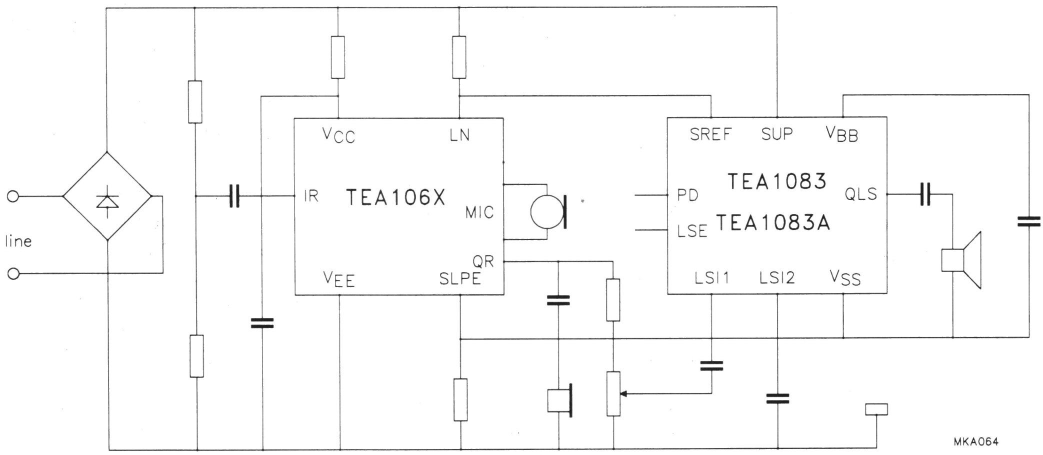

line
VCC
LN
IR
TEA106X
MIC
QR
VEE
SLPE
SREF
SUP
VBB
PD
TEA1083
QLS
LSE
TEA1083A
LSI1
LSI2
VSS
MKA064

Fig.5 Interconnection with a transmission IC of the TEA106X family.

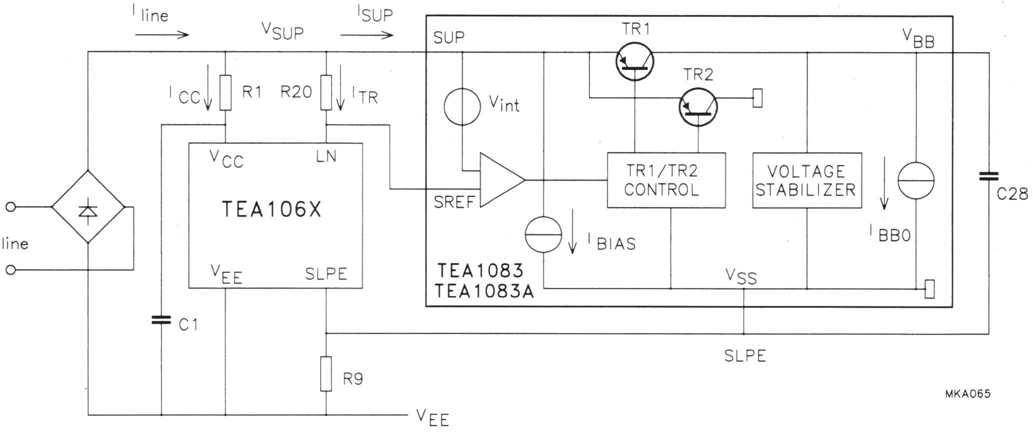

I line
VSUP
ISUP
SUP
TR1
VBB
ICC
R1
R20
ITR
TR2
Vint
VCC
LN
TEA106X
SREF
TR1/TR2 CONTROL
VOLTAGE STABILIZER
C28
line
IBIAS
IBBO
VEE
SLPE
TEA1083
TEA1083A
VSS
C1
SLPE
R9
VEE
MKA065

Fig.6 Supply arrangement.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	Supply voltage				
	continuous		–	12	V
	during switch-on or line interruption		–	13.2	V
V_{SUP}	Repetitive supply voltage from 1 ms to 5 s with 12 Ω current limiting resistor in series with supply		–	28	V
V_{SREF}	Supply reference voltage		V_{SS}–0.5	V_{SUP}+0.5	V
V	Voltage on all other pins		V_{SS}–0.5	V_{BB}+0.5	V
I_{SUP}	Supply current	see Fig.6	–	120	mA
P_{tot}	Total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1083		–	500	mW
	TEA1083A		–	769	mW
	TEA1083AT		–	555	mW
T_{stg}	Storage temperature range		–40	+125	°C
T_{amb}	Operating ambient temperature range		–25	+75	°C
T_j	Junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (TEA1083)	100 K/W
	from junction to ambient in free air (TEA1083A)	65 K/W
	from junction to ambient in free air (TEA1083AT)	90 K/W

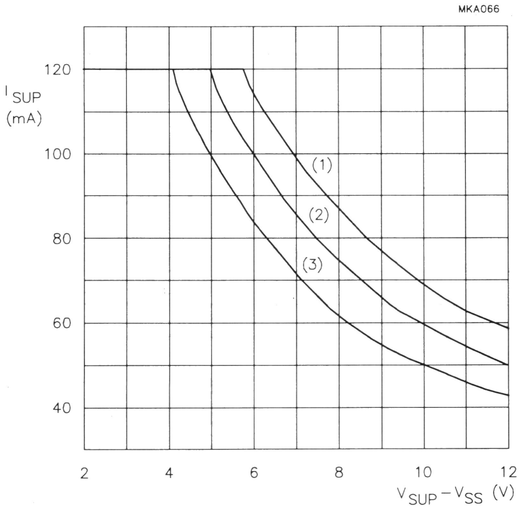


Fig.7 Safe operating area; see Table 2 (TEA1083).

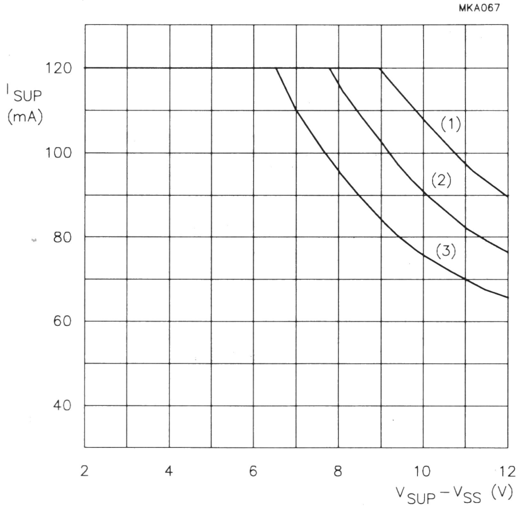


Fig.8 Safe operating area; see Table 3 (TEA1083A).

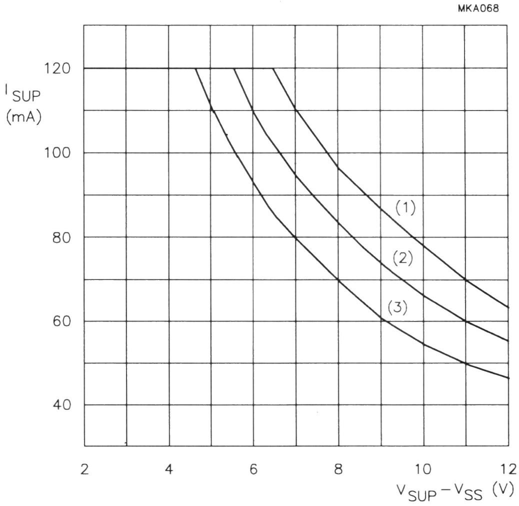


Fig.9 Safe operating area; see Table 4 (TEA1083AT).

Table 2

CURVE	T_{amb}	P_{tot}
1	55 °C	700 mW
2	65 °C	600 mW
3	75 °C	500 mW

Table 3

CURVE	T_{amb}	P_{tot}
1	55 °C	1077 mW
2	65 °C	923 mW
3	75 °C	769 mW

Table 4

CURVE	T_{amb}	P_{tot}
1	55 °C	777 mW
2	65 °C	666 mW
3	75 °C	555 mW

CHARACTERISTICS

V_{SUP} = 3.6 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; LSE = HIGH; loudspeaker amplifier load = 50 Ω; all measurements taken in test circuit Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SUP}	Minimum DC input voltage		–	V_{BB}+0.6	–	V
$V_{SUP-SREF}$	Internal reference voltage		400	500	600	mV
V_{BB}	Stabilized supply voltage	I_{SUP} = 15 mA	2.75	2.95	3.15	V
ΔV_{BB}	Variation of supply voltage	from I_{SUP} = 15 to 120 mA	–	15	–	mV
$\Delta V_{BB}/\Delta T$	Variation of supply voltage with temperature, referred to 25 °C	T_{amb} = −25 to +75 °C; I_{sup} = 15 mA	–	±0.2	–	mV/K
I_{SUP}	Minimum operating current		–	2.5	4.0	mA
THD	Distortion of AC signal between SUP and V_{EE}	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	Noise between SUP and V_{EE} (RMS value)	psophometrically weighted (P53 curve)	–	−71	–	dBmp
	Current consumption in power-down condition	PD = HIGH				
I_{SUP}	V_{SUP} = 3.6 V		–	50	75	µA
I_{BB}	V_{BB} = 2.95 V		–	400	550	µA
Loudspeaker amplifier inputs LSI1 and LSI2						
Z_i	input impedance (LSI1 and LSI2)	single ended	7.5	9.5	11.5	kΩ
		differential (LSI1 to LSI2)	15	19	23	kΩ
G_v	Voltage gain from LSI1/2 to QLS	I_{SUP} = 15 mA; V_i = 2 mV(RMS)	34	35	36	dB
ΔG_v	Total gain variation with input signal from 2 mV(RMS) to 10 mV(RMS)		–	0.2	–	dB
$\Delta G/\Delta T$	Total gain variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±0.4	–	dB
Output capabilities						
$V_{O(p-p)}$	Maximum output voltage (peak-to-peak value)	THD = 3 %; 50 Ω load	2.0	2.5	–	V
$V_{O(p-p)}$	Output voltage (peak-to-peak value)	V_i = 10 mV(RMS); I_{SUP} = 15 mA; $V_{SUP}-V_{EE}$ = 1 V(RMS)	–	1.6	–	V
$V_{no(RMS)}$	Noise output voltage (RMS value)	1 kΩ between inputs LSI1 and LSI2; psophometrically weighted (P53 curve)	–	250	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (PD) (TEA1083A only)						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_{PD}	Input current	PD = HIGH	–	2.3	2.8	μA
LSE input						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_I	Input current	LSE = HIGH	–	5	10	μA
ΔG	Reduction of gain from LSI1/LSI2 to QLS	LSE = LOW	60	80	–	dB

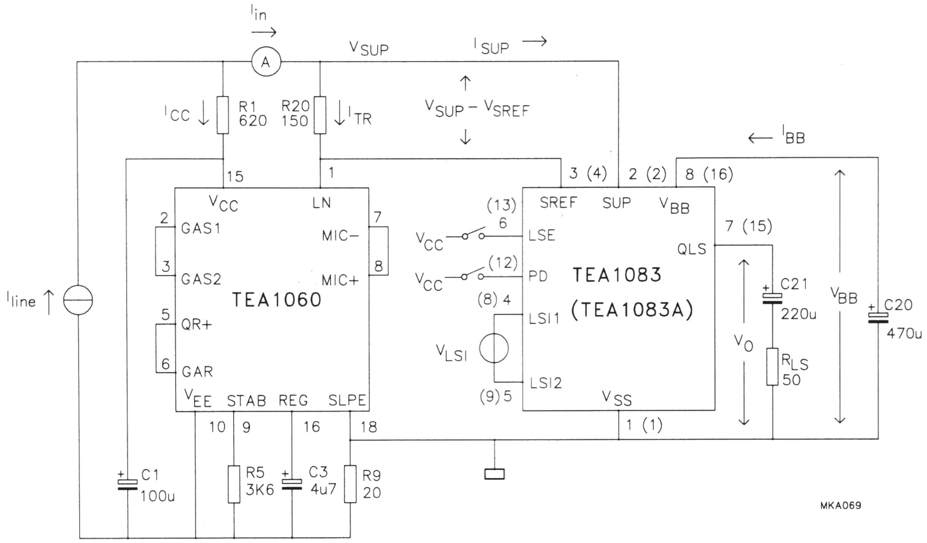

I_in
V_SUP
I_SUP
A
I_CC
R1 620
R20 150
I_TR
V_SUP – V_SREF
I_BB
15
1
3 (4)
2 (2)
8 (16)
V_CC
LN
GAS1
GAS2
MIC–
MIC+
TEA1060
QR+
GAR
V_EE
STAB
REG
SLPE
2
3
5
6
7
8
10
9
16
18
I_line
C1 100u
R5 3K6
C3 4u7
R9 20
SREF
SUP
V_BB
(13) 6
LSE
V_CC
(12)
PD
TEA1083
(TEA1083A)
(8) 4
LSI1
V_LSI
LSI2
(9) 5
V_SS
1 (1)
7 (15)
QLS
C21 220u
R_LS 50
V_O
V_BB
C20 470u
MKA069

Fig.10 Test circuit.

Notes to figure 10

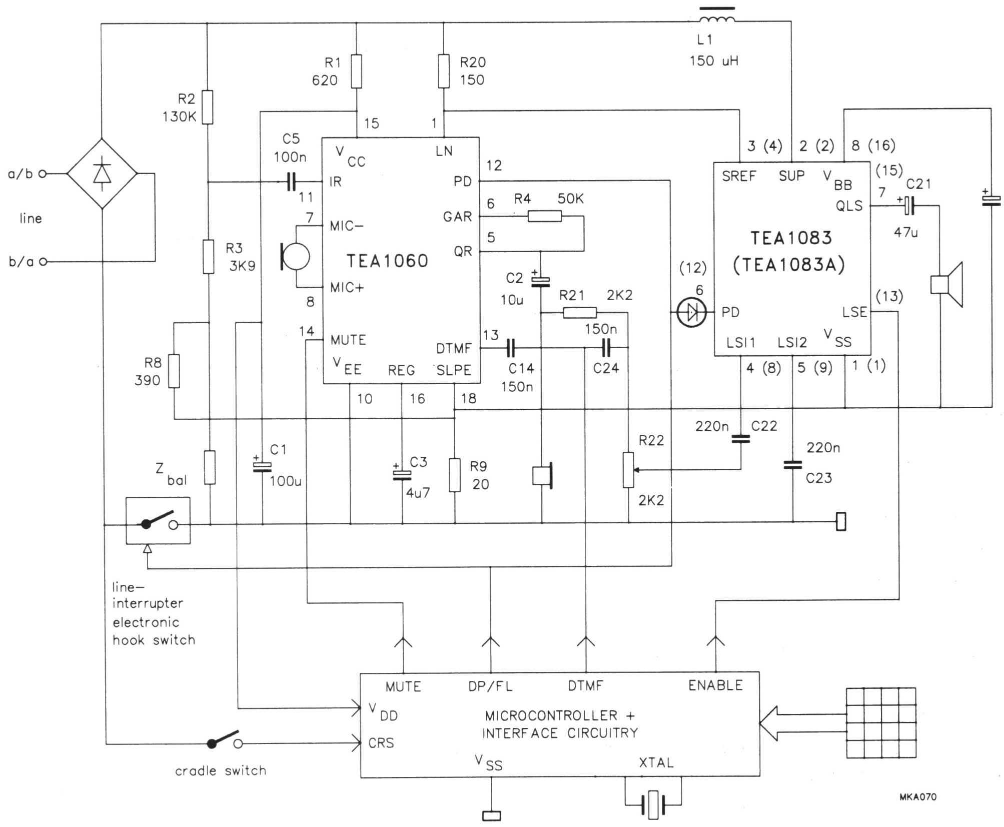
1. $I_{SUP} = I_{IN} - I_{TR}$
2. $G_v = 20\log\left|\frac{V_O}{V_{LSI}}\right|$
3. $I_{TR} = \frac{V_{SUP-SREF}}{R20}$
4. The pin numbers in parenthesis refer to the TEA1083
5. LSE has to be HIGH to measure the voltage gain
6. PD has to be HIGH to measure in PD conditions
7. The pins not shown in the TEA1060 are left open-circuit
8. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the values of I_{TR} and I_{SUP}.

APPLICATION INFORMATION

An application of the TEA1083/83A, in conjunction with a member of the TEA1060 family, is illustrated in figure 11. The TEA1083/83A is used for call progress monitoring during on-hook dialling. The dialling facilities are performed by a microcontroller (e.g. PCD3344, PCD3349).

Only the most important components have been shown. For detailed information refer to a data sheet of the TEA1060 family.

The electronic hook switch can be replaced by a mechanical system (hook switch) with a hold/release function which is intended for on-hook dialling.


L1
150 uH
R1
620
R20
150
R2
130K
15
1
C5
100n
V CC
LN
12
IR
PD
11
a/b
line
b/a
7
MIC−
6
R4
50K
GAR
5
R3
3K9
TEA1060
QR
C2
10u
MIC+
8
R21
2K2
14
MUTE
13
150n
DTMF
R8
390
V EE
REG
SLPE
C14
150n
C24
10
16
18
3 (4)
2 (2)
8 (16)
SREF
SUP
V BB
(15)
7
C21
QLS
47u
C20
220u
TEA1083
(TEA1083A)
(12)
6
PD
LSE
(13)
LSI1
LSI2
V SS
4 (8)
5 (9)
1 (1)
220n
C22
220n
C23
R22
2K2
C1
100u
C3
4u7
R9
20
Z bal
line−
interrupter
electronic
hook switch
MUTE
DP/FL
DTMF
ENABLE
V DD
MICROCONTROLLER +
INTERFACE CIRCUITRY
CRS
V SS
XTAL
cradle switch
MKA070

Pin numbers in parenthesis refer to the TEA1083.

Fig.11 Application example when the TEA1083/83A is used in conjunction with the TEA1060.

Listening-in circuit for line-powered telephone sets

TEA1085/TEA1085A

FEATURES

- Internal supply
  optimum current split-up
  - low constant current (adjustable) in transmission IC
  - nearly all line current available for listening-in
  adjustable supply voltage
- Loudspeaker amplifier
  dynamic limiter providing low distortion and the highest possible output power
  SE or BTL drive for loudspeaker
  volume control by potentiometer and/or logic inputs (e.g. microcontroller drive)
  fixed gain of 35 dB
- Larsen level limiter
  low sensitivity for own speech due to 3rd-order filter and attack delay
  adjustable voltage thresholds
- Power down input
- MUTE input
  TEA1085/TEA1085A
  - clickfree switching between listening-in mode and standby mode
  TEA1085
  - toggle function
  - start-up in standby condition
  TEA1085A
  - logic level input

GENERERAL DESCRIPTION

The TEA1085 and TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The circuits incorporate a supply circuit, loudspeaker amplifier dynamic limiter, MUTE circuit, power-down facility and logic inputs for gain setting. The devices also incorporate a Larsen Level Limiter to reduce howling effects.

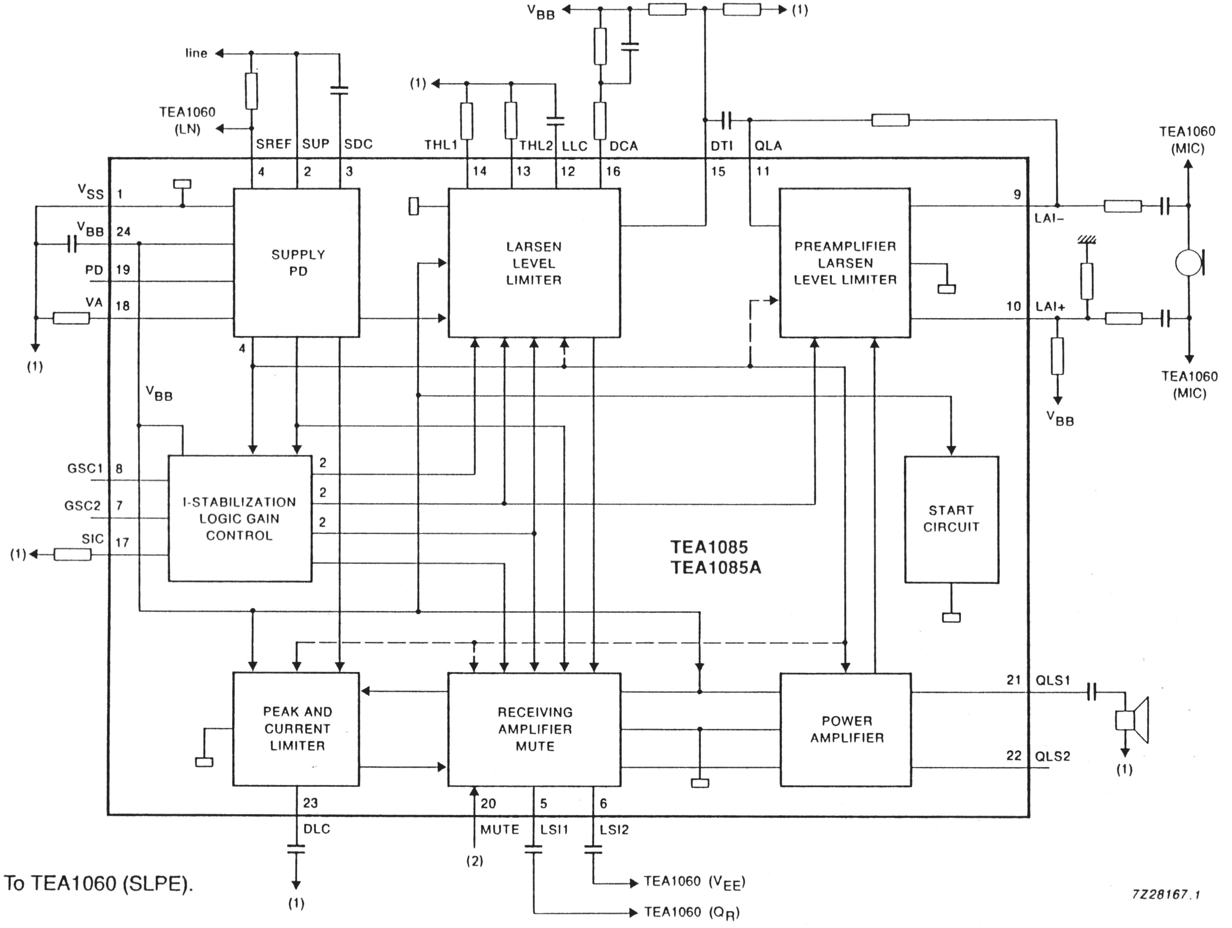
The ICs are intended for use in conjunction with a transmission circuit of the TEA1060 family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1085/TEA1085A	24	DIL	plastic	SOT101B
TEA1085T/TEA1085AT	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		4	–	120	mA
V_{BB}	stabilized supply voltage		–	3.6	–	V
I_{SUP}	current consumption	PD = HIGH	–	55	–	μA
G_v	voltage gain loudspeaker amplifier					
		SE	–	35	–	dB
		BTL	–	41	–	dB
ΔG_v	maximum gain reduction with logic inputs (3 steps)		–	18	–	dB
I_{SUP}	minimum input current					
		P_{OUT} = 20 mW typ. into 50 Ω SE	–	15	17	mA
		P_{OUT} = 40 mW typ. into 50 Ω BTL	–	–	32	mA
$t_{ad(RMS)}$	Larsen limiter attack delay time V_{DTI} jumps from 0 to ≥ 100 mV (RMS value)		100	–	200	ms
$V_{DTI(RMS)}$	Larsen limiter threshold level	Larsen mode	–	7	–	mV
G_v	Larsen limiter preamplifier gain setting range		30	–	52	dB
T_{amb}	operating ambient temperature range		–25	–	+75	°C


V_{BB}
(1)
line
TEA1060 (LN)
SREF
SUP
SDC
THL1
THL2
LLC
DCA
DTI
QLA
4
2
3
14
13
12
16
15
11
TEA1060 (MIC)
V_{SS} 1
V_{BB} 24
PD 19
VA 18
SUPPLY PD
LARSEN LEVEL LIMITER
PREAMPLIFIER LARSEN LEVEL LIMITER
9 LAI−
10 LAI+
V_{BB}
4
I-STABILIZATION LOGIC GAIN CONTROL
GSC1 8
GSC2 7
SIC 17
2
2
2
START CIRCUIT
TEA1085
TEA1085A
PEAK AND CURRENT LIMITER
RECEIVING AMPLIFIER MUTE
POWER AMPLIFIER
21 QLS1
22 QLS2
23 DLC
20 MUTE
5 LSI1
6 LSI2
(2)
TEA1060 (V_{EE})
TEA1060 (Q_R)
7Z28167.1

(1) To TEA1060 (SLPE).

(2) See Fig.16.

Fig.1 Block diagram.

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	negative supply
SUP	2	positive supply
SDC	3	supply amplifier decoupling
SREF	4	supply reference input
LSI1	5	loudspeaker amplifier input 1
LSI2	6	loudspeaker amplifier input 2
GSC2	7	logic input 2 for gain select
GSC1	8	logic input 1 for gain select
LAI–	9	Larsen limiter preamplifier inverting input
LAI+	10	Larsen limiter preamplifier non-inverting input
QLA	11	Larsen limiter preamplifier output
LLC	12	Larsen limiter capacitor
THL2	13	Larsen limiter residual threshold level
THL1	14	Larsen limiter attack delay threshold level
DTI	15	Larsen limiter detector input
DCA	16	Larsen limiter detector current adjustment
SIC	17	Larsen limiter current stabilizer
VA	18	V_{BB} voltage adjustment
PD	19	power-down input
MUTE	20	MUTE input
QLS1	21	loudspeaker amplifier output 1
QLS2	22	loudspeaker amplifier output 2
DLC	23	dynamic limiter capacitor
V_{BB}	24	stabilized supply decoupling

PIN CONFIGURATION

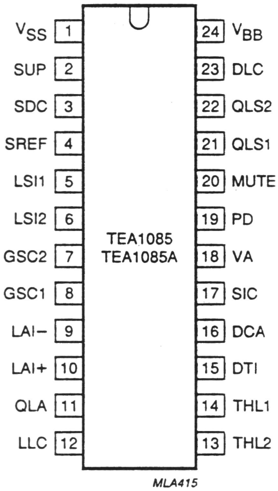

V_SS 1
SUP 2
SDC 3
SREF 4
LSI1 5
LSI2 6
GSC2 7
GSC1 8
LAI– 9
LAI+ 10
QLA 11
LLC 12
24 V_BB
23 DLC
22 QLS2
21 QLS1
20 MUTE
19 PD
18 VA
17 SIC
16 DCA
15 DTI
14 THL1
13 THL2
TEA1085
TEA1085A
MLA415

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 illustrates a block diagram of the TEA1085/TEA1085A with external components and connections to the transmission IC.

The TEA1085/TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The loudspeaker amplifier consists of a preamplifier, to amplify the earpiece signal from the transmission circuit and, a double push-pull output stage to drive the loudspeaker in the BTL (bridge tied load) or SE (single ended) configuration. The gain of the preamplifier is controlled by a dynamic limiter which prevents high distortion of the loudspeaker signal. This is achieved by preventing clipping of the loudspeaker signal, with respect to the supply voltage, and at too low supply current. Two logic inputs can be used to reduce the gain in 3 steps.

Because of acoustic feedback from the loudspeaker to the microphone, howling signals (Larsen effect) can occur on the telephone line and in the loudspeaker. When the Larsen signal exceeds a voltage and time duration threshold the Larsen level limiter (LLL) will reduce the Larsen signal to a low level within a short period of time by reducing the gain of the receiving preamplifier. This is achieved by using the microphone signal as an input signal which is processed in the LLL via a preamplifier and 3rd-order filter.

The MUTE input can be used to enable or disable the loudspeaker amplifier.

The MUTE function of the TEA1085 has a toggle input to permit the use of a simple push-button switch.

The MUTE function of the TEA1085A has a logic input to operate with a microcontroller.

By activating the power-down input the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC and start-up of the listening-in IC in the standby mode.

The TEA1085/TEA1085A are intended for use in conjunction with a member of the TEA1060 family and should be connected between LINE and SLPE of the transmission IC. The transmission characteristics (impedance, gain settings, for example) are not affected. The interconnection between the two ICs is illustrated in Fig.3.

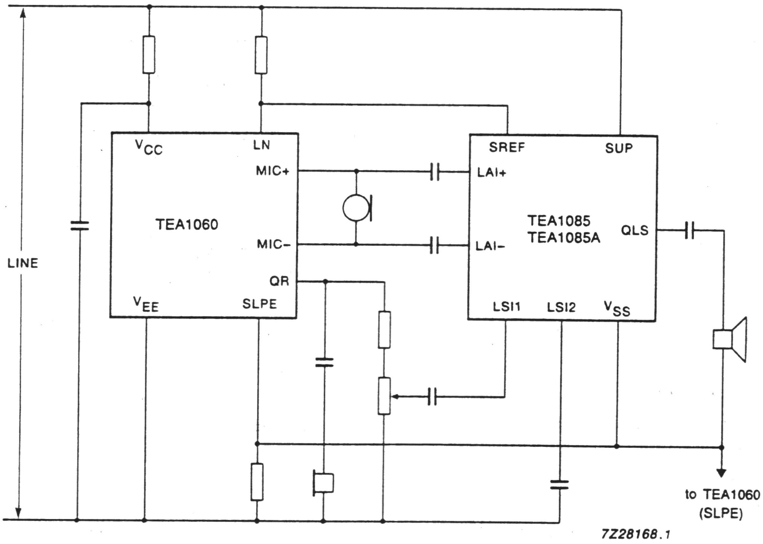
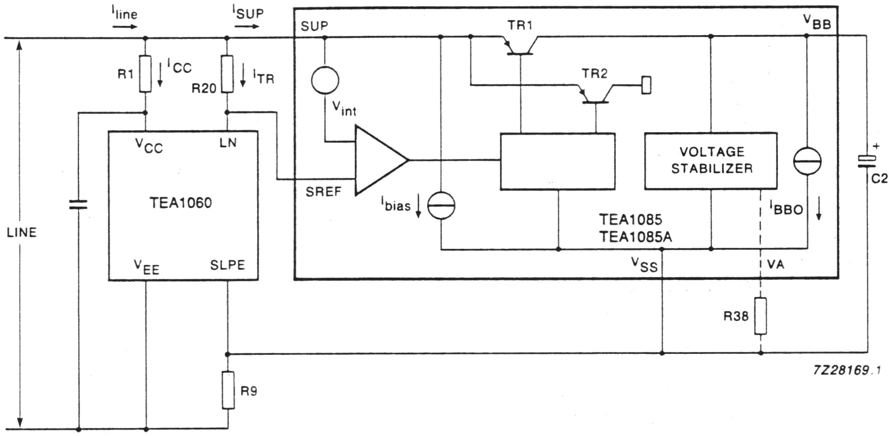


Fig.3 Interconnection of the TEA1085/TEA1085A with the TEA1060.

Supply; SUP, SREF, V_{BB}, V_{SS} and VA

The line current is divided into I_{TR} for the TEA1060 and I_{SUP} for the TEA1085/TEA1085A. The supply arrangement is illustrated in Fig.4.



I_{TR} is constant: $I_{TR} = V_{int}/R20$; $I_{SUP} = I_{line} - I_{CC} - I_{TR}$

Fig.4 Supply arrangement.

Where:

V_{int}	is an internal temperature compensated reference voltage with a typical value of 315 mV between SUP and SREF
R20	is a resistor between SUP and SREF
I_{CC}	is the internal current consumption of the TEA106X (≈ 1 mA)

A practical value for R20 is 150 Ω. This value of resistance produces a value for I_{TR} = 2 mA and $I_{SUP} = I_{line}$ −3 mA.

The TEA1085/TEA1085A stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. TR2 is used to minimize the signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 3.6 V but can be increased by means of an external resistor (R38) connected between VA and V_{SS} or decreased by connecting this resistor between VA and V_{BB}. The minimum level on V_{BB} is restricted to 3.0 V; the level of the V_{BB} limiter is also affected (see application report for further information). The supply at V_{BB} is decoupled by a 470 µF capacitor.

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC ($V_{LN-SLPE}$); thus $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$. The minimum DC voltage that can be applied to this input is $V_{BB(max)}$ + 0.4 V.

Where: $V_{BB(max)}$ is the worst case supply voltage (this depends on the setting of R38, which is connected between VA and V_{SS}).

The internal current consumption of the TEA1085/TEA1085A (I_{SUPo}) is typically 4.2 mA (where $V_{SUP} - V_{SS}$ = 4.5 V, MUTE off). Thus the current available for powering the loudspeaker is $I_{SUP} - I_{SUPo}$.
The current I_{SUPo} consists of a bias current of ≈ 0.4 mA for the circuitry connected to SUP and current I_{BBo} of ≈ 3.8 mA which is used for the circuitry connected to V_{BB} (see Fig.4).

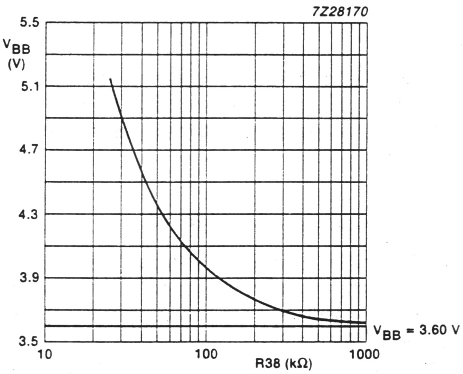


Fig.5 Stabilized supply voltage as a function of R38.

Supply amplifier stability (SDC) pin 3

To ensure stability of the TEA1085/TEA1085A, in combination with a transmission IC of the TEA1060 family, a 47 pF capacitor connected between SDC and SUP and a 150 µH coil connected between SUP and the positive line terminal (Fig.16) is required.

Loudspeaker amplifier (LSI1/LSI2 and QLS1/QLS2) pins 5/6, 21/22

The TEA1085/TEA1085A have symetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit via a resistive attenuator (see Fig.3). The amount of attenuation must be chosen in accordance with the receive gain of the transmission IC (which depends on the sensitivity of the earpiece transducer). The maximum input signal level is 450 mV(RMS) at T_{amb} = +25 °C.
The outputs QLS1 and QLS2 can be used for single ended drive (SE) or bridge tied load drive (BTL). The output stages have been optimized for use with a 50 Ω loudspeaker (eg Philips type AD2071).
The gain of the amplifier is fixed to ≈ 35 dB for the SE drive and ≈ 41 dB for the BTL drive (when the inputs for logic control are left open-circuit or are connected to V_{SS}).
The volume control can be obtained by using a potentiometer at the input and/or by the logic control function.

Logic gain control (GSC1 and GSC2) pins 7 and 8

The logic inputs GSC1 and GSC2 can be used to reduce the gain of the loudspeaker amplifier by means of the logic gain control function in 3 steps of 6 dB.

Table 1 Data for microcontroller drive of logic inputs

GSC2	GSC1	gain (dB)	gain reduction (dB)
0	0	35	0
0	1	28.7	6.3
1	0	22.2	12.2
1	1	17	18

Where:

0 = connection to V_{SS} or left open-circuit
1 = applying a voltage ≥ V_{SS} + 1.5 V

Dynamic limiter (DLC) pin 23

To prevent distortion of the signal at the loudspeaker outputs the gain of the amplifier is reduced rapidly when:

- the peaks of the signal at the loudspeaker outputs exceed an internaly determined threshold (voltage limiter)
- the DC current into SUP is insufficient (current limiter)
- the voltage at V_{BB} decreases below an internally determined threshold, typically 2.9 V (V_{BB} limiter)

The time in which the gain reduction is effected is the 'attack time'; this is very short in the first and third instance and relatively long in the second instance. The circuit will remain in the gain-reduced condition until the peaks of the output signal remain below the threshold level. The gain will then return to a nominal level after a time determined by the capacitor connected to DLC (release time).

MUTE input (MUTE) pin 20; TEA1085A

This MUTE is provided with a logic input to operate with a microcontroller for instance.
The loudspeaker amplifier is disabled when the MUTE input is LOW (connected to V_{SS} or open input). A HIGH level at the MUTE input enables the amplifier in the listening-in mode.

MUTE input (MUTE) pin 20; TEA1085

The MUTE function is provided with a toggle input and is designed to switch between the standby condition and the listening-in condition on the rising edge of the input MUTE signal (see Fig.6).
In the basic application the MUTE input must be LOW (connected to V_{SS}). A simple push-button can be used to operate the MUTE toggle (see Fig.7). Debouncing can be realized by means of a small capacitor connected between MUTE and V_{SS}.
An internal start circuit ensures that the circuit always starts up in the standby condition.

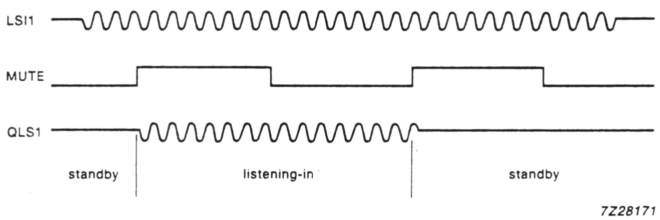
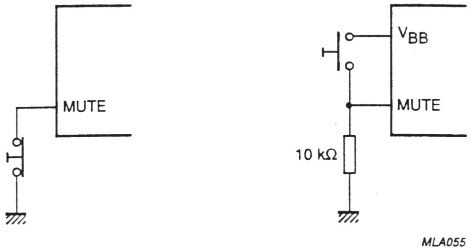


Fig.6 Mute toggle function of the TEA1085.



(a) Break contact.

(b) Make contact.

Fig.7 Mute switch alternatives with the TEA1085.

Power down input (PD) pin 19

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply to the transmission and listening-in circuits. The capacitor connected to V_{BB} provides the supply for the listening-in circuit during the supply breaks.
By making the PD input HIGH during the loop break the requirement on the capacitor is eased and, consequently, the internal (standby) current consumption I_{BBO} (Fig.4) at V_{BB} is reduced from 3.8 mA to 400 µA typical. So that the transmission circuit is not affected transistors TR1 and TR2 are inhibited and the bias current is reduced from ≈ 0.4 mA to ≈ 55 µA with V_{SUP} = 4.5 V in the following equation:

$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$

(where $4.2\ V < V_{SUP} < V_{BB} + 3\ V$)

$2V_d$ = the voltage drop across 2 internal diodes (≈ 1.3 V)
Ra = an internal resistor of typical 60 kΩ

Larsen limiter current stabilizer (SIC) pin 17

A current reference is set by resistor R36 between SIC and V_{SS}. The preferred value is 120 kΩ. The internal reference current is given by the following equation:

$I_{SIC} = 1.25/R36$; when R36 = 120 kΩ, I_{SIC} = 10.5 µA

Changing the value of R36 will affect the timing of the Larsen level limiter system.

Larsen limiter preamplifier (LAI1/LAI2 and QLA) pins 9/10 and 11

This circuit amplifies the microphone signal to a level suitable for the Larsen limiter detector. The gain is set by external components (see Fig.8).
Normally the gain is set to the same level as the microphone amplifier of the transmission circuit, this ensures that the output signal level at output QLA is equal to the line signal level.

The gain between QLA and the microphone input is given by the following equation (the high-pass filter is not taken into account):

$A_{pre} = V_{QLA}/V_M = R29/R26$; in the basic application R25 = R26 = 10 kΩ

The gain can be adjusted between 30 dB (R29 = 316 kΩ) and 52 dB (R29 = 4 MΩ). The impedance result of R28 and R27 in parallel must be equal to R29 (e.g. R27 = R28 = 2 x R29)

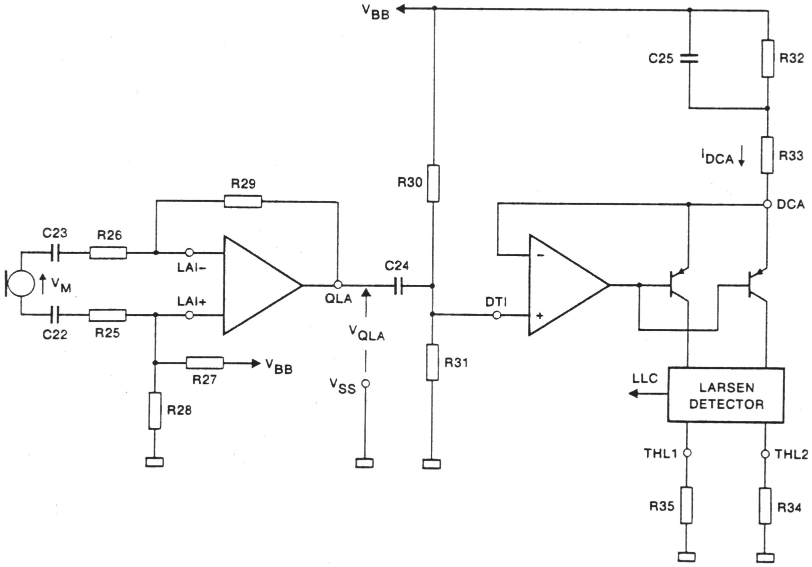


Fig.8 Larsen limiter preamplifier and voltage/current converter.

7Z28173

Larsen limiter detector (DTI and DCA) pins 15 and 16

The QLA output signal is AC coupled to the detector input DTI. DTI is biased by potential divider R30 and R31. The voltage applied to DTI of the Larsen level limiter is converted into a current for further processing in this circuit. Current adjustment is achieved using the network connected between DCA and V_{BB} (see Fig.8).

The equation for DC current is:

$$I_{DCA} = \frac{R30}{R30 + R31} \times V_{BB} \times \frac{1}{R32 + R33}$$

The equation for AC current is:

$$i_{DCA} = \frac{V_{DTI}}{R33} \text{ for } f > 1/2\pi R33C25$$

In the basic application:

R30 = 100 kΩ, R31 = 220 kΩ, R33 = 500 Ω, R32 = 100 kΩ and C25 = 330 nF

This results in I_{DCA} = 11 μA and the equation:

$$\frac{i_{DCA}}{V_{DTI}} + 2 \text{ (mA/V)}$$

High-pass filter

A third order high-pass filter is created between the microphone input voltage and the current flowing into DCA. The cut-off frequencies (see Fig.9) of the three sections are:

$$f1 = \frac{1}{2\pi R_{eq}C24} \text{ where } R_{eq} = \frac{R30 \times R31}{R30 + R31}$$

$$f2 = \frac{1}{2\pi R33C24} \qquad f3 = \frac{1}{2\pi R26C23} = 1/(2\pi R25C22)$$

Where: R25 = R26 and C22 = C23

The filter reduces the sensitivity of the system to own speech.
Normal speech is in the frequency range 300 Hz to 3400 Hz, however, the Larsen signal normally occurs at a frequency > 3 kHz.
With the component values as used in the basic application (see Fig.16); f1 = 500 Hz, f2 = 1 kHz and f3 = 3 kHz

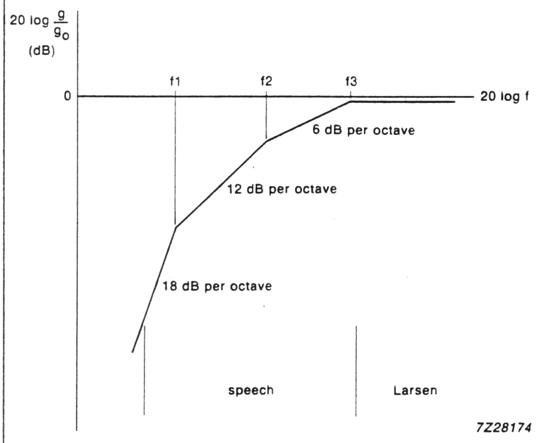


Fig.9 Third-order high-pass filter.

Where:

$$g = \frac{i_{DCA}}{V_m} \qquad g_O = \frac{A_{pre}}{R33}$$

Larsen limiter capacitor (LLC) pin 12

A 1 μF capacitor (C26) is connected externally between V_{SS} and LLC to determine the attack and release timing of the Larsen level limiter in the listen-in and Larsen mode. The timing is also dependent on the value of the resistor connected between SIC and V_{SS}.

Larsen level limiter threshold (THL1 and THL2) pins 13 and 14

When the signal at DTI exceeds the first threshold level the capacitor connected to LLC will start to discharge. The first threshold level is determined by the value of the resistor, R35, connected to THL1 and V_{SS}. The amount of discharge of C26 depends on how much the level of the signal at DTI exceeds the first threshold level (for normal speech the discharge is small).
The Larsen effect is generally defined as a signal level of ≥ 100 mV(RMS),on line, for a period of more than 100 ms. The Larsen signal must be reduced to a low level within 200 ms. For Larsen signal levels (f > f3 in Fig.9) of ≥ 100 mV(RMS) at DTI and, with the component values of Fig.16, the system will switch from the listen-in mode to the Larsen mode in a time period of 100 ms to 200 ms; consequently, the initial Larsen effect will last only for a short period of time.

This reaction time is the 'attack delay time' and ensures minimum sensitivity of the system for own speech.

The first threshold level at DTI is determined by the equation:

$$V_{DTI1} = \left(\frac{1.25}{R25} - \frac{I_{DCA}}{2}\right) \text{ x } 2 \text{ x } R33 \text{ (if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, I_{DCA} = 11 μA thus V_{DTI1} = 18.8 mV.

Listen-in mode

During normal speech the discharge of the capacitor connected to LLC is not sufficient to reach the threshold level whereby the system switches to the Larsen mode. This is because normal speech is not continuous, the discharge of C26 is slow (attack delay) and the charge is fast.
The slope of V_{LLC} during charge is given in the equation:

$$S_{1i} = \frac{\Delta V_{LLC}}{\Delta_\tau} = \frac{1.25}{C26 \times R36} \text{ (V/s)}$$

With C26 = 1 μF and R36 = 120 kΩ this results in S_{1i} = 10 V/s.

Discharge of the capacitor at LLC occurs when the signal at DTI exceeds V_{DTI1}, thus for a continuous signal at DTI the attack delay time t_{ad} (see Fig.10) is determined by the equation:

$$t_{ad} = \frac{C26 \times R36}{2 \times (3 \times k - 1)}$$

Where k = t1/T

The duty cycle is determined by the time in which the first threshold level (V_{DTI1}) is exceeded by the signal level at DTI (see Fig.11) thus for large signals; $k \leq 0.5$.
With the component values given in Fig.16; $k \geq 0.457$ for signals ≥ 100 mV(RMS).
Consequently 120 ms $\leq t_{ad} \leq$ 160 ms, for $V_{DTI} \geq$ 100 mV(RMS)

Larsen mode

After the 'attack delay time' the circuit switches from the listen-in mode to the Larsen mode. The gain of the loudspeaker amplifier is reduced quickly to a value (t_{LAa} = Larsen attack time see Fig.10) whereby the residual Larsen signal is determined by a second threshold level. This level can be set by resistor R34 connected between THL2 and V_{SS}. The second threshold level must always be selected at a lower level than the first threshold level thus R34 > R35.
The time taken to effect gain reduction is very short. In the Larsen mode the circuit acts as a dynamic limiter with peak detector and regulates the gain so that the signal level at DTI is determined by the second threshold level V_{DTI2}.
The second threshold level at DTI is determined by the equation:

$$V_{DTI2} = \left(\frac{1.25}{R34} - \frac{I_{DCA}}{2}\right) \text{ x } 2 \text{ x } R33 \text{ (if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, V_{DTI2} = 6.9 mV.

The charge current in the Larsen mode is reduced to half the charge current in the listen-in mode.

The slope of V_{LLC} during charge (see Fig.10) is given in the equation:

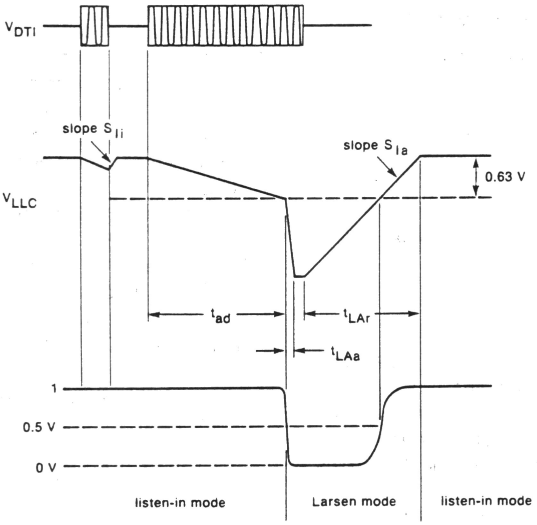
$$S_{la} = \frac{\Delta V_{LLC}}{\Delta_\tau} = \frac{1.25}{2 \times C26 \times R34} \text{ (V/s)}$$

Where: C26 = 1 μF and R36 = 100 kΩ, S_{la} = 5 V/s

When the Larsen effect stops (total open-loop gain < 1) the gain of the loudspeaker amplifier will return to its normal value in a time period known as the 'Larsen release time' (t_{LAr}). This time period is determined by capacitor C26 connected to LLC and resistor R36 connected to SIC.

Where: C26 = 1 μF and R36 = 120 kΩ, t_{LAr} = 250 ms

In practice the choice of the threshold levels (determined by R35 and R34) depends on the sensitivity of the microphone and loudspeaker, the send and receive gains, sidetone suppression and the acoustical properties which are determined by the cabinet of the telephone set.

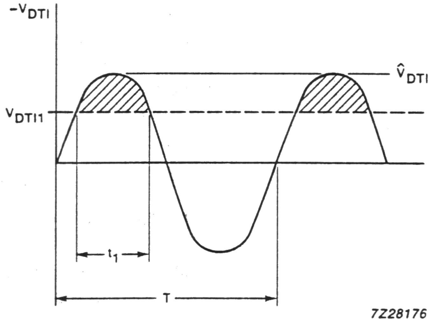

V_DTI
slope S_li
slope S_la
V_LLC
0.63 V
t_ad
t_LAr
t_LAa
1
0.5 V
0 V
listen-in mode
Larsen mode
listen-in mode
7Z28175

Where:

Change of receive gain = $\frac{G_v}{G_{vo}}$

Nominal receive gain = 20 log G_{vo} = 35 dB

Fig.10 Dynamic behaviour of Larsen limiter (in open-loop condition).


-V_DTI
V̂_DTI
V_DTI1
t_1
T
7Z28176

Where:

$$k = \frac{t_1}{T}$$

$$k = 0.5 - \frac{\arcsin\left(\frac{V_{DTI1}}{\hat{V}_{DTI}}\right)}{\pi}$$

Fig.11 Definition of duty cycle k.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

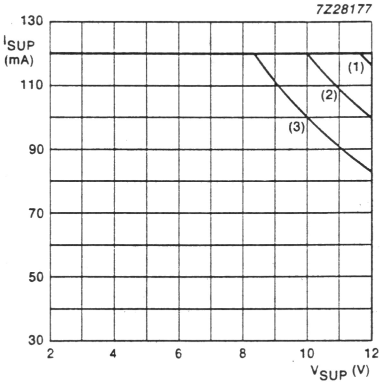
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	positive supply voltage				
	continous		–	12	V
	during switch-on or line interruption		–	13.2	V
	repetitive supply voltage from 1 ms to 5 s	with 12 Ω current limiting resistor in series with supply	–	28	V
V_{SREF}	supply reference voltage		V_{SS}–0.5	V_{SUP}+0.5	V
V_n	voltage on all other pins		V_{SS}–0.5	V_{BB}+0.5	V
I_{SUP}	supply current				
	TEA1085/TEA1085A	see Fig.12	–	120	mA
	TEA1085T/TEA1085AT	see Fig.13	–	120	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1085/TEA1085A		–	1	W
	TEA1085T/TEA1085AT		–	666	mW
T_{amb}	operating ambient temperature range		–25	+75	°C
T_{stg}	storage temperature range		–40	+125	°C
T_j	junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	TEA1085/TEA1085A		50 K/W
	TEA1085T/TEA1085AT	note 1	75 K/W

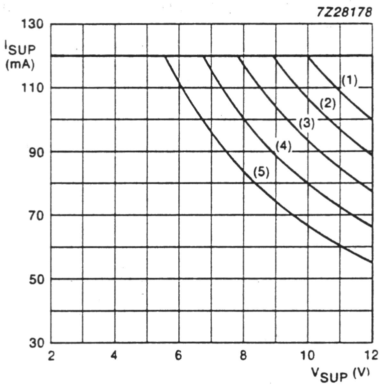
Note

1. Device mounted on a glass epoxy board 40.1 x 19.1 1.5 mm.



(1) T_{amb} = 55 °C; P_{tot} = 1.4 W.
(2) T_{amb} = 65 °C; P_{tot} = 1.2 W.
(3) T_{amb} = 75 °C; P_{tot} = 1.0 W.

Fig.12 TEA1085/TEA1085A safe operating area.



(1) T_{amb} = 35 °C; P_{tot} = 1.2 W.
(2) T_{amb} = 45 °C; P_{tot} = 1.07 W.
(3) T_{amb} = 55 °C; P_{tot} = 0.93 W.
(4) T_{amb} = 65 °C; P_{tot} = 0.8 W.
(5) T_{amb} = 75 °C; P_{tot} = 0.666 W.

Fig.13 TEA1085T/TEA1085AT safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V(RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; MUTE (TEA1085) = OFF (listening-in mode); MUTE (TEA1085A) = HIGH (listening-in mode); GSC1 = GSC2 = LOW; 50 Ω loudspeaker; no R38; test circuit Fig.14; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{SUP}	minimum DC input voltage		–	V_{BB}+0.7	–	V
$V_{SUP\text{-}SREF}$	internal reference voltage		275	315	355	mV
V_{BB}	stabilized supply voltage	no R38; I_{SUP} = 15 mA	3.4	3.6	3.8	V
ΔV_{BB}	variation from I_{SUP} = 15 to 120 mA		–	10	–	mV
		R38 = 39.2 kΩ between pins V_{SS} and VA; V_{SREF} = 5.2 V; I_{SUP} = 15 mA	4.2	4.45	4.7	V
$\Delta V_{BB}/\Delta T$	variation with temperature	no R38; I_{SUP} = 15 mA	tbf	−0.2	tbf	V
I_{SUP}	minimum operating current		–	4.2	5.5	mA
THD	distortion of AC signal on SUP	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	noise between SUP and V_{EE}		–	−72	–	dBmp
	current consumption in power-down condition	PD = HIGH				
I_{SUP}		V_{SUP} = 4.5 V	–	55	75	μA
I_{BB}		V_{BB} = 3.6 V	–	400	550	μA
Loudspeaker amplifier inputs LSI1 and LSI2						
$\lvert Z_i \rvert$	input impedance					
		single ended	7.5	9.5	11.5	kΩ
		differential	15	19	23	kΩ
G_v	voltage gain with 50 Ω load	I_{SUP} = 15 mA; V_i = 1.8 mV(RMS)				
		single ended	34	35	36	dB
		BTL output	39.9	40.9	41.9	dB
ΔG_v	variation with signal level	I_{SUP} = 50 mA; V_i = 1.8 mV(RMS) and 14 mV(RMS)				
		single ended	–	+0.1	0.4	dB
		BTL output	–	+0.2	0.6	dB
ΔG_v	variation with frequency referred to 1 kHz	f = 300 Hz and 3400 Hz; V_i = 1.8 mV(RMS)				
		single ended	–	± 0.1	–	dB
		BTL output	–	± 0.1	–	dB

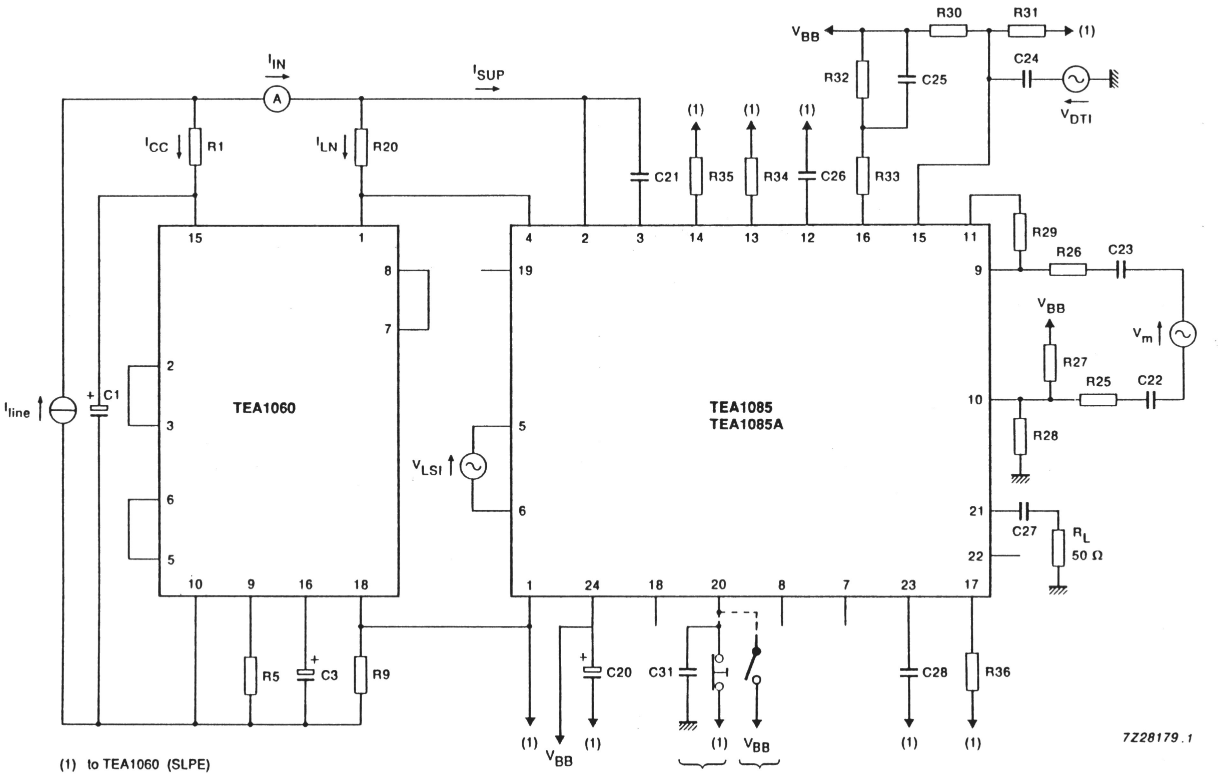
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_v	variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C				
		single ended	–	± 0.4	–	dB
		BTL output	–	± 0.5	–	dB
Loudspeaker outputs QLS1 and QLS2						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA; note 1	1.2	1.45	–	V
		I_{SUP} = 17 mA; note 2	2.5	2.9	–	V
	bridge-tied load	I_{SUP} = 23.5 mA; note 2	2.5	2.9	–	V
		I_{SUP} = 32 mA; note 3	3.5	4.0	–	V
THD	total harmonic distortion	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA	–	0.4	2	%
		I_{SUP} = 17 mA	–	0.7	2	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.4	2	%
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 17 mA; V_{SUP}-V_{EE} = 1 V(RMS)	1.75	2.15	–	V
Dynamic limiter						
THD	total harmonic distortion	V_i = 22 mV(RMS) +10 dB				
	single ended	I_{SUP} = 9 mA	–	0.5	10	%
		I_{SUP} = 17 mA	–	1.2	10	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.6	10	%
	dynamic behaviour of limiter	single ended load				
t_{att}	attack time; V_i jumps from 10 mV(RMS) to 65 mV(RMS)					
	voltage limiter	I_{SUP} = 17 mA	–	2	5	ms
	current limiter	I_{SUP} = 12 mA	–	500	tbf	ms
	V_{BB} limiter	I_{SUP} = 9 mA	–	10	–	ms
t_{rel}	release time; V_i jumps from 65 mV(RMS) to 10 mV(RMS)	I_{SUP} = 17 mA	tbf	75	tbf	ms
V_{BBO}	threshold V_{BB} limiter below which gain reduction starts	I_{SUP} = 9 mA	tbf	2.95	tbf	V
$V_{no(RMS)}$	noise output voltage	1 kΩ between inputs LSI1, LSI2; psophometrically weighted (P53 curve)				
	single ended		–	170	–	μV
	bridge tied load		–	350	–	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic gain control						
ΔG_v	reduction of voltage gain	V_i = 1.8 mV(RMS)				
	GSC2 = 0, GSC1 = 1		5.8	6.3	6.8	dB
	GSC2 = 1, GSC1 = 0		11.7	12.2	12.7	dB
	GSC2 = 1, GSC1 = 1		17	18	19	dB
Larsen limiter preamplifier						
	operational amplifier					
G_{v0}	open-loop gain		–	92	–	dB
f_{p1}	1st pole		–	120	–	Hz
f_{p2}	2nd pole		–	3.3	–	MHz
G_B	unity gain bandwidth		–	4	–	MHz
G_v	voltage gain	f = 3 kHz; R26 = 10 kΩ; R29 = 4 MΩ	51	52	53	dB
G_v	gain adjustment range		30	–	52	dB
Larsen limiter detector						
	voltage to current convertor					
V_{DCA}-V_{DTI}	DC offset voltage	V_{BB}-V_{DTI} = 1 V	–25	1	+25	mV
G_v	voltage gain from DTI to DCA	V_{DTI} = 100 mV(RMS); f = 3 kHz	tbf	–0.8	tbf	dB
V_{THL1}	DC voltage at THL1	R35 = 51 kΩ	1.8	1.25	1.33	V
V_{THL2}	DC voltage at THL2	R34 = 100 kΩ	1.8	1.25	1.33	V
	dynamic behaviour with a burst at DTI	f = 3 kHz; see Fig.15				
t_{LIr}	listen-in release time	see Fig.15(a)	tbf	40	tbf	ms
t_{ad}	attack delay time	see Fig.15(b)				
	V_{DTI} jumps from 0 to 100 mV (RMS value)		–	160	200	ms
	V_{DTI} jumps from 0 to 1 V (RMS value)		100	120	–	ms
t_{LAa}	Larsen attack time	see Fig.15(b); V_{DTI} = 100 mV(RMS)	–	20	tbf	ms
t_{LAr}	Larsen release time	see Fig.15(b)				
	V_{DTI} jumps from 100 mV to 0 mV (RMS value)		tbf	250	tbf	ms
V_{LLC}	DC voltage at LLC	V_{DTI} = 0 V	1.75	1.9	2.0	V
$-\Delta V_{LLC}$	reduction of V_{LLC} to attack Larsen mode		0.59	0.63	0.68	V
ΔG_v	gain reduction	V_{LLC} = 0.7 V	60	tbf	tbf	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE INPUT; TEA1085						
	(toggle function, positive edge triggered set-reset flip-flop)					
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{MUTE}	input current	MUTE = LOW	–	−22	−28	µA
t_W	minimum input pulse width		–	50	–	µs
P_R	minimum pulse repetition time		–	2	–	ms
$V_{BB(MUTE)}$	supply voltage below which MUTE toggle is reset		tbf	2	tbf	V
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = ON	60	100	–	dB
MUTE INPUT; TEA1085A						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{MUTE}	input current	MUTE = HIGH	–	10	20	µA
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = HIGH	60	100	–	dB
POWER DOWN INPUT						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{PD}	input current	PD = HIGH	–	2.3	2.8	µA
LOGIC INPUTS GSC1 and GSC2						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{GSC}	input current	GSC = HIGH	–	6	8	µA

Notes to the characteristics

1. Typical output power is 5 mW into 50 Ω
2. Typical output power is 20 mW into 50 Ω
3. Typical output power is 40 mW into 50 Ω


TEA1060
TEA1085
TEA1085A
R1
R20
R5
C3
R9
C1
I_line
I_IN
I_CC
I_LN
I_SUP
A
V_LSI
C21
R35
R34
C26
R33
R32
C25
R30
R31
C24
V_DTI
V_BB
R29
R26
C23
V_m
R27
R25
C22
R28
C27
R_L
50 Ω
C20
C31
C28
R36
(1)
for TEA1085
for TEA1085A
7Z28179.1

(1) to TEA1060 (SLPE)

The DC current is divided as follows:

$$I_{SUP} = I_{IN} - \frac{V_{SUP-SREF}}{R20}$$

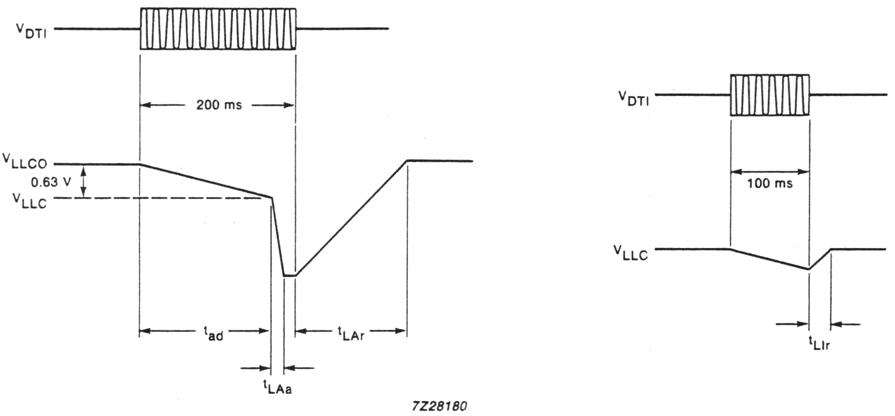
$$I_{LN} = \frac{V_{SUP-SREF}}{R20}$$

The pins not shown in the TEA1060 are left open. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the value of I_{LN}.

Fig.14 Test circuit.

Table 2 Component values in test circuit Fig.14

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R1		620	Ω
R5		3.6	kΩ
R9		20	Ω
R20		150	Ω
R25		10	kΩ
R26		10	kΩ
R27		8	MΩ
R28		8	MΩ
R29		4	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
Capacitor			
C1		100	μF
C3		4.7	μF
C20		470	μF
C21		68	pF
C22		2.2	μF
C23		2.2	μF
C24		100	nF
C25		330	nF
C26		1	μF
C27		220	μF
C28		330	nF
C31	TEA1085 only	10	nF


V_{DTI}
200 ms
V_{LLCO}
0.63 V
V_{LLC}
t_{ad}
t_{LAr}
t_{LAa}
7Z28180
V_{DTI}
100 ms
V_{LLC}
t_{LIr}

(a) Listen-in release time (t_{LIr}); V_{DTI} = 100 mV(RMS); f = 3 kHz.

(b) Attack delay (t_{ad}), Larsen attack time (t_{LAa}), Larsen release time (t_{LAr}); V_{DTI} = 100 mV(RMS) and 1 V(RMS); f = 3 kHz.

Fig.15 Test signals for Larsen level limiter.

APPLICATION INFORMATION

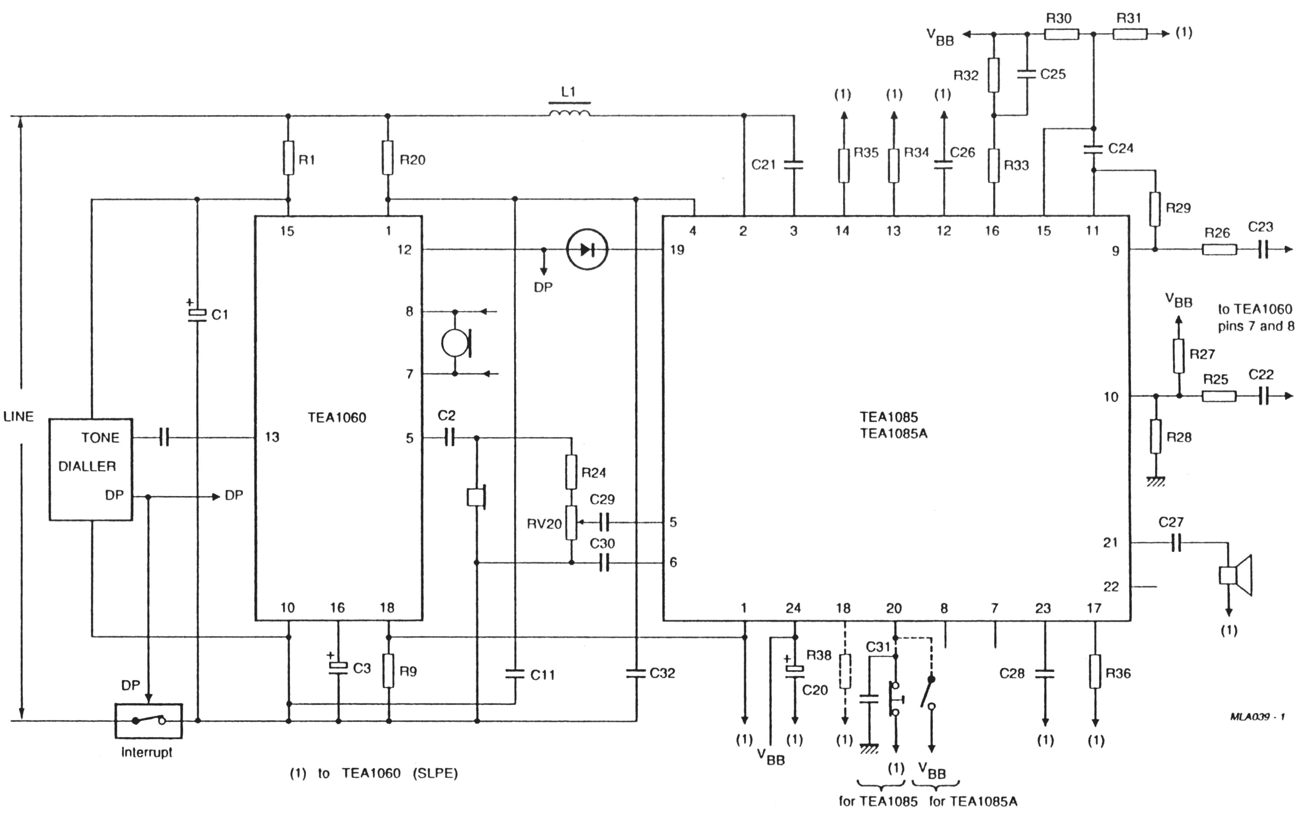

VBB
R30
R31
(1)
R32
C25
L1
(1)
(1)
(1)
R1
R20
C21
R35
R34
C26
R33
C24
R29
15
1
4
2
3
14
13
12
16
15
11
R26
C23
12
19
9
DP
C1
VBB
to TEA1060 pins 7 and 8
8
R27
7
R25
C22
10
LINE
TEA1060
C2
TEA1085
TEA1085A
TONE
DIALLER
13
5
R28
DP
DP
R24
C29
RV20
5
C27
C30
21
6
22
10
16
18
1
24
18
20
8
7
23
17
C3
R9
C11
C32
R38
C31
C28
R36
DP
C20
(1)
MLA039 - 1
Interrupt
(1)
(1)
(1)
(1)
(1)
VBB
(1)
VBB
(1) to TEA1060 (SLPE)
for TEA1085
for TEA1085A

Fig.16 Basic application of TEA1085/TEA1085A and TEA1060.

The basic application circuit of the TEA1085/TEA1085A is illustrated in Fig.16. Only the most important components of the TEA1060 part are shown, other components and their values are given in the TEA1060 Data sheet.
The supply pin (V_{BB}) of the TEA1085/TEA1085A can also be used to supply peripheral circuits (e.g. microcontrollers, diallers etc.). Further information will be published in the TEA1085 application report.

Table 3 Component values in application circuit Fig.16

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R20		150	Ω
R24	note 1	1	kΩ
R25		10	kΩ
R26		10	kΩ
R27	note 1	3.3	MΩ
R28	note 1	3.3	MΩ
R29	note 1	1.65	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
RV20	note 1	1	kΩ
Capacitor			
C11		4.7	nF
C20		470	μF
C21		47	pF
C22		4.7	nF
C23		4.7	nF
C24		4.7	nF
C25		330	nF
C26		1	μF
C27		47	μF
C28		330	nF
C29		220	nF
C30		220	nF
C31	TEA1085 only	10	nF
Coil			
L1		150	μH

Note to Table 3

1. Value depends on the gain setting of the transmission circuit.

Hands-free IC

TEA1093

FEATURES

- Line powered supply with:
  - adjustable stabilized supply voltage
  - power down function
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stages for single-ended or bridge-tied load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:

    externally adjustable sensitivity

    externally adjustable signal envelope time constant

    externally adjustable noise envelope time constant
  - decision logic with:

    externally adjustable switch-over timing

    externally adjustable idle mode timing

    externally adjustable dial tone detector in receive channel
  - voice switch control with:

    adjustable switching range

    constant sum of gain during switching

    constant sum of gain at different volume settings.

APPLICATIONS

- Line-powered telephone sets with hands-free/listening-in functions.

GENERAL DESCRIPTION

The TEA1093 is a bipolar circuit intended for use in line-powered telephone sets. In conjunction with a member of the TEA1060 family or PCA1070 transmission circuits, the device offers a hands-free function for line powered telephone sets. It incorporates a supply, a microphone channel, a loudspeaker channel and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1093	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1093T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

V_{SREF} = 4.2 V; V_{GND} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 1 kHz; T_{amb} = 25 °C; PD = LOW; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.15; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	operating supply current (pin SUP)		7	–	140	mA
V_{BB}	stabilized supply voltage		3.35	3.6	3.85	V
$I_{BB(pd)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA
$I_{SUP(pd)}$	current consumption from pin SUP in power-down condition	PD = HIGH; V_{sup} = 4.5 V	–	55	75	µA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	12.5	15	17.5	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		–10	–	+10	dB
G_{vrx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω				
	the difference between RIN1 and RIN2 to LSP1 or LSP2 single-ended load		15.5	18	20.5	dB
	the difference between RIN1 and RIN2 to the difference between LSP1 and LSP2 bridge-tied load		21.5	24	26.5	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		–15	–	+15	dB
$V_{O(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_L = 33 Ω; note 1	–	5.15	–	V
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		–40	–	+12	dB
T_{amb}	operating ambient temperature		–25	–	+75	°C

Note

1. Corresponds to 100 mW output power.

BLOCK DIAGRAM

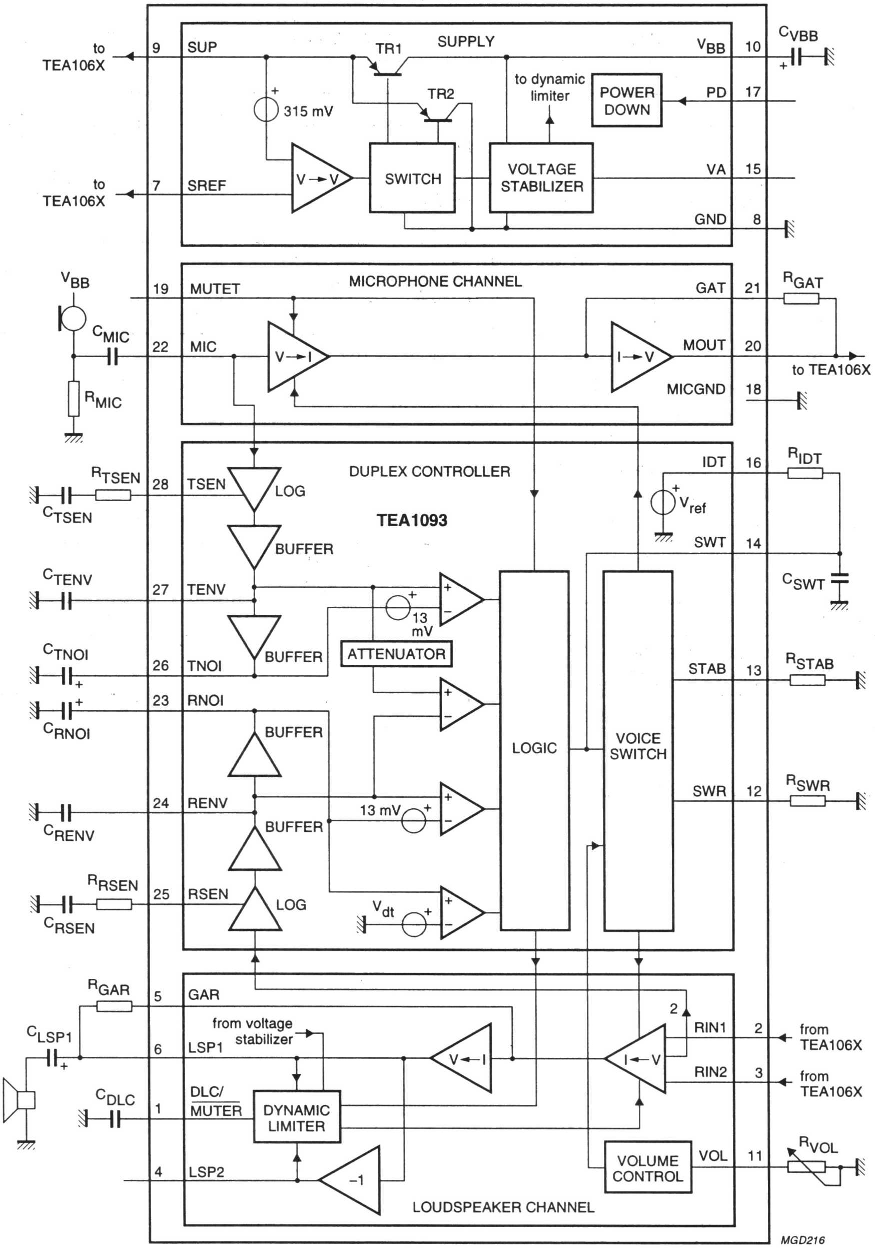

to TEA106X
9
SUP
TR1
SUPPLY
V_{BB}
10
C_{VBB}
TR2
315 mV
to dynamic limiter
POWER DOWN
PD
17
V→V
SWITCH
VOLTAGE STABILIZER
VA
15
to TEA106X
7
SREF
GND
8
V_{BB}
19
MUTET
MICROPHONE CHANNEL
GAT
21
R_{GAT}
C_{MIC}
22
MIC
V→I
I→V
MOUT
20
to TEA106X
R_{MIC}
MICGND
18
IDT
16
R_{IDT}
R_{TSEN}
28
TSEN
LOG
DUPLEX CONTROLLER
TEA1093
V_{ref}
C_{TSEN}
BUFFER
SWT
14
C_{SWT}
C_{TENV}
27
TENV
13 mV
C_{TNOI}
26
TNOI
BUFFER
ATTENUATOR
STAB
13
R_{STAB}
23
RNOI
C_{RNOI}
BUFFER
LOGIC
VOICE SWITCH
SWR
12
R_{SWR}
24
RENV
13 mV
C_{RENV}
BUFFER
R_{RSEN}
25
RSEN
LOG
V_{dt}
C_{RSEN}
R_{GAR}
5
GAR
2
RIN1
2
from TEA106X
C_{LSP1}
6
LSP1
from voltage stabilizer
V←I
I←V
RIN2
3
from TEA106X
C_{DLC}
1
DLC/MUTER
DYNAMIC LIMITER
VOL
11
R_{VOL}
4
LSP2
−1
VOLUME CONTROL
LOUDSPEAKER CHANNEL
MGD216

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DLC/$\overline{\text{MUTER}}$	1	dynamic limiter timing adjustment, receiver channel mute input
RIN1	2	receiver amplifier input 1
RIN2	3	receiver amplifier input 2
LSP2	4	loudspeaker amplifier output 2
GAR	5	receiver gain adjustment
LSP1	6	loudspeaker amplifier output 1
SREF	7	supply reference input
GND	8	ground reference
SUP	9	supply input
V_{BB}	10	stabilized supply output
VOL	11	receiver volume adjustment
SWR	12	switching range adjustment
STAB	13	reference current adjustment
SWT	14	switch-over timing adjustment
VA	15	V_{BB} voltage adjustment
IDT	16	idle mode timing adjustment
PD	17	power-down input
MICGND	18	ground reference for the microphone amplifier
MUTET	19	transmit channel mute input
MOUT	20	microphone amplifier output
GAT	21	microphone gain adjustment
MIC	22	microphone input
RNOI	23	receive noise envelope timing adjustment
RENV	24	receive signal envelope timing adjustment
RSEN	25	receive signal envelope sensitivity adjustment
TNOI	26	transmit noise envelope timing adjustment
TENV	27	transmit signal envelope timing adjustment
TSEN	28	transmit signal envelope sensitivity adjustment

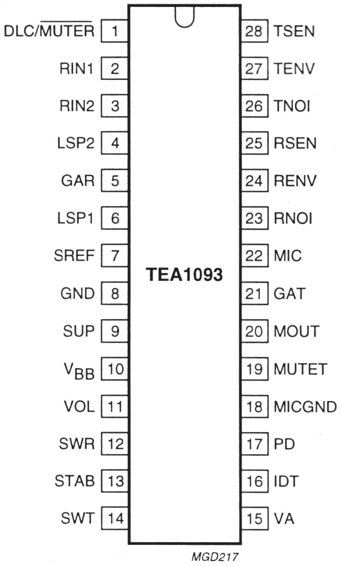

DLC/$\overline{\text{MUTER}}$
1
RIN1
2
RIN2
3
LSP2
4
GAR
5
LSP1
6
SREF
7
GND
8
SUP
9
V_{BB}
10
VOL
11
SWR
12
STAB
13
SWT
14
TEA1093
28
TSEN
27
TENV
26
TNOI
25
RSEN
24
RENV
23
RNOI
22
MIC
21
GAT
20
MOUT
19
MUTET
18
MICGND
17
PD
16
IDT
15
VA
MGD217

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in the functional description are typical values except when otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.3. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid. For more details on the TEA1060 family, please refer to *"Data Handbook IC03"*. The right side of Fig.3 shows a principle diagram of the TEA1093, a hands-free add-on circuit with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller.The duplex controller of the TEA1093 detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

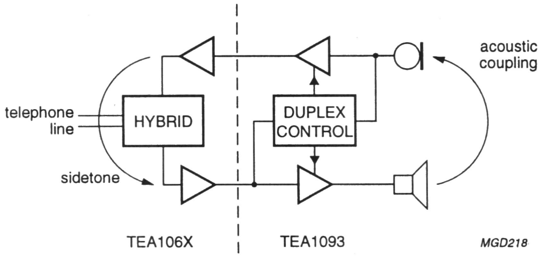


Fig.3 Hands-free telephone set principles.

Supply: pins SUP, SREF, V_{BB}, GND, VA and PD

As can be seen from Fig.4, the line current is divided between the speech-transmission circuit ($I_{TR} + I_{CC}$) and the TEA1093 circuit (I_{SUP}). It can be shown that:

$I_{SUP} = I_{line} - I_{TR} - I_{CC}$

Where:

$I_{TR} = V_{SUP} - V_{SREF}/R_{SREF}$

$V_{SUP} - V_{SREF} = 315$ mV

$R_{SREF} = 100\ \Omega$

$I_{CC} \approx 1$ mA

It follows that $I_{SUP} \approx I_{LINE} - 4$ mA.

The TEA1093 stabilizes its own supply voltage of 3.6 V at V_{BB}. The voltage on V_{BB} can be adjusted by means of an external resistor R_{VA}.

When R_{VA} is connected between pin V_A and GND, the voltage on V_{BB} is increased, when connected between pin V_A and V_{BB}, it is decreased. This is shown in Fig.5. Two capacitors of 4.7 nF (C_{SREF} and C_{STAB}) are required to ensure stability of the supply block. When V_{SUP} is greater than V_{BB} + 0.4 V, the current I_{SUP} is supplied to V_{BB} via TR1. When V_{SUP} is less, the current is shunted to GND via TR2, which prevents distortion on the line.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1093 is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from SUP is 55 μA and from V_{BB} 400 μA. Therefore a capacitor of 470 μF (C_{VBB}) is sufficient to power the TEA1093 during pulse dialling.

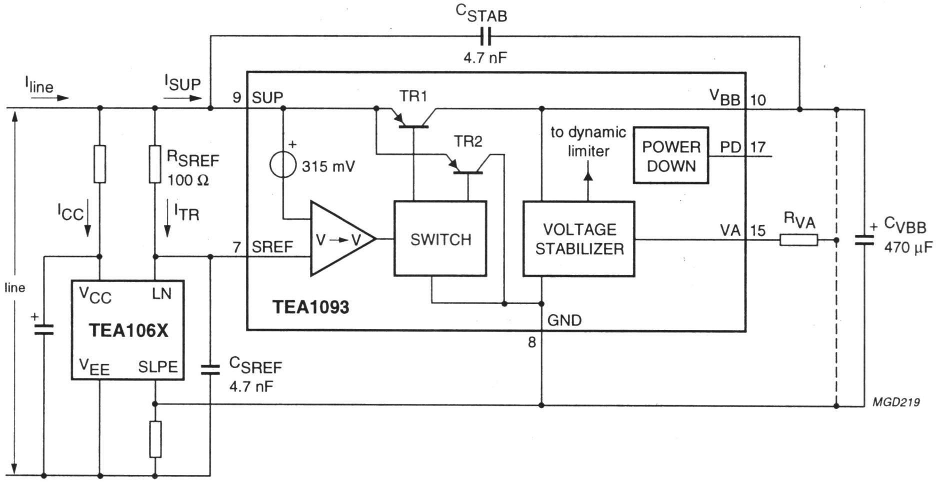

CSTAB
4.7 nF
Iline
ISUP
9 SUP
TR1
TR2
VBB 10
+
315 mV
to dynamic limiter
POWER DOWN
PD 17
RSREF 100 Ω
ICC
ITR
7 SREF
V→V
SWITCH
VOLTAGE STABILIZER
VA 15
RVA
+ CVBB 470 μF
line
VCC LN
TEA106X
VEE SLPE
TEA1093
GND
8
CSREF 4.7 nF
MGD219

Fig.4 Supply arrangement.

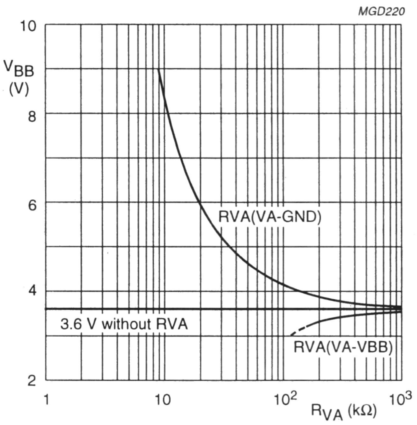


Fig.5 V_{BB} as a function of R_{VA}.

Microphone channel: pin MIC, GAT, MOUT, MICGND and MUTET

The TEA1093 has an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1093. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pin MIC to MOUT) can be adjusted from 5 dB up to 25 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15 dB typical with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first-order low-pass filter.

By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1093 is automatically forced into the receive mode.

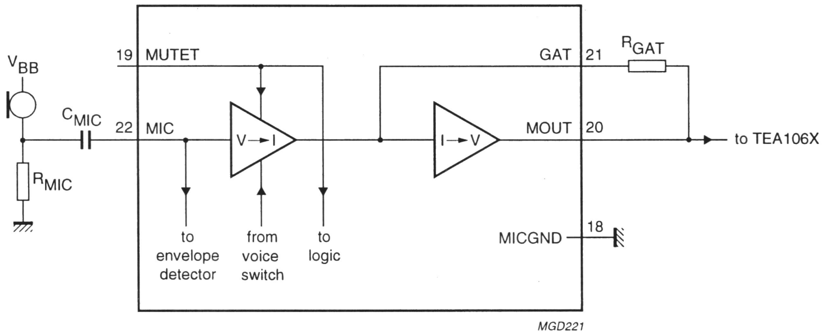


Fig.6 Microphone channel.

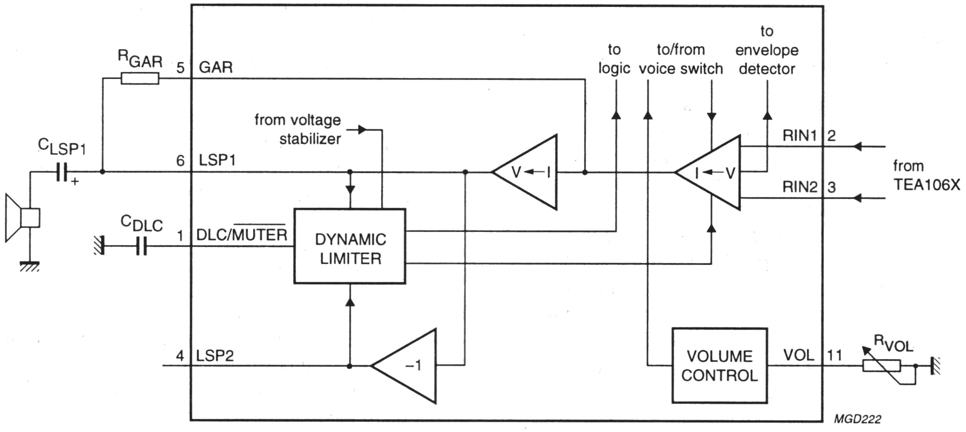


Fig.7 Loudspeaker channel.

Loudspeaker channel

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR, LSP1 AND LSP2

The TEA1093 has symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 × 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1093. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker which is connected as a single-ended load (between LSP1 and GND) or as a bridge-tied load (between LSP1 and LSP2).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 3 dB up to 39 dB to suit specific application requirements. The gain from RIN1 or RIN2 to LSP1 is proportional to the value of R_{GAR} and equals 18 dB with R_{GAR} = 66.5 kΩ. The second output LSP2 is in opposite phase with LSP1. Therefore, in the basic application, the gain between RIN1-RIN2 to LSP1-LSP2 equals 24 dB typical with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1093 prevents clipping of the loudspeaker output stages and protects the operation of the circuit when the supply condition falls below a certain level.

Hard clipping of the loudspeaker output stages is prevented by rapidly reducing the gain when the output stages start to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typical 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stages, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply conditions drop below the required level, the gain of the loudspeaker amplifier is reduced in order to prevent the TEA1093 from malfunctioning. Only the gain of the loudspeaker amplifier is affected since it is considered to be the major power consuming part of the TEA1093.

When the TEA1093 experiences a loss of current, the supply voltage V_{BB} decreases. In this event, the gain of the loudspeaker amplifiers is slowly reduced (approximately a few seconds). When the supply voltage continues to decrease and drops below an internal voltage threshold of 2.75 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When normal supply conditions are resumed, the gain of the loudspeaker amplifier is increased again. This system ensures that in the event of large continuous signals, all current is used to power the loudspeaker while the voltage on pin V_{BB} remains at its nominal value.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1093 is automatically forced into the transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.8.

For the transmit channel, the input signal at MIC is 40 dB, amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.16, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

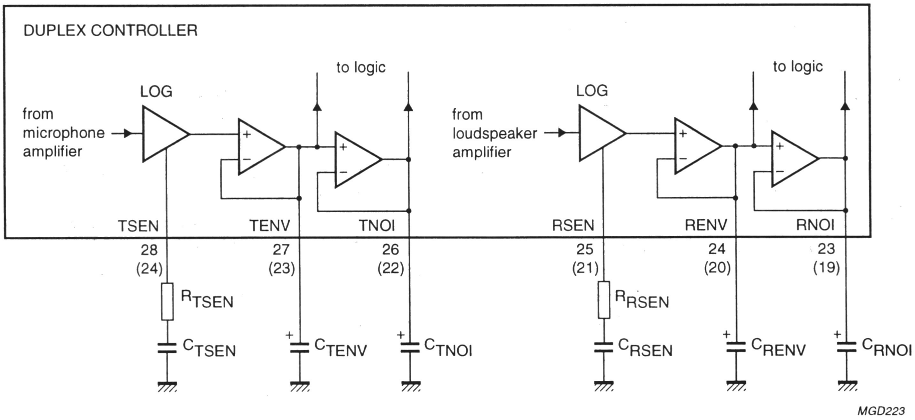


Fig.8 Signal and noise envelope detectors.

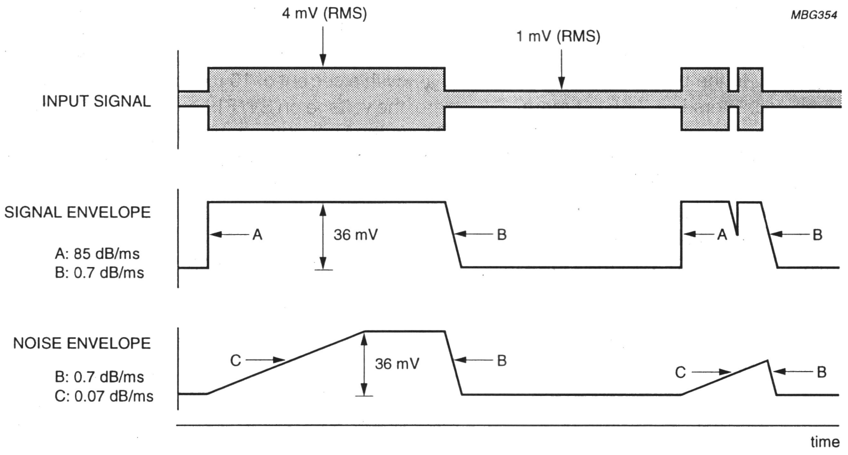
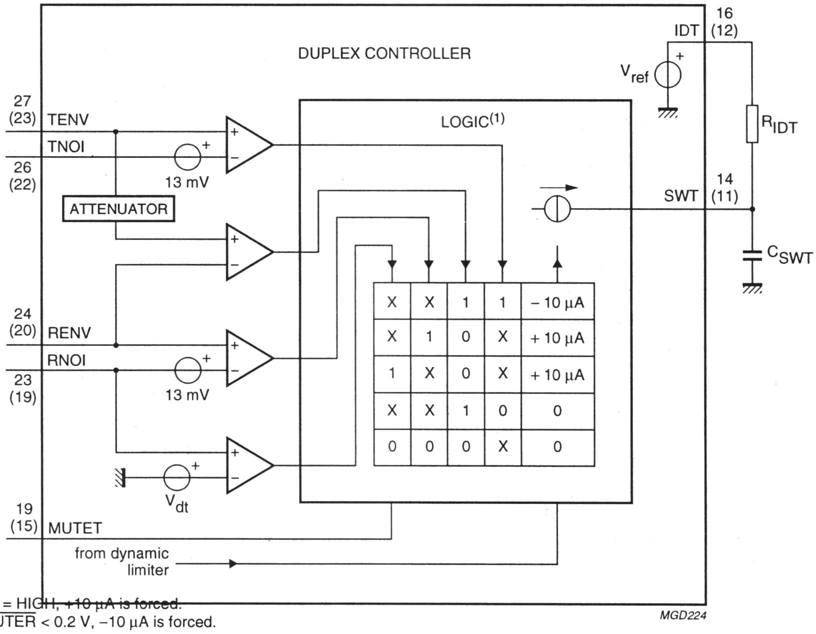

MBG354
4 mV (RMS)
1 mV (RMS)
INPUT SIGNAL
SIGNAL ENVELOPE
A: 85 dB/ms
B: 0.7 dB/ms
A
36 mV
B
A
B
NOISE ENVELOPE
B: 0.7 dB/ms
C: 0.07 dB/ms
C
36 mV
B
C
B
time

Fig.9 Signal and noise envelope waveforms.


DUPLEX CONTROLLER
LOGIC(1)
16
IDT
(12)
Vref
RIDT
14
SWT
(11)
CSWT
27
(23)
TENV
TNOI
26
(22)
13 mV
ATTENUATOR
24
(20)
RENV
RNOI
23
(19)
13 mV
Vdt
19
(15)
MUTET
from dynamic limiter
MGD224

X	X	1	1	− 10 μA
X	1	0	X	+ 10 μA
1	X	0	X	+ 10 μA
X	X	1	0	0
0	0	0	X	0

(1) When MUTET = HIGH, +10 μA is forced.
When DLC/$\overline{\text{MUTER}}$ < 0.2 V, −10 μA is forced.

Fig.10 Decision logic.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.16, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.9.

DECISION LOGIC: PINS IDT AND SWT

The TEA1093 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference V_{ENV}–V_{NOI} = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1093 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.10, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 μA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1093 and can vary between −400 mV and +400 mV.

Table 1 Modes of TEA1093

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>+180	receive mode

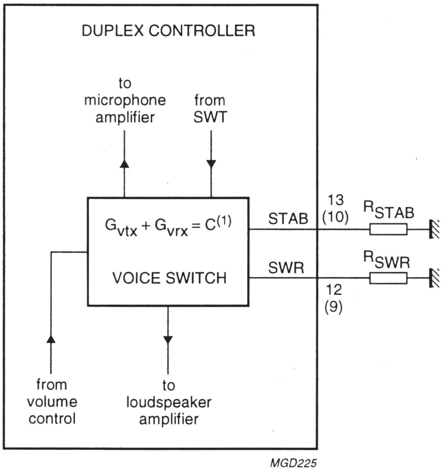
The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.16, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch over, from receive mode or transmit mode to idle mode, is equal to 4 × R_{IDT} × C_{SWT} and is approximately 2 seconds (idle mode time).

The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 μA thus resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor is discharged with 10 μA thus resulting in the transmit mode.

VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.11. With the voltage on SWT, the TEA1093 voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.


DUPLEX CONTROLLER
to microphone amplifier
from SWT
$G_{vtx} + G_{vrx} = C^{(1)}$
VOICE SWITCH
STAB
SWR
13 (10)
12 (9)
R_{STAB}
R_{SWR}
from volume control
to loudspeaker amplifier
MGD225

(1) c - constant.

Fig.11 Voice-switch.

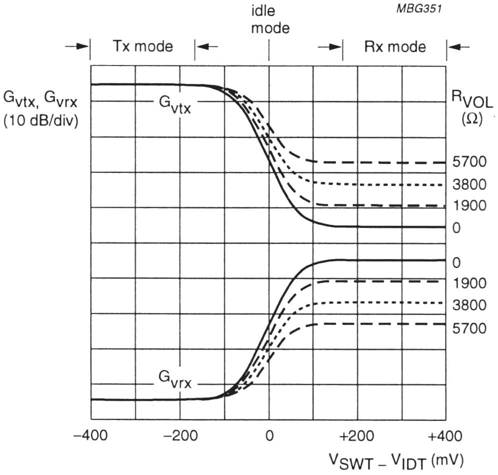


Fig.12 Switch-over behaviour.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway. The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.16, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.12.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.12). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

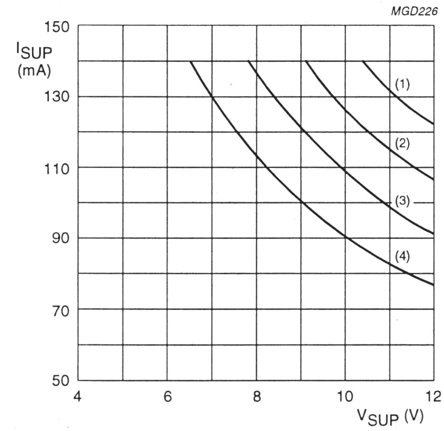
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins SUP, SREF, V_{BB}, RIN1 and RIN2		V_{GND} – 0.4 V	V_{BB} + 0.4 V	V
V_{RINmax}	maximum voltage on pin RIN1 or RIN2		V_{GND} – 1.2 V	V_{BB} + 0.4 V	V
V_{BBmax}	maximum voltage on pin V_{BB}		V_{GND} – 0.4 V	12.0	V
$V_{SREFmax}$	maximum voltage on pin SREF		V_{GND} – 0.4 V	V_{SUP} + 0.4 V	V
V_{SUPmax}	maximum voltage on pin SUP		V_{GND} – 0.4 V	12.0	V
I_{SUPmax}	maximum current on pin SUP	see also Figs 13 and 14	–	140	mA
P_{tot}	total power dissipation	see also Figs 13 and 14; T_{amb} = 75 °C			
	TEA1093		–	910	mW
	TEA1093T		–	670	mW
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

HANDLING

ESD in accordance with MIL STD883C; Method 3015 (HBM 1500 Ω, 100 pF); 3 pulses positive and 3 pulses negative on each pin referenced to ground. Class 2: 2000 to 3999 V.

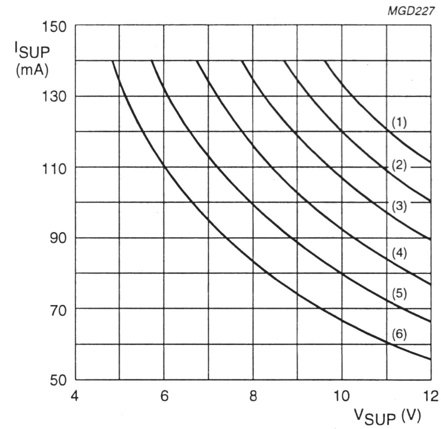
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1093	55	K/W
	TEA1093T	75	K/W



(1) T_{amb} = 45 °C; P_{tot} = 1.45 W.
(2) T_{amb} = 55 °C; P_{tot} = 1.27 W.
(3) T_{amb} = 65 °C; P_{tot} = 1.09 W.
(4) T_{amb} = 75 °C; P_{tot} = 0.91 W.

Fig.13 TEA1093 safe operating area.



(1) T_{amb} = 25 °C; P_{tot} = 1.33 W.
(2) T_{amb} = 35 °C; P_{tot} = 1.20 W.
(3) T_{amb} = 45 °C; P_{tot} = 1.07 W.
(4) T_{amb} = 55 °C; P_{tot} = 0.93 W.
(5) T_{amb} = 65 °C; P_{tot} = 0.80 W.
(6) T_{amb} = 75 °C; P_{tot} = 0.67 W.

Fig.14 TEA1093T safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{GND} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 1 kHz; T_{amb} = 25 °C; PD = LOW; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.15; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (VA, SREF, SUP, V_{BB}, GND and PD)						
V_{BB}	stabilized supply voltage		3.35	3.6	3.85	V
$\Delta V_{BB(ISUP)}$	V_{BB} variation with I_{SUP}	I_{SUP} = 15 to 140 mA	–	20	–	mV
$\Delta V_{BB(T)}$	V_{BB} variation with temperature referenced to 25 °C	T_{amb} = –25 to + 75 °C	–	±20	–	mV
$\Delta V_{BB(RVA)}$	V_{BB} adjustment with R_{VA}	between VA and V_{BB}; R_{VA} = 180 kΩ	–	3.2	–	V
		between VA and GND; V_{SREF} = 4.9 V; R_{VA} = 56 kΩ	–	4.5	–	V
$I_{SUP(min)}$	minimum operating current		–	5.5	7.0	mA
$V_{SUP} - V_{BB}$	minimum DC voltage drop between pin SUP and V_{BB}		0.4	–	–	V
$V_{SUP} - V_{SREF}$	internal reference voltage		275	315	355	mV
THD	total harmonic distortion of AC signal on SUP	V_{SUP} = 1 V (RMS)	–	0.5	–	%
Power-Down input PD						
V_{IL}	LOW level input voltage		V_{GND} – 0.4 V	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4 V	V
I_{PD}	input current in power-down condition	PD = HIGH	–	2.5	5.0	µA
$I_{SUP(PD)}$	current consumption from pin SUP in power-down condition	PD = HIGH; V_{SUP} = 4.5 V	–	55	75	µA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pin MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	12.5	15	17.5	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−10	−	+10	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = −25 to +75 °C	−	±0.3	−	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	−	±0.3	−	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	−	−100	−	dBmp
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} − 0.4 V	−	0.3	V
V_{IH}	HIGH level input voltage		1.5	−	V_{BB} + 0.4 V	V
I_{MUTET}	input current	MUTET = HIGH	−	2.5	5	μA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	−	80	−	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP1, LSP2 and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\|Z_i\|$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS)				
	the difference between RIN1 and RIN2 to the difference between LSP1 and LSP2, bridge-tied load		21.5	24	26.5	dB
	the difference between RIN1 and RIN2 to LSP1 or LSP2, single-ended load		15.5	18	20.5	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−15	−	+15	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = -25 to +75 °C	−	±0.3	−	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	for 2% THD in input stage; R_{GAR} = 11.8 kΩ	–	390	–	mV
$V_{norx(rms)}$	noise output voltage at pin LSP1 or LSP2 (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	80	–	μV
CMRR	common mode rejection ratio		–	50	–	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
OUTPUT CAPABILITY						
$V_{OSE(p-p)}$	single-ended load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); I_{SUP} = 11 mA; note 1	1.2	1.45	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 16.5 mA; note 2	2.5	2.9	–	V
$V_{OBTL(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); I_{SUP} = 27 mA; note 2	2.5	2.9	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 35 mA; note 3	3.5	4.0	–	V
		V_{RIN} = 150 mV (RMS); I_{SUP} = 62 mA; R_L = 33 Ω; note 4	–	5.15	–	V
$\lvert I_{OM(max)} \rvert$	maximum output current at LSP1 or LSP2 (peak value)		150	300	–	mA
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.75	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		$V_{GND} - 0.4$ V	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	$V_{DLC} = 0.2$ V	–	80	–	μA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	$V_{DLC} < 0.2$ V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN and RENV)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		38	40	42	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN.		−2	0	+2	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	$I_{TSEN} = 0.8$ to 160 μA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	$I_{RSEN} = 0.8$ to 160 μA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	μA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	μA
ΔV_{ENV}	voltage difference between pin RENV and TENV	when 10 μA is sourced from both RSEN and TSEN; envelope detectors tracking; note 5	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pin TNOI or RNOI		0.75	1	1.25	μA
$I_{sink(NOI)}$	maximum current sunk by pin TNOI or RNOI		–	120	–	μA
ΔV_{NOI}	voltage difference between pin RNOI and TNOI	when 5 μA is sourced from both RSEN and TSEN; noise detectors tracking; note 5	–	±3	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pin RIN1 and RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pin RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 6	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pin TENV and TNOI to switch-over from transmit to idle mode	note 6	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	µA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	µA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	µA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to 365 kΩ		−40	–	12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 5 mW output power.
2. Corresponds to 20 mW output power.
3. Corresponds to 40 mW output power.
4. Corresponds to 100 mW output power.
5. Corresponds to ±1 dB tracking.
6. Corresponds to 4.3 dB noise/speech recognition level.

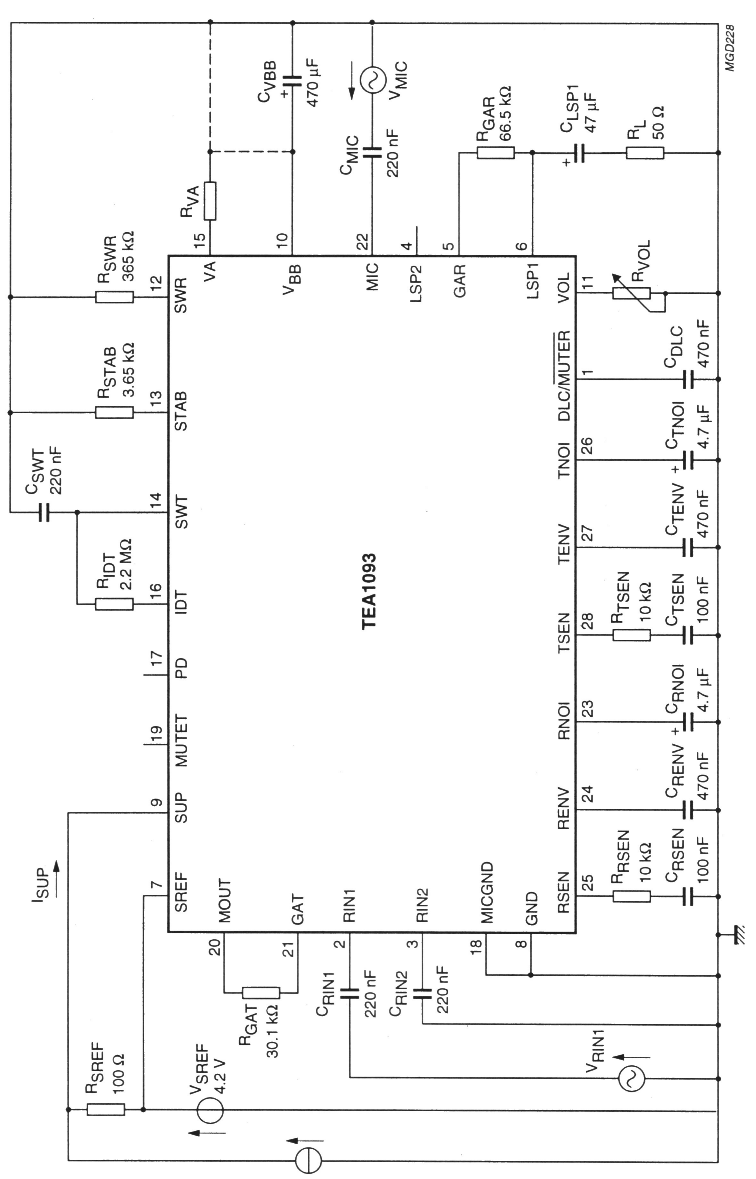

TEA1093
MGD228
RSWR 365 kΩ
RSTAB 3.65 kΩ
CSWT 220 nF
RIDT 2.2 MΩ
RVA
CVBB 470 µF
CMIC 220 nF
VMIC
RGAR 66.5 kΩ
CLSP1 47 µF
RL 50 Ω
RVOL
CDLC 470 nF
CTNOI 4.7 µF
CTENV 470 nF
RTSEN 10 kΩ
CTSEN 100 nF
CRNOI 4.7 µF
CRENV 470 nF
RRSEN 10 kΩ
CRSEN 100 nF
RGAT 30.1 kΩ
CRIN1 220 nF
CRIN2 220 nF
VRIN1
RSREF 100 Ω
VSREF 4.2 V
ISUP
12 SWR
13 STAB
14 SWT
16 IDT
17 PD
19 MUTET
9 SUP
7 SREF
15 VA
10 VBB
22 MIC
4 LSP2
5 GAR
6 LSP1
11 VOL
1 DLC/MUTER
26 TNOI
27 TENV
28 TSEN
23 RNOI
24 RENV
25 RSEN
20 MOUT
21 GAT
2 RIN1
3 RIN2
18 MICGND
8 GND

Fig.15 Test circuit.

APPLICATION INFORMATION

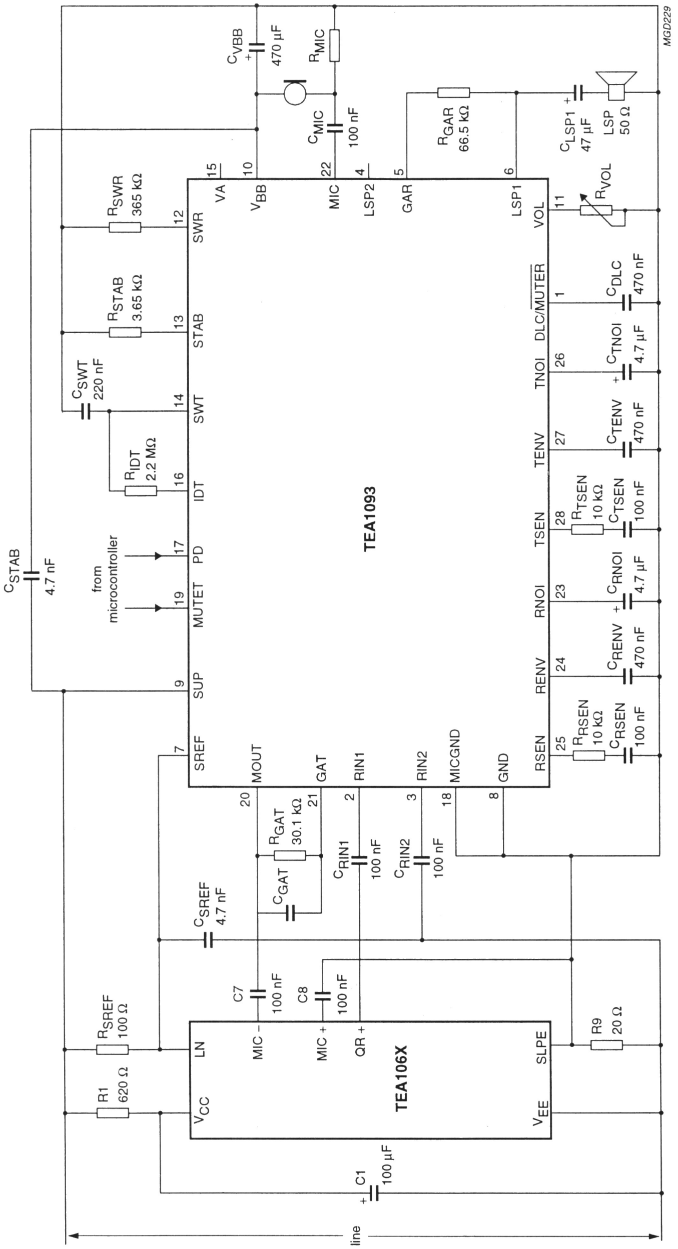

MGD229
TEA1093
TEA106X
C_{VBB} 470 μF
R_{MIC}
C_{MIC} 100 nF
R_{GAR} 66.5 kΩ
C_{LSP1} 47 μF
LSP 50 Ω
R_{VOL}
R_{SWR} 365 kΩ
R_{STAB} 3.65 kΩ
C_{SWT} 220 nF
R_{IDT} 2.2 MΩ
C_{STAB} 4.7 nF
from microcontroller
C_{DLC} 470 nF
C_{TNOI} 4.7 μF
C_{TENV} 470 nF
R_{TSEN} 10 kΩ
C_{TSEN} 100 nF
C_{RNOI} 4.7 μF
C_{RENV} 470 nF
R_{RSEN} 10 kΩ
C_{RSEN} 100 nF
R_{GAT} 30.1 kΩ
C_{GAT}
C_{RIN1} 100 nF
C_{RIN2} 100 nF
C_{SREF} 4.7 nF
C7 100 nF
C8 100 nF
R_{SREF} 100 Ω
R1 620 Ω
R9 20 Ω
C1 100 μF
line
15 VA
10 V_{BB}
22 MIC
4 LSP2
5 GAR
6 LSP1
11 VOL
1 DLC/$\overline{MUTER}$
26 TNOI
27 TENV
28 TSEN
23 RNOI
24 RENV
25 RSEN
12 SWR
13 STAB
14 SWT
16 IDT
17 PD
19 MUTET
9 SUP
7 SREF
20 MOUT
21 GAT
2 RIN1
3 RIN2
18 MICGND
8 GND
LN
V_{CC}
MIC −
MIC +
QR +
SLPE
V_{EE}

Fig.16 Basic application diagram.

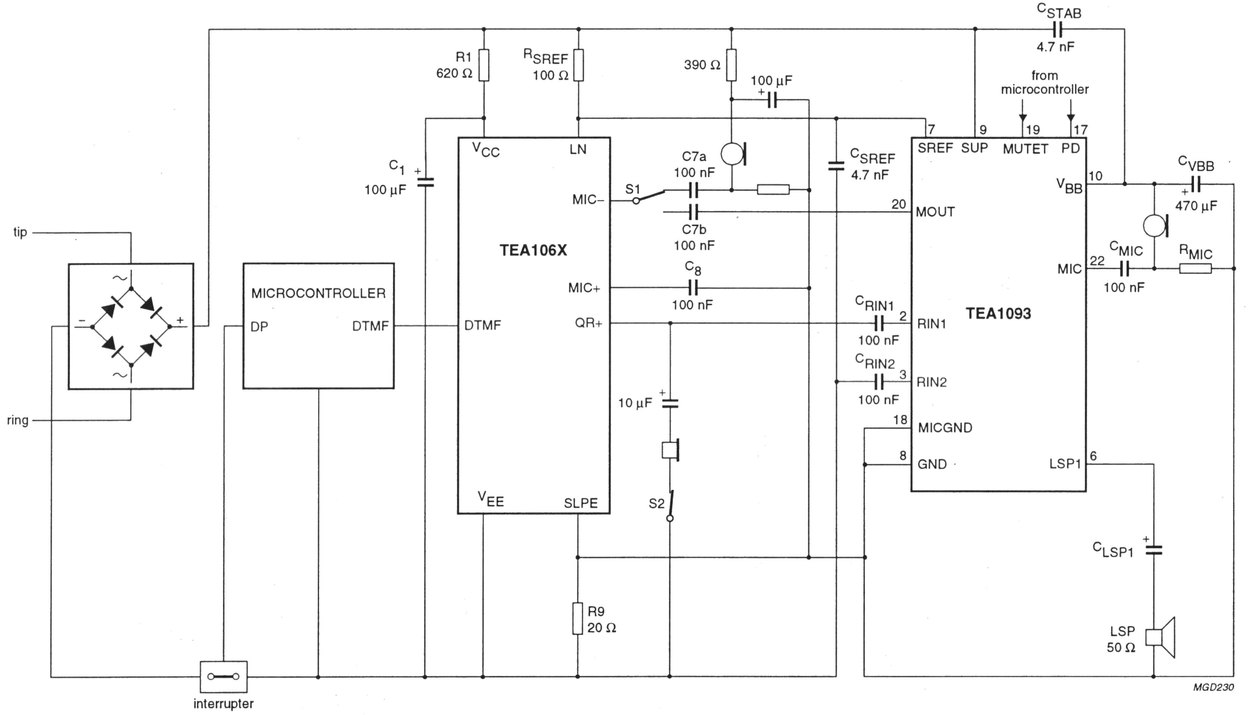

tip
ring
~
~
-
+
MICROCONTROLLER
DP
DTMF
interrupter
C1
+
100 µF
R1
620 Ω
RSREF
100 Ω
390 Ω
100 µF
+
VCC
LN
TEA106X
MIC−
MIC+
QR+
DTMF
VEE
SLPE
S1
C7a
100 nF
C7b
100 nF
C8
100 nF
10 µF
+
S2
R9
20 Ω
CSREF
4.7 nF
CSTAB
4.7 nF
from
microcontroller
7
9
19
17
SREF
SUP
MUTET
PD
TEA1093
VBB
10
20
MOUT
MIC
22
CRIN1
2
100 nF
RIN1
CRIN2
3
100 nF
RIN2
18
MICGND
8
GND
LSP1
6
CVBB
+
470 µF
CMIC
100 nF
RMIC
CLSP1
+
LSP
50 Ω
MGD230

Fig.17 Application proposal.

Hands free IC

TEA1094; TEA1094A

FEATURES

- Low power consumption
- Power-down function (TEA1094A only)
- Microphone channel with:
  - externally adjustable gain
  - microphone mute function.
- Loudspeaker channel with:
  - externally adjustable gain
  - dynamic limiter to prevent distortion
  - rail-to-rail output stage for single-ended load drive
  - logarithmic volume control via linear potentiometer
  - loudspeaker mute function.
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:

    externally adjustable sensitivity

    externally adjustable signal envelope time constant

    externally adjustable noise envelope time constant
  - decision logic with:

    externally adjustable switch-over timing

    externally adjustable idle mode timing

    externally adjustable dial tone detector in receive channel
  - voice switch control with:

    adjustable switching range

    constant sum of gain during switching

    constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets with hands-free/listening-in functions
- Cordless telephones
- Answering machines
- Fax machines.

GENERAL DESCRIPTION

The TEA1094; TEA1094A are bipolar circuits intended for use in mains, battery or line-powered telephone sets, cordless telephones, answering machines and Fax machines. In conjunction with a member of the TEA106X, TEA111X families of transmission circuits, the devices offer a hands-free function. They incorporate a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1094	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1094A	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1094T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TEA1094AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

QUICK REFERENCE DATA

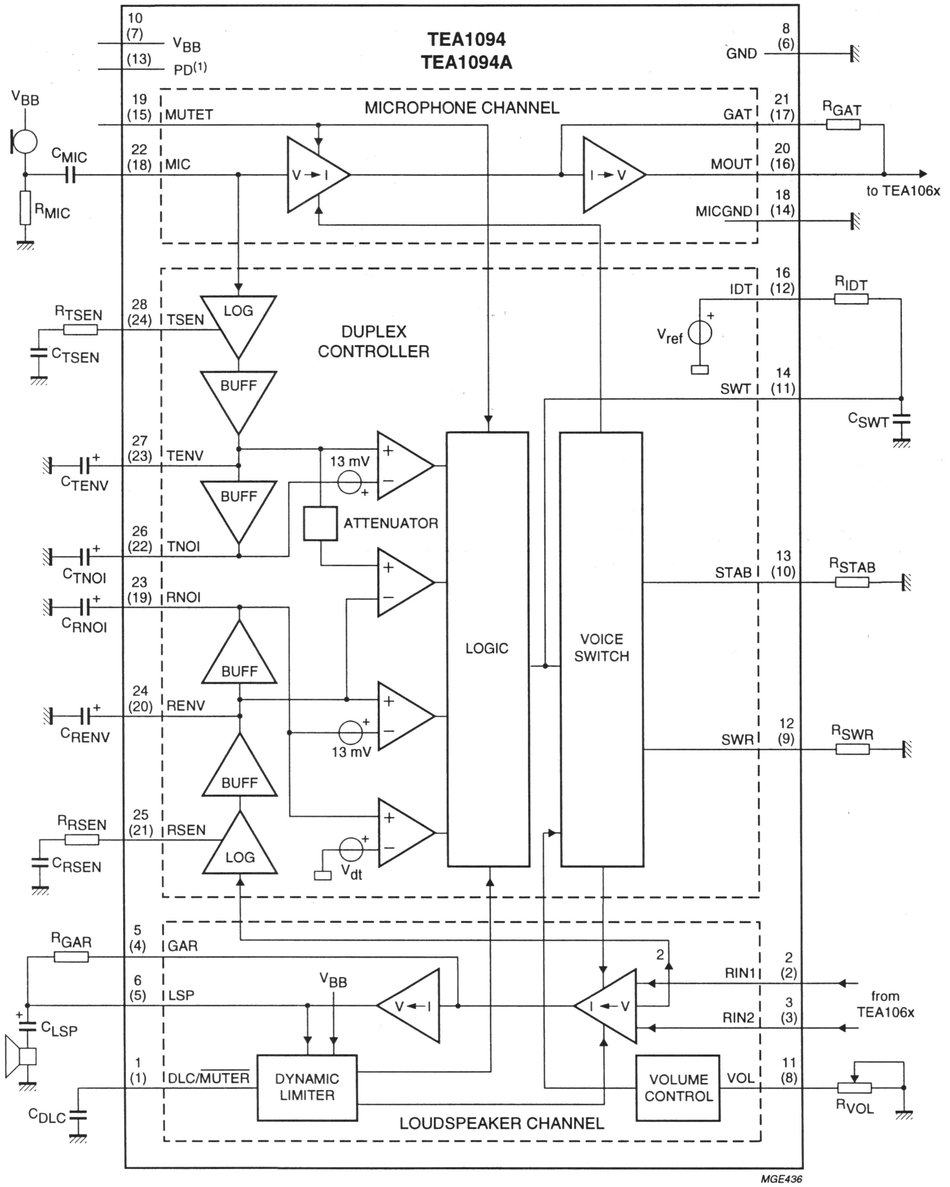
V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
G_{vtx}	voltage gain from pin MIC to pin MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		−15.5	–	+15.5	dB
G_{vrx}	voltage gain in receive mode; the difference between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
$V_{O(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 1	–	7.5	–	V
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment with R_{SWR} referenced to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note

1. Corresponds to 200 mW output power.

BLOCK DIAGRAM


TEA1094
TEA1094A
10
(7)
VBB
(13)
PD(1)
8
(6)
GND
VBB
19
(15)
MUTET
MICROPHONE CHANNEL
GAT
21
(17)
RGAT
CMIC
22
(18)
MIC
V → I
I → V
MOUT
20
(16)
to TEA106x
RMIC
18
(14)
MICGND
16
(12)
IDT
RIDT
RTSEN
28
(24)
TSEN
LOG
DUPLEX
CONTROLLER
Vref
CTSEN
BUFF
14
(11)
SWT
CSWT
27
(23)
TENV
13 mV
CTENV
BUFF
26
(22)
TNOI
ATTENUATOR
CTNOI
13
(10)
STAB
RSTAB
23
(19)
RNOI
CRNOI
BUFF
LOGIC
VOICE
SWITCH
24
(20)
RENV
CRENV
13 mV
12
(9)
SWR
RSWR
BUFF
RRSEN
25
(21)
RSEN
LOG
Vdt
CRSEN
RGAR
5
(4)
GAR
2
RIN1
2
(2)
6
(5)
LSP
VBB
V ← I
I ← V
from
TEA106x
CLSP
RIN2
3
(3)
1
(1)
DLC/MUTER
DYNAMIC
LIMITER
VOLUME
CONTROL
VOL
11
(8)
CDLC
RVOL
LOUDSPEAKER CHANNEL
MGE436

The pin numbers given in parenthesis are for the TEA1094A.

(1) TEA1094A only.

Fig.1 Block diagram.

PINNING

SYMBOL	PINS		DESCRIPTION
	TEA1094	TEA1094A	
DLC/$\overline{\text{MUTER}}$	1	1	dynamic limiter timing adjustment; receiver channel mute input
RIN1	2	2	receiver amplifier input 1
RIN2	3	3	receiver amplifier input 2
n.c.	4	–	not connected
GAR	5	4	receiver gain adjustment
LSP	6	5	loudspeaker amplifier output
n.c.	7	–	not connected
GND	8	6	ground reference
n.c.	9	–	not connected
V_{BB}	10	7	supply voltage
VOL	11	8	receiver volume adjustment
SWR	12	9	switching range adjustment
STAB	13	10	reference current adjustment
SWT	14	11	switch-over timing adjustment
n.c.	15	–	not connected
IDT	16	12	idle mode timing adjustment
PD	–	13	power-down input
n.c.	17	–	not connected
MICGND	18	14	ground reference for the microphone amplifier
MUTET	19	15	transmit channel mute input
MOUT	20	16	microphone amplifier output
GAT	21	17	microphone gain adjustment
MIC	22	18	microphone input
RNOI	23	19	receive noise envelope timing adjustment
RENV	24	20	receive signal envelope timing adjustment
RSEN	25	21	receive signal envelope sensitivity adjustment
TNOI	26	22	transmit noise envelope timing adjustment
TENV	27	23	transmit signal envelope timing adjustment
TSEN	28	24	transmit signal envelope sensitivity adjustment

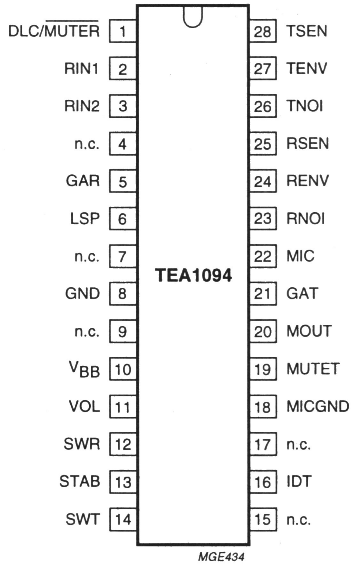

DLC/MUTER 1
RIN1 2
RIN2 3
n.c. 4
GAR 5
LSP 6
n.c. 7
GND 8
n.c. 9
VBB 10
VOL 11
SWR 12
STAB 13
SWT 14
28 TSEN
27 TENV
26 TNOI
25 RSEN
24 RENV
23 RNOI
22 MIC
21 GAT
20 MOUT
19 MUTET
18 MICGND
17 n.c.
16 IDT
15 n.c.
TEA1094
MGE434

Fig.2 Pin configuration (TEA1094).

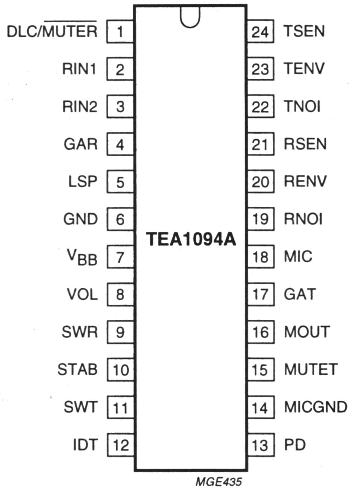

DLC/MUTER 1
RIN1 2
RIN2 3
GAR 4
LSP 5
GND 6
VBB 7
VOL 8
SWR 9
STAB 10
SWT 11
IDT 12
24 TSEN
23 TENV
22 TNOI
21 RSEN
20 RENV
19 RNOI
18 MIC
17 GAT
16 MOUT
15 MUTET
14 MICGND
13 PD
TEA1094A
MGE435

Fig.3 Pin configuration (TEA1094A).

FUNCTIONAL DESCRIPTION

General

The values given in the functional description are typical values unless otherwise specified.

A principle diagram of the TEA106X is shown on the left side of Fig.4. The TEA106X is a transmission circuit of the TEA1060 family intended for hand-set operation.
It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid.
For more details on the TEA1060 family, please refer to *"data Handbook IC03"*. The right side of Fig.4 shows a principle diagram of the TEA1094; TEA1094A, hands-free add-on circuits with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.4, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case.
The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1094; TEA1094A detects which channel has the 'largest' signal and then controls the gain of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant.
As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode).

   The gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.

2. Receive mode (Rx mode).

   The gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.

3. Idle mode.

   The gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

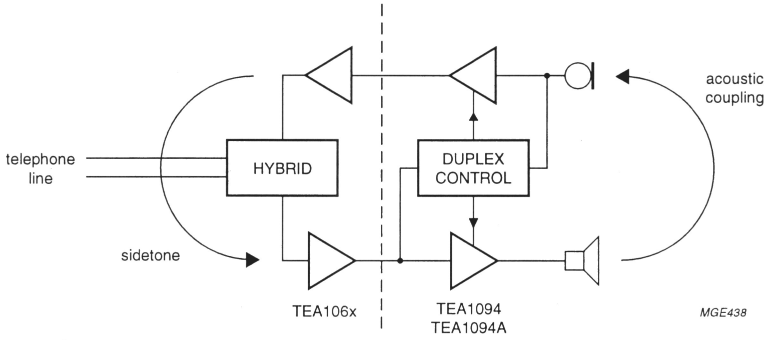


Fig.4 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1094; TEA1094A must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In the idle mode, without any signal, the internal supply current is 3.1 mA at V_{BB} = 5 V.

To reduce the current consumption during pulse dialling or register recall (flash), the TEA1094A is provided with a power-down (PD) input. When the voltage on PD is HIGH the current consumption from V_{BB} is 180 μA.

Microphone channel: pins MIC, GAT, MOUT, MICGND and MUTET (see Fig.5)

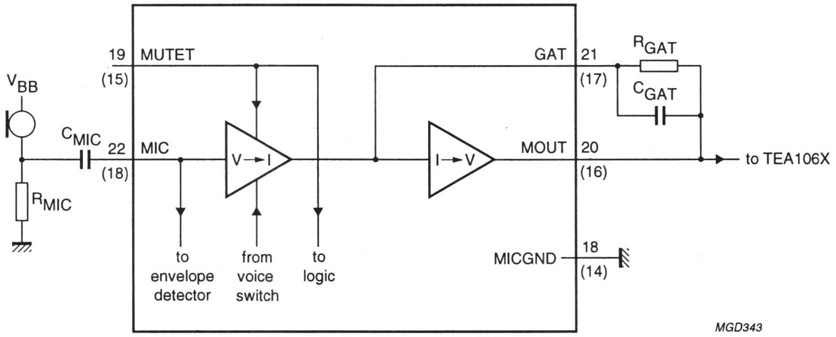
The TEA1094; TEA1094A have an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1094; TEA1094A. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum.

Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pins MIC to MOUT) can be adjusted from 0 dB up to 31 dB to suit specific application requirements. The gain is proportional to the value of R_{GAT} and equals 15.5 dB with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first-order low-pass filter.

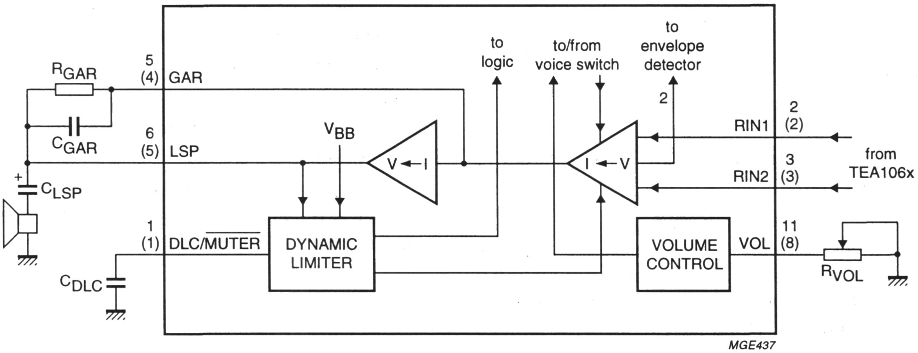
By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1094; TEA1094A are automatically forced into the receive mode.


19
(15)
MUTET
V_BB
C_MIC
22
(18)
MIC
R_MIC
V→I
to envelope detector
from voice switch
to logic
GAT
21
(17)
R_GAT
C_GAT
I→V
MOUT
20
(16)
to TEA106X
MICGND
18
(14)
MGD343

The pin numbers given in parenthesis refer to the TEA1094A.

Fig.5 Microphone channel.

Loudspeaker channel


R_GAR
5
(4)
GAR
C_GAR
6
(5)
LSP
+
C_LSP
1
(1)
DLC/MUTER
C_DLC
V_BB
DYNAMIC LIMITER
V←I
to logic
to/from voice switch
to envelope detector
2
I←V
VOLUME CONTROL
RIN1
2
(2)
RIN2
3
(3)
from TEA106x
VOL
11
(8)
R_VOL
MGE437

The pin numbers given in parenthesis refer to the TEA1094A.

Fig.6 Loudspeaker channel.

LOUDSPEAKER AMPLIFIER: PINS RIN1, RIN2, GAR AND LSP

The TEA1094; TEA1094A have symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (2 × 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1094; TEA1094A. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between LSP and GND).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 0 dB up to 33 dB to suit specific application requirements. The gain from RIN1 and RIN2 to LSP is proportional to the value of R_{GAR} and equals 18.5 dB with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first-order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain at the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1094; TEA1094A prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{BB} falls below 2.9 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{RIN} is below 390 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.9 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.9 V, the gain of the loudspeaker amplifier is increased again.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1094; TEA1094A is automatically forced into the transmit mode.

Duplex controller

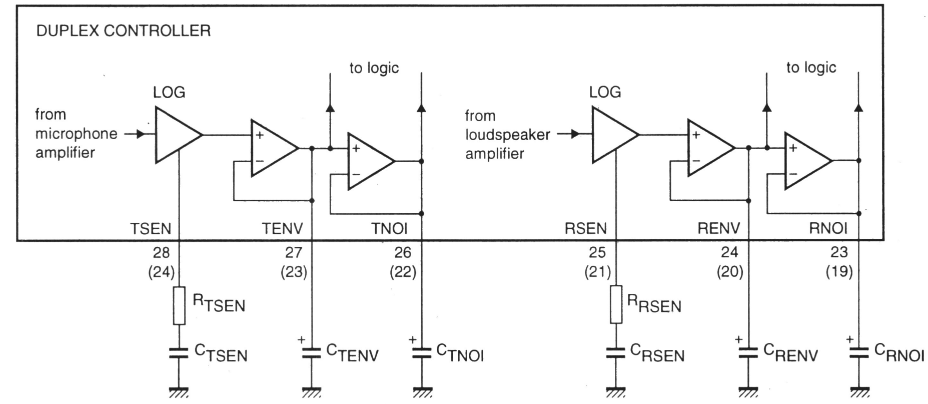
SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelope detectors are shown in Fig.7.

For the transmit channel, the input signal at MIC is 40 dB amplified to TSEN. For the receive channel, the differential signal between RIN1 and RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first-order high-pass filter. In the basic application, see Fig.13, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is sufficient to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is sufficient for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signals on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 µA and a maximum sink current of 120 µA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.13 the value of both capacitors is 4.7 µF. At room temperature, the 1 µA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 µA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.8.


DUPLEX CONTROLLER
to logic
LOG
from microphone amplifier
+
−
TSEN
TENV
TNOI
28
(24)
27
(23)
26
(22)
R TSEN
C TSEN
C TENV
C TNOI
to logic
LOG
from loudspeaker amplifier
RSEN
RENV
RNOI
25
(21)
24
(20)
23
(19)
R RSEN
C RSEN
C RENV
C RNOI
MGD223

The pin numbers given in parenthesis refer to the TEA1094A.

Fig.7 Signal and noise envelope detectors.

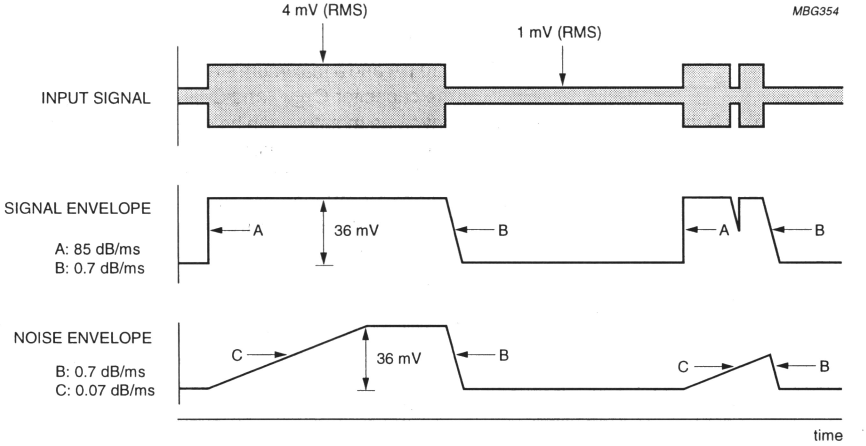
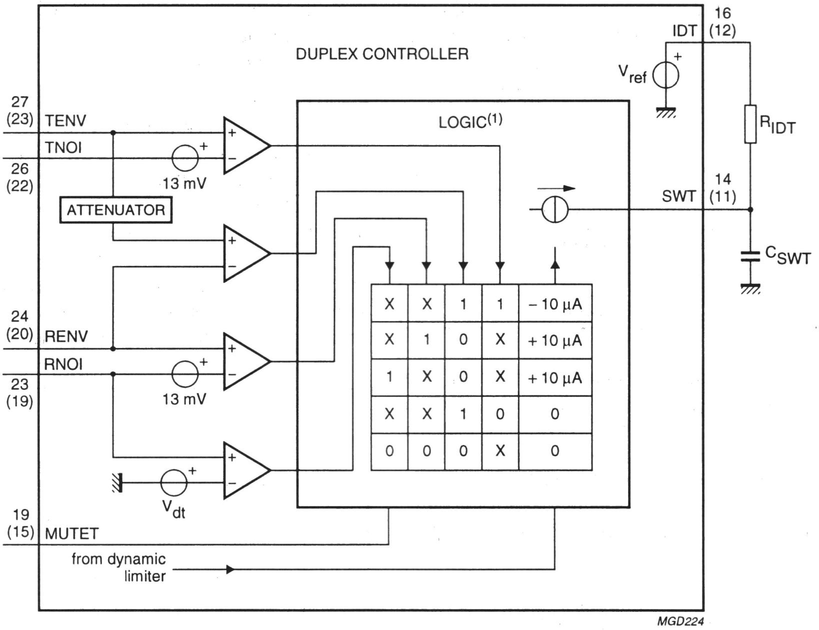


Fig.8 Signal and noise envelope waveforms.

DECISION LOGIC: PINS IDT AND SWT



X	X	1	1	−10 μA
X	1	0	X	+10 μA
1	X	0	X	+10 μA
X	X	1	0	0
0	0	0	X	0

The pin numbers given in parenthesis refer to the TEA1094A.

(1) When MUTET = HIGH, +10 μA is forced.
When DLC/$\overline{\text{MUTER}}$ < 0.2 V, −10 μA is forced.

Fig.9 Decision logic.

The TEA1094; TEA1094A select their modes of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV} - V_{NOI}$ = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1094; TEA1094A to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard applications, does not consider input signals between RIN1 and RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.9, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 µA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1094; TEA1094A and can vary between −400 and +400 mV (see Table 1).

Table 1 Modes of TEA1094; TEA1094A.

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.13, C_{SWT} is 220 nF and R_{IDT} is 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time, from receive mode or transmit mode to idle mode, is equal to 4 × $R_{IDT}C_{SWT}$ and is approximately 2 seconds (idle mode time).

The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 µA thus resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ goes lower than 0.2 V, the capacitor C_{SWT} is discharged with 10 µA thus resulting in the transmit mode.

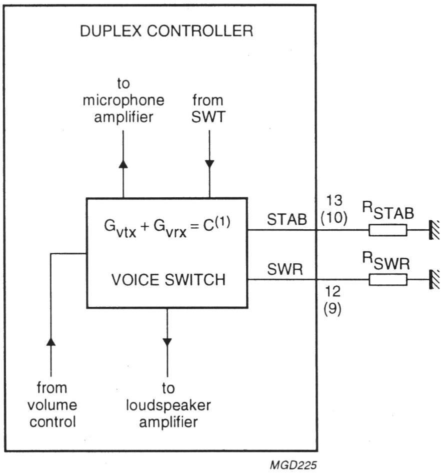
VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.10. With the voltage on SWT, the TEA1094; TEA1094A voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.13, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.11.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.11). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.



The pin numbers given in parenthesis refer to the TEA1094A.
(1) C = constant.

Fig.10 Voice switch.

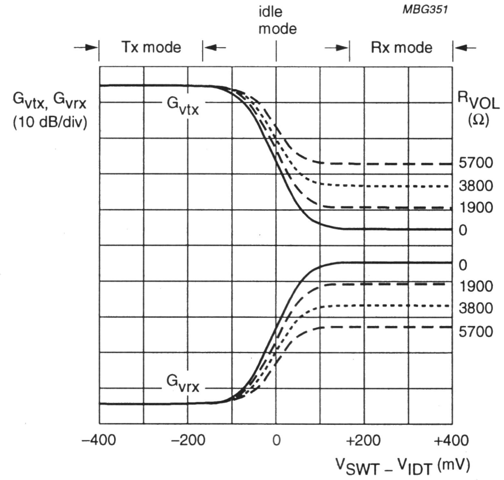


Fig.11 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB}, RIN1 and RIN2		$V_{GND} - 0.4$	$V_{BB} + 0.4$	V
$V_{RIN(max)}$	maximum voltage on pins RIN1 and RIN2		$V_{GND} - 1.2$	$V_{BB} + 0.4$	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		$V_{GND} - 0.4$	12.0	V
P_{tot}	total power dissipation	T_{amb} = 75 °C			
	TEA1094		–	1000	mW
	TEA1094A		–	910	mW
	TEA1094T		–	625	mW
	TEA1094AT		–	590	mW
T_{stg}	IC storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1094	45	K/W
	TEA1094A	50	K/W
	TEA1094T	70	K/W
	TEA1094AT	75	K/W

CHARACTERISTICS

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTET = LOW; PD = LOW (TEA1094A only); R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, GND and PD)						
V_{BB}	supply voltage		3.3	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	3.1	4.4	mA
POWER-DOWN INPUT PD (TEA1094A ONLY)						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	input current	PD = HIGH	–	2.5	5	μA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down condition	PD = HIGH	–	180	240	μA
Microphone channel (MIC, GAT, MOUT, MUTET and MICGND)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pins MIC and MICGND		17	20	23	kΩ
G_{vtx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	13	15.5	18	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAT}		–15.5	–	+15.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT	pin MIC connected to MICGND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–100	–	dBmp

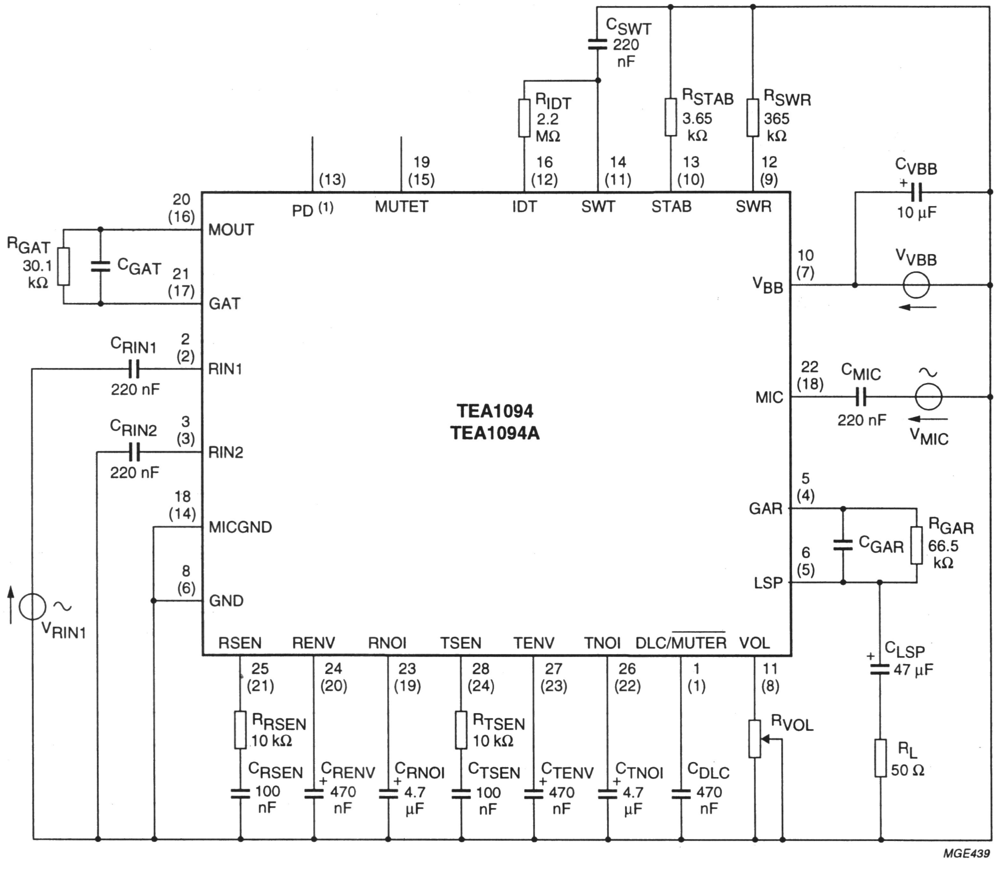
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit mute input MUTET						
V_{IL}	LOW level input voltage		$V_{GND} - 0.4$	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	$V_{BB} + 0.4$	V
I_{MUTET}	input current	MUTET = HIGH	–	2.5	5	µA
ΔG_{vtxm}	voltage gain reduction with MUTET active	MUTET = HIGH	–	80	–	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP and DLC/$\overline{\text{MUTER}}$)						
Loudspeaker amplifier						
$\lvert Z_i \rvert$	input impedance	between pins RIN1 or RIN2 and GND	17	20	23	kΩ
		between pins RIN1 and RIN2	34	40	46	kΩ
G_{vrx}	voltage gain in receive mode; between RIN1 and RIN2 to LSP	V_{RIN} = 20 mV (RMS)	16	18.5	21	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		−18.5	–	+14.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$V_{RIN(rms)}$	maximum input voltage between RIN1 and RIN2 (RMS value)	R_{GAR} = 11.8 kΩ; for 2% THD in input stage	–	390	–	mV
$V_{norx(rms)}$	noise output voltage at pin LSP (RMS value)	inputs RIN1 and RIN2 short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve)	–	80	–	µV
CMRR	common mode rejection ratio		–	50	–	dB
ΔG_{vrxv}	voltage gain variation related to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
Output capability						
$V_{OSE(p-p)}$	output voltage (peak-to-peak value)	V_{RIN} = 300 mV (RMS); note 1	3.5	4.5	–	V
		V_{RIN} = 150 mV (RMS); R_{GAR} = 374 kΩ; R_L = 33 Ω; V_{BB} = 9.0 V; note 2	–	7.5	–	V
I_{OM}	maximum output current at LSP (peak value)		150	500	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; $t > t_{att}$	–	0.9	5	%
$V_{BB(th)}$	V_{BB} limiter threshold		–	2.9	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$		–	1	–	ms
MUTE RECEIVE						
$V_{DLC(th)}$	threshold voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4	–	0.2	V
$I_{DLC(th)}$	threshold current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	100	–	μA
ΔG_{vrxm}	voltage gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN, RENV, RNOI and TNOI)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from MIC to TSEN		37.5	40	42.5	dB
$G_{v(RSEN)}$	voltage gain between RIN1 and RIN2 to RSEN		−2.5	0	+2.5	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\Delta V_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 μA	–	18	–	mV
$\Delta V_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 μA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	μA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	μA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 μA is sourced from both RSEN and TSEN; envelope detectors tracking; note 3	–	±3	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	μA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	μA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 5 μA is sourced from both RSEN and TSEN; noise detectors tracking; note 3	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pins RIN1 and RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 4	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 4	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	μA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	μA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	μA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to 365 kΩ	−40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to 50 mW output power.
2. Corresponds to 200 mW output power.
3. Corresponds to ±1 dB tracking.
4. Corresponds to 4.3 dB noise/speech recognition level.


TEA1094
TEA1094A
MOUT
GAT
RIN1
RIN2
MICGND
GND
PD (1)
MUTET
IDT
SWT
STAB
SWR
VBB
MIC
GAR
LSP
RSEN
RENV
RNOI
TSEN
TENV
TNOI
DLC/MUTER
VOL
R_{GAT} 30.1 kΩ
C_{GAT}
C_{RIN1} 220 nF
C_{RIN2} 220 nF
V_{RIN1}
C_{SWT} 220 nF
R_{IDT} 2.2 MΩ
R_{STAB} 3.65 kΩ
R_{SWR} 365 kΩ
C_{VBB} 10 µF
V_{VBB}
C_{MIC} 220 nF
V_{MIC}
C_{GAR}
R_{GAR} 66.5 kΩ
C_{LSP} 47 µF
R_L 50 Ω
R_{RSEN} 10 kΩ
C_{RSEN} 100 nF
C_{RENV} 470 nF
C_{RNOI} 4.7 µF
R_{TSEN} 10 kΩ
C_{TSEN} 100 nF
C_{TENV} 470 nF
C_{TNOI} 4.7 µF
C_{DLC} 470 nF
R_{VOL}
MGE439

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

Fig.12 Test circuit.

APPLICATION INFORMATION

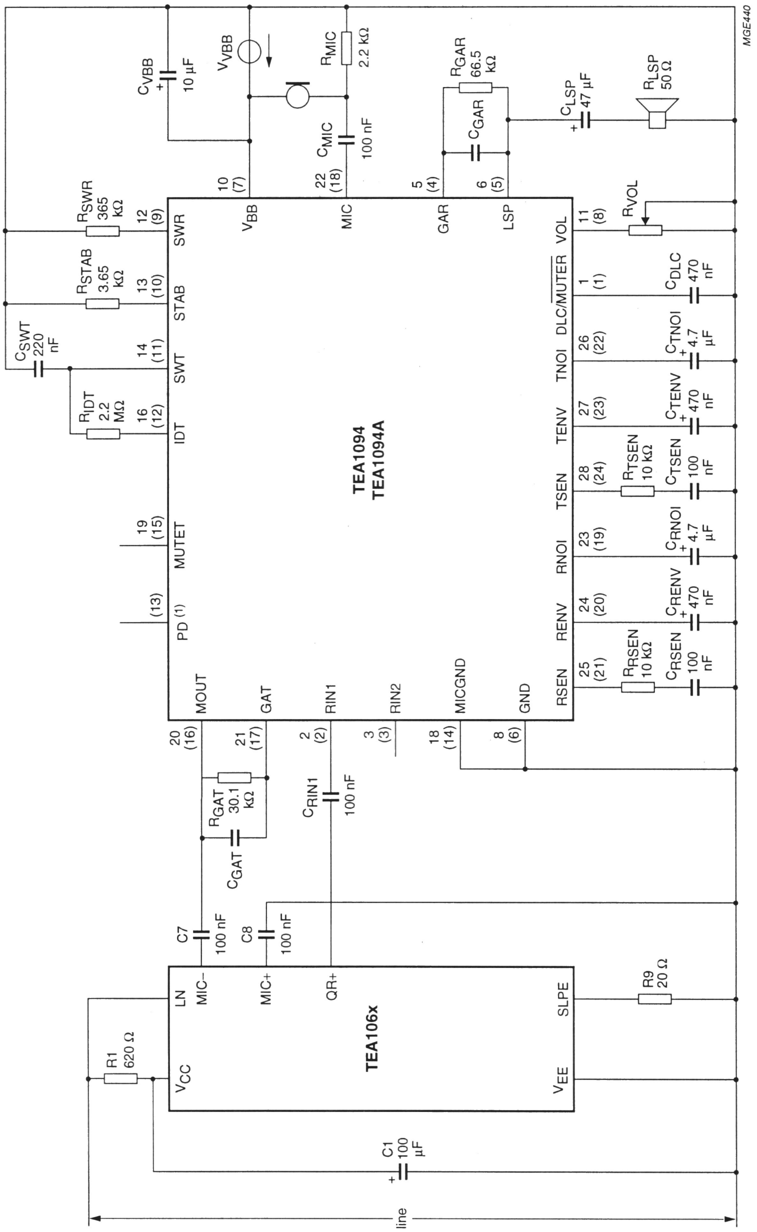
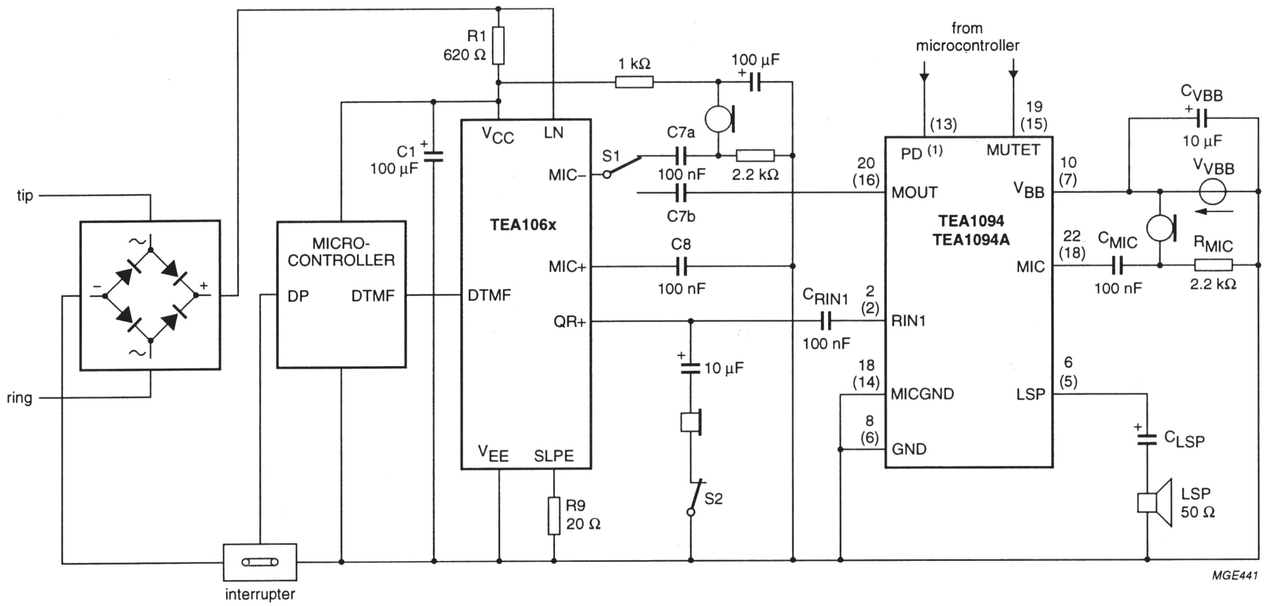

MGE440
C_VBB 10 µF
V_VBB
R_MIC 2.2 kΩ
C_MIC 100 nF
R_GAR 66.5 kΩ
C_GAR
C_LSP 47 µF
R_LSP 50 Ω
R_SWR 365 kΩ
R_STAB 3.65 kΩ
C_SWT 220 nF
R_IDT 2.2 MΩ
R_VOL
C_DLC 470 nF
C_TNOI 4.7 µF
C_TENV 470 nF
R_TSEN 10 kΩ
C_TSEN 100 nF
C_RNOI 4.7 µF
C_RENV 470 nF
R_RSEN 10 kΩ
C_RSEN 100 nF
TEA1094
TEA1094A
SWR 12 (9)
STAB 13 (10)
SWT 14 (11)
IDT 16 (12)
MUTET 19 (15)
PD (1) (13)
V_BB 10 (7)
MIC 22 (18)
GAR 5 (4)
LSP 6 (5)
VOL 11 (8)
DLC/MUTER 1 (1)
TNOI 26 (22)
TENV 27 (23)
TSEN 28 (24)
RNOI 23 (19)
RENV 24 (20)
RSEN 25 (21)
MOUT 20 (16)
GAT 21 (17)
RIN1 2 (2)
RIN2 3 (3)
MICGND 18 (14)
GND 8 (6)
R_GAT 30.1 kΩ
C_GAT
C_RIN1 100 nF
C7 100 nF
C8 100 nF
TEA106x
LN
MIC−
MIC+
QR+
SLPE
V_CC
V_EE
R1 620 Ω
R9 20 Ω
C1 100 µF
line

Fig.13 Basic application diagram.

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.


tip
ring
~
~
+
-
interrupter
MICRO-
CONTROLLER
DP
DTMF
C1
100 µF
+
R1
620 Ω
VCC
LN
MIC−
MIC+
DTMF
QR+
VEE
SLPE
TEA106x
R9
20 Ω
S1
1 kΩ
100 µF
+
C7a
100 nF
2.2 kΩ
C7b
C8
100 nF
+
10 µF
S2
CRIN1
100 nF
from
microcontroller
(13)
19
(15)
PD (1)
MUTET
20
(16)
MOUT
2
(2)
RIN1
18
(14)
MICGND
8
(6)
GND
TEA1094
TEA1094A
10
(7)
VBB
22
(18)
MIC
6
(5)
LSP
CVBB
+
10 µF
VVBB
CMIC
100 nF
RMIC
2.2 kΩ
+
CLSP
LSP
50 Ω
MGE441

The pin numbers given in parenthesis refer to the TEA1094A.

(1) TEA1094A only.

Fig.14 Application example.

Voice switched speakerphone IC TEA1095

FEATURES

- External power supply with power-down function
- Transmit channel with:
  - externally adjustable gain
  - transmit mute function
- Receive channel with:
  - externally adjustable gain
  - logarithmic volume control via a linear potentiometer
  - receive mute function
- Duplex controller consisting of:
  - signal envelope and noise envelope monitors for both channels with:

    externally adjustable sensitivity

    externally adjustable signal envelope time constant

    externally adjustable noise envelope time constant
  - decision logic with:

    externally adjustable switch-over timing

    externally adjustable idle mode timing

    externally adjustable dial tone detector in receive channel
  - voice switch control with:

    adjustable switching range

    constant sum of gain during switching

    constant sum of gain at different volume settings.

APPLICATIONS

- Mains, battery or line-powered telephone sets
- Cordless telephones
- Answering machines
- Fax machines
- Hands-free car kits.

GENERAL DESCRIPTION

The TEA1095 is a bipolar circuit, that in conjunction with a member of the TEA106X, TEA111X families of transmission or TEA1096 transmission/listening-in circuits offers a hands-free function. It incorporates a transmit amplifier, a receiver channel amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1095	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TEA1095T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

QUICK REFERENCE DATA

V_{BB} = 5 V; V_{GND} = 0 V; f = 1 kHz; T_{amb} = 25 °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; R_{VOL} = 0 Ω; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
G_{vtx}	voltage gain from TXIN to TXOUT in transmit mode	V_{TXIN} = 1 mV (RMS); R_{GATX} = 30.1 kΩ	–	15.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GATX}		−15.5	–	+24.5	dB
G_{vrx}	voltage gain from RXIN to RXOUT in receive mode	V_{RXIN} = 20 mV (RMS); R_{GARX} = 16.5 kΩ	–	6.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GARX}		−20.5	–	+19.5	dB
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to R_{SWR} = 365 kΩ	−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

BLOCK DIAGRAM

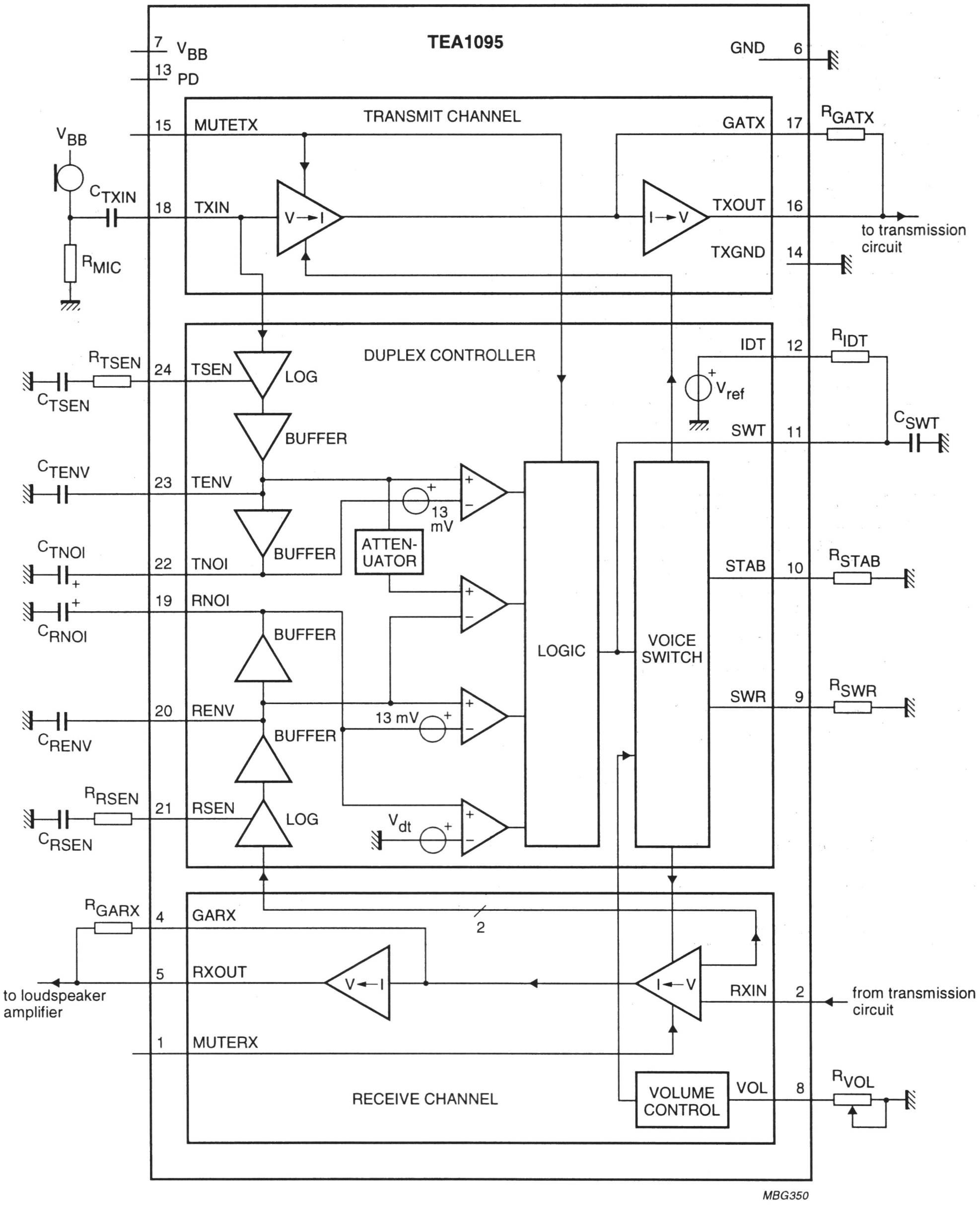

TEA1095
7 VBB
13 PD
GND 6
TRANSMIT CHANNEL
15 MUTETX
GATX 17
RGATX
VBB
CTXIN
18 TXIN
V→I
I→V
TXOUT 16
to transmission circuit
TXGND 14
RMIC
DUPLEX CONTROLLER
IDT 12
RIDT
RTSEN
24 TSEN
LOG
CTSEN
Vref
SWT 11
CSWT
BUFFER
CTENV
23 TENV
13 mV
BUFFER
ATTEN-UATOR
CTNOI
22 TNOI
STAB 10
RSTAB
19 RNOI
CRNOI
BUFFER
LOGIC
VOICE SWITCH
SWR 9
RSWR
20 RENV
CRENV
13 mV
BUFFER
RRSEN
21 RSEN
LOG
Vdt
CRSEN
RGARX
4 GARX
2
5 RXOUT
V←I
I←V
RXIN 2
to loudspeaker amplifier
from transmission circuit
1 MUTERX
RECEIVE CHANNEL
VOLUME CONTROL
VOL 8
RVOL
MBG350

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MUTERX	1	receiver channel mute input
RXIN	2	receiver amplifier input
n.c.	3	not connected
GARX	4	receiver gain adjustment
RXOUT	5	receiver amplifier output
GND	6	ground reference
V_{BB}	7	supply voltage input
VOL	8	receiver volume adjustment
SWR	9	switching range adjustment
STAB	10	reference current adjustment
SWT	11	switch-over timing adjustment
IDT	12	idle mode timing adjustment
PD	13	power-down input
TXGND	14	ground reference for the transmit channel
MUTETX	15	transmit channel mute input
TXOUT	16	transmit amplifier output
GATX	17	transmit gain adjustment
TXIN	18	transmit amplifier input
RNOI	19	receive noise envelope timing adjustment
RENV	20	receive signal envelope timing adjustment
RSEN	21	receive signal envelope sensitivity adjustment
TNOI	22	transmit noise envelope timing adjustment
TENV	23	transmit signal envelope timing adjustment
TSEN	24	transmit signal envelope sensitivity adjustment

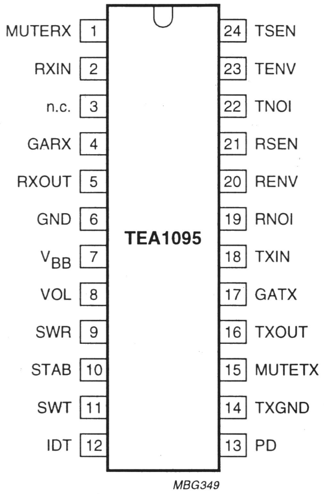

MUTERX 1
RXIN 2
n.c. 3
GARX 4
RXOUT 5
GND 6
VBB 7
VOL 8
SWR 9
STAB 10
SWT 11
IDT 12
TEA1095
24 TSEN
23 TENV
22 TNOI
21 RSEN
20 RENV
19 RNOI
18 TXIN
17 GATX
16 TXOUT
15 MUTETX
14 TXGND
13 PD
MBG349

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in the functional description are typical values except when otherwise specified.

A principle diagram of the TEA1096 is shown on the left side of Fig.3. The TEA1096 is a transmission and listening-in circuit. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone, a loudspeaker amplifier and a hybrid. For more details on the TEA1096 circuit (please refer to *Data Handbook IC03*). The right side of Fig.3 shows a principle diagram of the TEA1095, a hands-free add-on circuit with a transmit amplifier, a receiver amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1095 detects which channel has the 'largest' signal and then controls the gains of the transmit amplifier and the receiver amplifier such that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the transmit amplifier is at its maximum and the gain of the receiver amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the receiver amplifier is at its maximum and the gain of the transmit amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

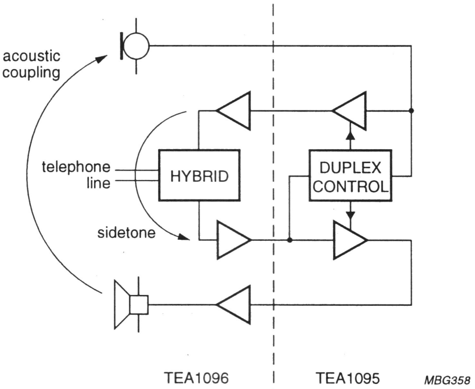


Fig.3 Hands-free telephone set principles.

Supply: pins V_{BB}, GND and PD

The TEA1095 must be supplied with an external stabilized voltage source between pins V_{BB} and GND. In idle mode, without any signal, the internal supply current is 2.7 mA at V_{BB} = 5 V.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1095 is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from V_{BB} is 140 μA.

Transmit channel: pins TXIN, GATX, TXOUT, TXGND and MUTETX

The TEA1095 has an asymmetrical transmit input (TXIN) with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin TXOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the transmit amplifier (from pin TXIN to TXOUT) can be adjusted from 0 dB to 40 dB to suit application specific requirements. The gain is proportional to the value of R_{GATX} and equals 15.5 dB with R_{GATX} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GATX} to ensure stability of the transmit amplifier. Together with R_{GATX}, it also provides a first-order low-pass filter.

By applying a HIGH level on pin MUTETX, the transmit amplifier is muted and the TEA1095 is automatically forced into the receive mode.

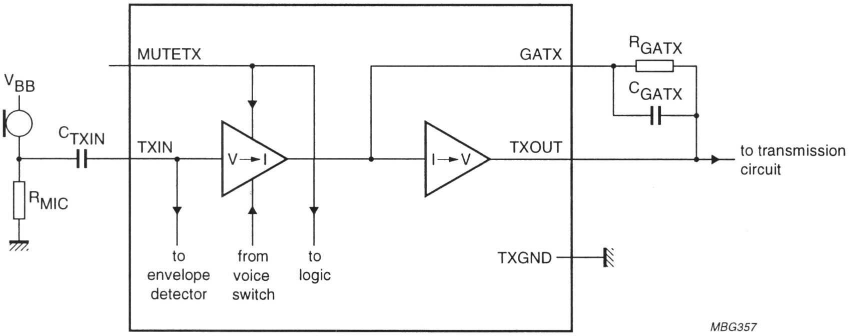


Fig.4 Transmit channel.

Receive channel

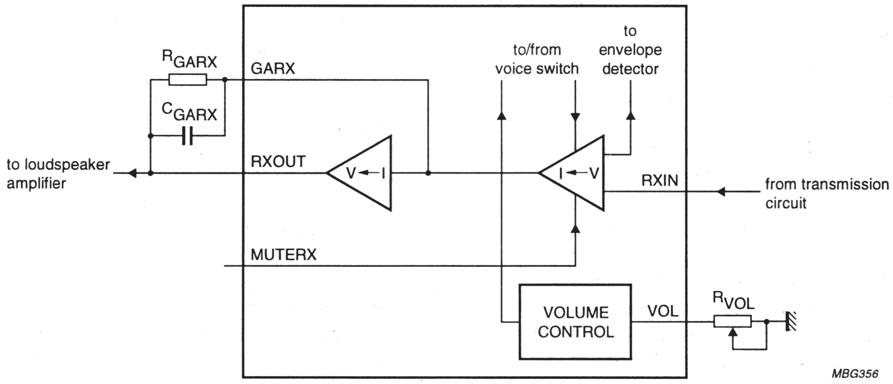


Fig.5 Receive channel.

RECEIVER AMPLIFIER: PINS RXIN, GARX, RXOUT AND MUTERX

The TEA1095 has an asymmetrical input (RXIN) for the receiver amplifier with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1095. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free.

In the receive mode, the overall gain of the receive amplifier can be adjusted from −14 dB to +26 dB to suit application specific requirements. The gain from RXIN to RXOUT is proportional to the value of R_{GARX} and equals 6.5 dB with R_{GARX} = 16.5 kΩ. A capacitor connected in parallel with R_{GARX} can be used to provide a first-order low-pass filter.

By applying a HIGH level on pin MUTERX, the receiver amplifier is muted and the TEA1095 is automatically forced into the transmit mode.

VOLUME CONTROL: PIN VOL

The receiver amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control of the gain of the receiver amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS: PINS TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelopes detectors are shown in Fig.6.

For the transmit channel, the input signal at TXIN is 40 dB amplified to TSEN. For the receive channel, the input signal at RXIN is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}.

The capacitors connected in series with the two resistors block any DC component and form a first order high-pass filter. In the basic application (see Fig.12), it is assumed that V_{TXIN} = 1 mV (RMS) and V_{RXIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitors C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is enough to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is enough for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 μA and a maximum sink current of 120 μA. Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.12, the value of both capacitors is 4.7 μF. At room temperature, the 1 μA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120 μA current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.7.

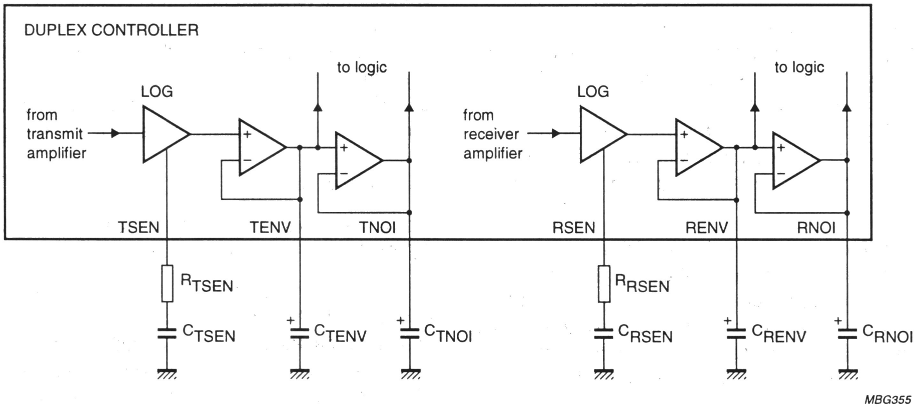


Fig.6 Signal and noise envelope detectors.

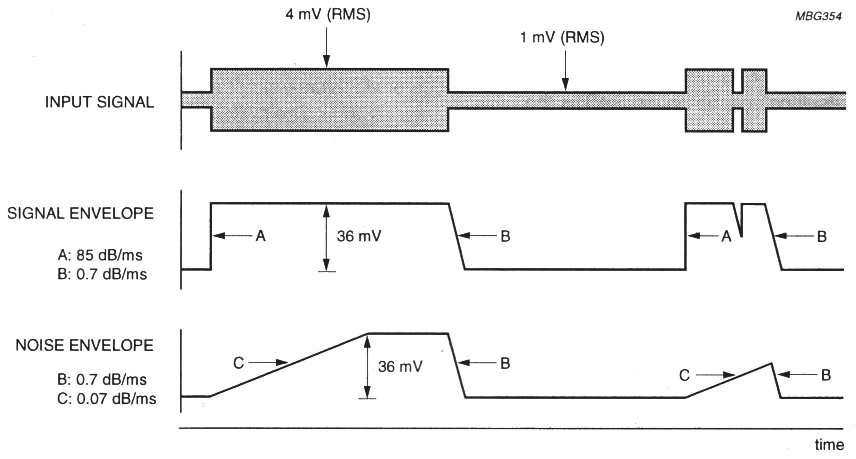
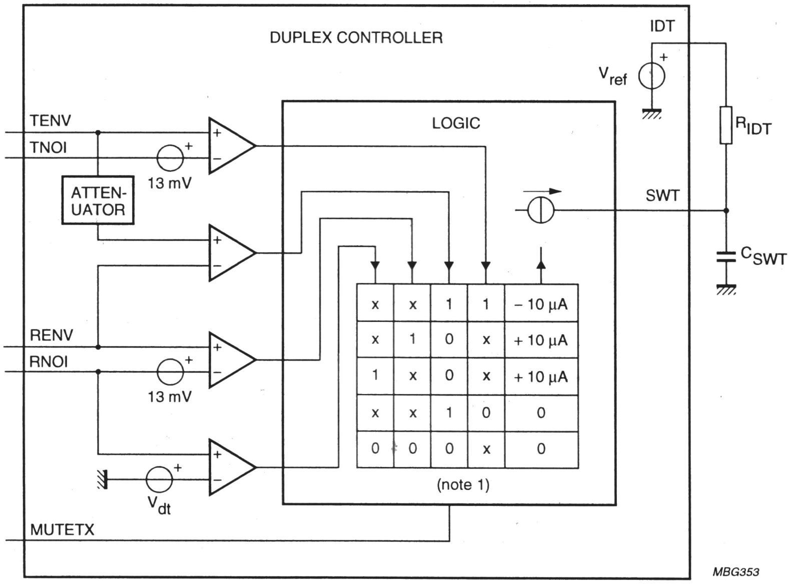


Fig.7 Signal and noise envelope waveforms.


DUPLEX CONTROLLER
IDT
V_ref
+
LOGIC
R_IDT
TENV
TNOI
+
13 mV
ATTEN-UATOR
SWT
C_SWT
RENV
RNOI
+
13 mV
+
V_dt
(note 1)
MUTETX
MBG353

x	x	1	1	− 10 µA
x	1	0	x	+ 10 µA
1	x	0	x	+ 10 µA
x	x	1	0	0
0	0	0	x	0

(1) When MUTETX = HIGH +10 µA is forced. When MUTERX = HIGH −10 µA is forced.

Fig.8 Decision logic.

DECISION LOGIC: PINS IDT AND SWT

The TEA1095 selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV-NOI}$ = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on TXIN contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the transmit amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1095 to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard application, does not consider the input signals at RXIN as noise when they have a level greater than 42 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.8, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 µA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1095 and can vary between −400 mV and +400 mV.

Table 1 Modes of TEA1095

$V_{SWT} - V_{IDT}$ (mV)	MODE
<−180	transmit mode
0	idle mode
>180	receive mode

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.12, C_{SWT} is chosen at 220 nF and R_{IDT} at 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time from receive mode or transmit mode to idle mode is equal to 4 × R_{IDT} C_{SWT} and is approximately 2 s (idle mode time).

The inputs MUTETX and MUTERX overrule the decision logic. When MUTETX goes HIGH, the capacitor C_{SWT} is charged with 10 µA resulting in the receive mode. When the voltage on pin MUTERX goes HIGH, the capacitor C_{SWT} is discharged with 10 µA resulting in the transmit mode.

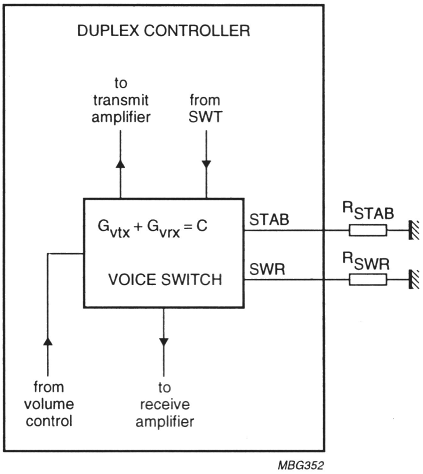
VOICE-SWITCH: PINS STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.9. With the voltage on SWT, the TEA1095 voice-switch regulates the gains of the transmit and the receive channel such that the sum of both is kept constant.

In the transmit mode, the gain of the transmit amplifier is at its maximum and the gain of the receive amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both transmit and receive amplifier gains are halfway.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be equal to 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.12, R_{SWR} is equal to 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.10.

In the receive mode, the gain of the receive amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the transmit amplifier is increased at the same time (see dashed curves in Fig.10). In the transmit mode however, the volume control has no influence on the gain of the transmit amplifier or the gain of the receive amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.


DUPLEX CONTROLLER
to transmit amplifier
from SWT
$G_{vtx} + G_{vrx} = C$
VOICE SWITCH
STAB
SWR
R_{STAB}
R_{SWR}
from volume control
to receive amplifier
MBG352

Where C = constant.

Fig.9 Voice switch.

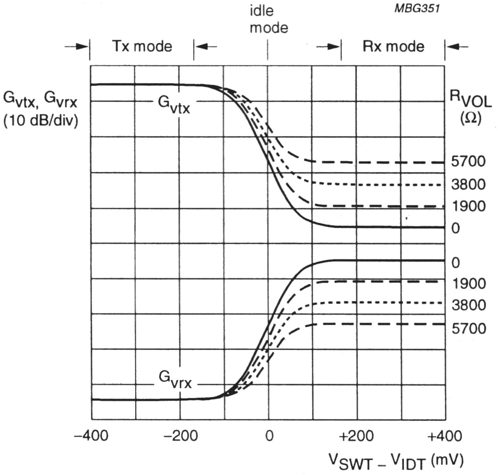


Fig.10 Switch-over behaviour.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{n(max)}$	maximum voltage on all pins; except pins V_{BB} and RXIN		$V_{GND} - 0.4$	$V_{BB} + 0.4$	V
$V_{RIN(max)}$	maximum voltage on pin RXIN		$V_{GND} - 1.2$	$V_{BB} + 0.4$	V
$V_{BB(max)}$	maximum voltage on pin V_{BB}		$V_{GND} - 0.4$	12.0	V
T_{stg}	IC storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1095	50	K/W
	TEA1095T	75	K/W

CHARACTERISTICS

$V_{BB} = 5$ V; $V_{GND} = 0$ V; f = 1 kHz; $T_{amb} = 25$ °C; MUTETX = LOW; MUTERX = LOW; PD = LOW; $R_{VOL} = 0\ \Omega$; measured in test circuit of Fig.11; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (V_{BB}, PD and GND)						
V_{BB}	supply voltage		2.9	–	12.0	V
I_{BB}	current consumption from pin V_{BB}		–	2.7	3.8	mA
POWER-DOWN INPUT PD						
V_{IL}	LOW level input voltage		$V_{GND} - 0.4$	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	$V_{BB} + 0.4$	V
I_{PD}	power-down input current	PD = HIGH	–	2.5	5	μA
$I_{BB(PD)}$	current consumption from pin V_{BB} in power-down mode	PD = HIGH	–	140	190	μA
Transmit channel (TXIN, GATX, TXOUT, MUTETX and TXGND)						
TRANSMIT AMPLIFIER						
$\lvert Z_i \rvert$	input impedance between pins TXIN and TXGND		17	20	23	kΩ
G_{vtx}	voltage gain from TXIN to TXOUT in transmit mode	$V_{TXIN} = 1$ mV (RMS); $R_{GATX} = 30.1$ kΩ	–	15.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GATX}		−15.5	–	+24.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	$V_{TXIN} = 1$ mV (RMS); $T_{amb} = -25$ to +75 °C	–	±0.3	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	$V_{TXIN} = 1$ mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{notx}	noise output voltage at pin TXOUT	pin TXIN connected to TXGND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–100	–	dBmp
TRANSMIT MUTE INPUT MUTETX						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTETX}	input current	MUTETX = HIGH	–	2.5	5	μA
ΔG_{vtxm}	voltage gain reduction with MUTETX active	MUTETX = HIGH	–	80	–	dB
Receive channel (RXIN, GARX, RXOUT and MUTERX)						
RECEIVE AMPLIFIER						
$\lvert Z_i \rvert$	input impedance between pins RXIN and GND		17	20	23	kΩ
G_{vrx}	voltage gain from RXIN to RXOUT in receive mode	V_{RXIN} = 20 mV (RMS); R_{GARX} = 16.5 kΩ	–	6.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GARX}		–20.5	–	+19.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C	V_{RXIN} = 20 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	V_{RXIN} = 20 mV (RMS); f_i = 300 to 3400 Hz	–	±0.3	–	dB
$V_{norx(rms)}$	noise output voltage at pin RXOUT (RMS value)	input RXIN short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	20	–	μV
ΔG_{vrxv}	voltage gain variation referenced to ΔR_{VOL} = 950 Ω	when total attenuation does not exceed the switching range	–	3	–	dB
RECEIVE MUTE INPUT MUTERX						
V_{IL}	LOW level input voltage		V_{GND} – 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{MUTERX}	input current	MUTERX = HIGH	–	2.5	5	μA
ΔG_{vrxm}	gain reduction with MUTERX active	MUTERX = HIGH	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Envelope and noise detectors (TSEN, TENV, TNOI, RSEN, RENV and RNOI)						
PREAMPLIFIERS						
$G_{v(TSEN)}$	voltage gain from TXIN to TSEN		–	40	–	dB
$G_{v(RSEN)}$	voltage gain between RXIN to RSEN		–	0	–	dB
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
$\varphi_{det(TSEN)}$	sensitivity detection on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 µA	–	18	–	mV
$\varphi_{det(RSEN)}$	sensitivity detection on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 µA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
$I_{source(ENV)}$	maximum current sourced from pin TENV or RENV		–	120	–	µA
$I_{sink(ENV)}$	maximum current sunk by pin TENV or RENV		0.75	1	1.25	µA
ΔV_{ENV}	voltage difference between pins RENV and TENV	when 10 µA is sourced from both RSEN and TSEN; envelope detectors tracking; note 1	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
$I_{source(NOI)}$	maximum current sourced from pins TNOI or RNOI		0.75	1	1.25	µA
$I_{sink(NOI)}$	maximum current sunk by pins TNOI or RNOI		–	120	–	µA
ΔV_{NOI}	voltage difference between pins RNOI and TNOI	when 2 µA is sourced from both RSEN and TSEN; noise detectors tracking; note 1	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(rms)}$	threshold level at pin RXIN (RMS value)		–	42	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
$\Delta V_{Srx(th)}$	threshold voltage between pins RENV and RNOI to switch-over from receive to idle mode	$V_{RXIN} < V_{RINDT}$; note 2	–	13	–	mV
$\Delta V_{Stx(th)}$	threshold voltage between pins TENV and TNOI to switch-over from transmit to idle mode	note 2	–	13	–	mV
SWITCH-OVER						
$I_{source(SWT)}$	current sourced from pin SWT when switching to receive mode		7.5	10	12.5	μA
$I_{sink(SWT)}$	current sunk by pin SWT when switching to transmit mode		7.5	10	12.5	μA
$I_{idle(SWT)}$	current sourced from pin SWT in idle mode		–	0	–	μA
Voice switch (STAB and SWR)						
SWRA	switching range		–	40	–	dB
ΔSWRA	switching range adjustment	with R_{SWR} referenced to $R_{SWR} = 365\ k\Omega$	−40	–	+12	dB
$\lvert\Delta G_v\rvert$	voltage gain variation from transmit mode to idle mode on both channels		–	20	–	dB
G_{tr}	gain tracking ($G_{vtx} + G_{vrx}$) during switching, referenced to idle mode		–	±0.5	–	dB

Notes

1. Corresponds to ±1 dB tracking.
2. Corresponds to 4.3 dB noise/speech recognition level.

TEST AND APPLICATION INFORMATION

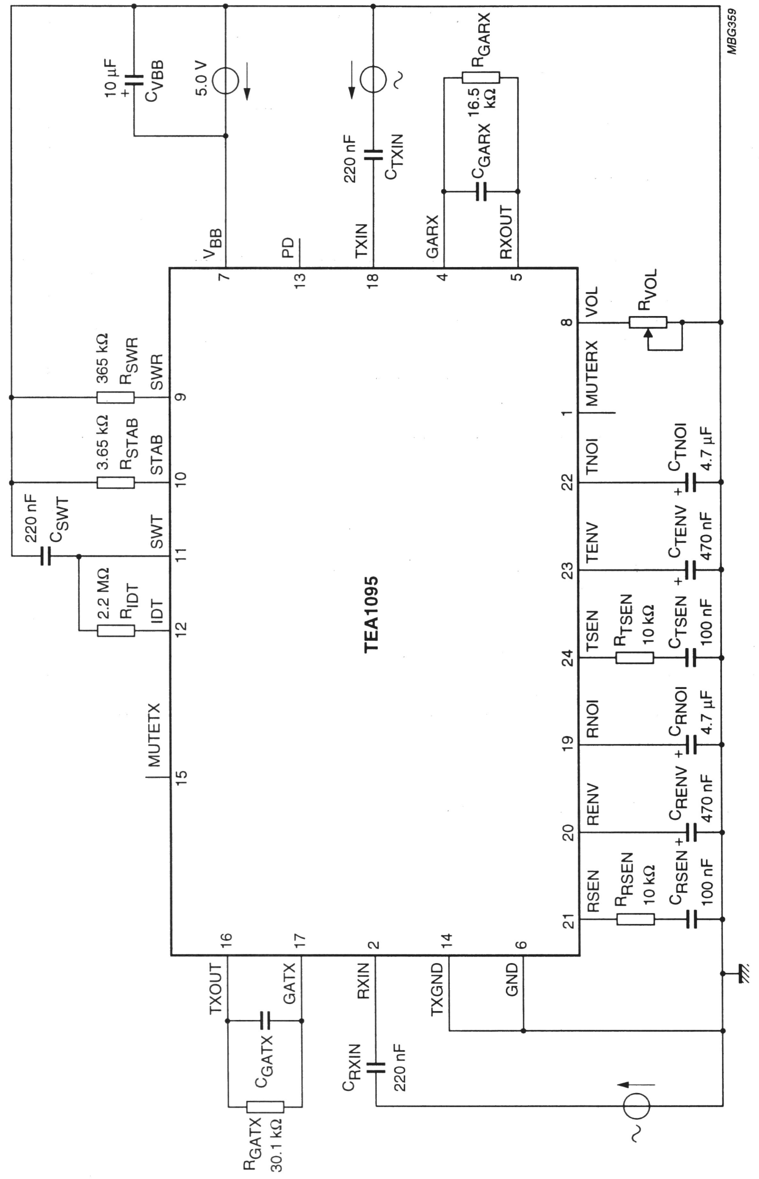

10 µF
C_{VBB}
5.0 V
220 nF
C_{TXIN}
R_{GARX}
16.5 kΩ
C_{GARX}
MBG359
V_{BB}
PD
TXIN
GARX
RXOUT
7
13
18
4
5
VOL
R_{VOL}
8
MUTERX
1
TNOI
22
C_{TNOI}
4.7 µF
TENV
23
C_{TENV}
470 nF
TSEN
24
R_{TSEN}
10 kΩ
C_{TSEN}
100 nF
RNOI
19
C_{RNOI}
4.7 µF
RENV
20
C_{RENV}
470 nF
RSEN
21
R_{RSEN}
10 kΩ
C_{RSEN}
100 nF
365 kΩ
R_{SWR}
SWR
9
3.65 kΩ
R_{STAB}
STAB
10
220 nF
C_{SWT}
SWT
11
2.2 MΩ
R_{IDT}
IDT
12
MUTETX
15
TEA1095
16
17
2
14
6
TXOUT
GATX
RXIN
TXGND
GND
C_{GATX}
R_{GATX}
30.1 kΩ
C_{RXIN}
220 nF

Fig.11 Test circuit.

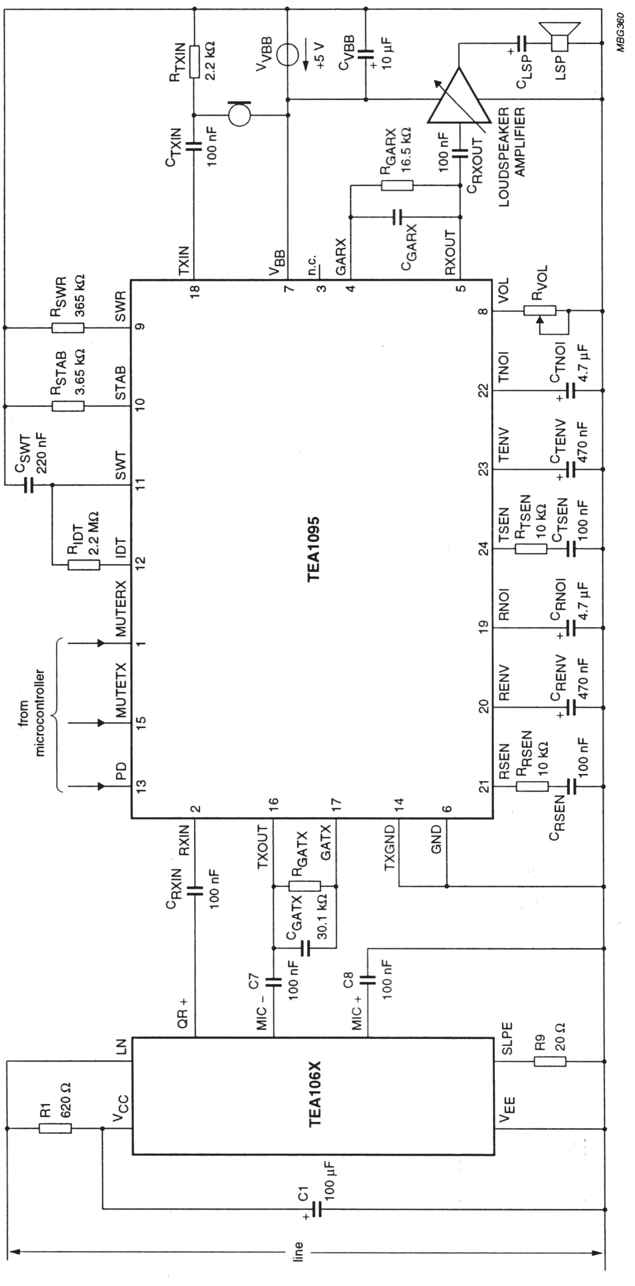
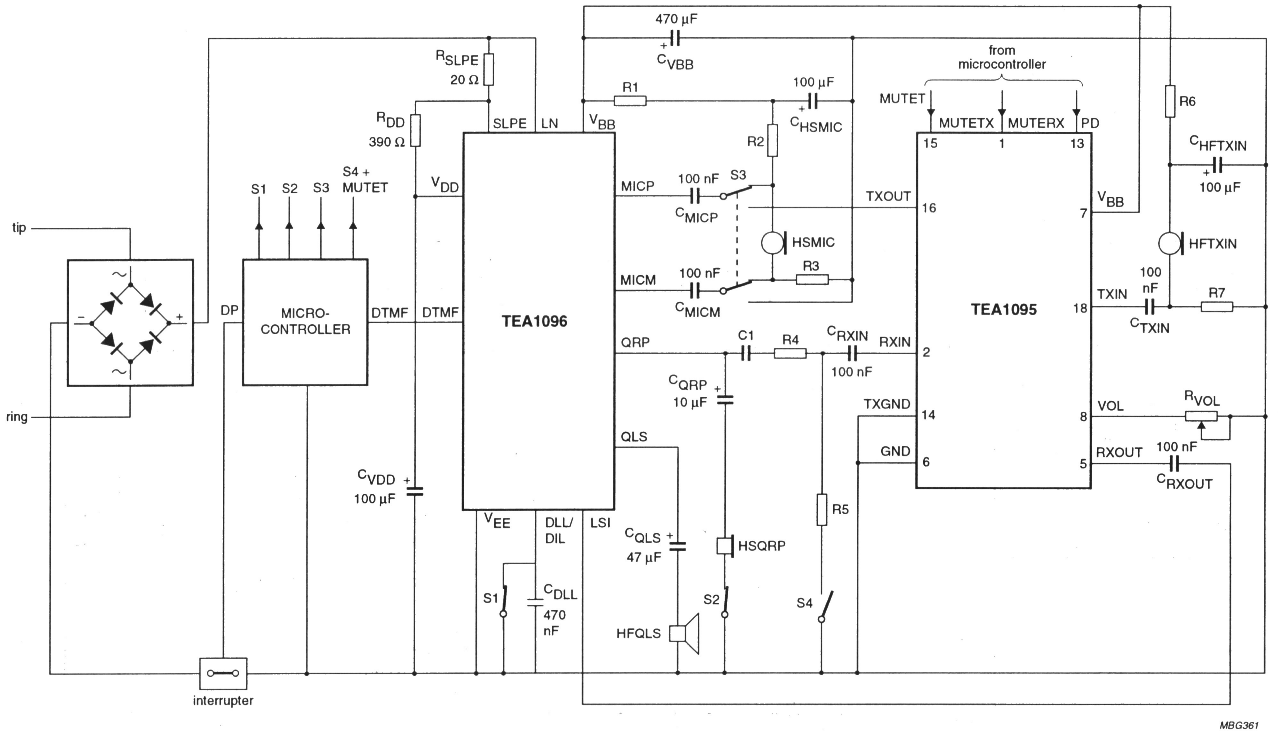

TEA1095
TEA106X
RTXIN 2.2 kΩ
CTXIN 100 nF
VVBB +5 V
CVBB 10 µF
CLSP
LSP
LOUDSPEAKER AMPLIFIER
RGARX 16.5 kΩ
CRXOUT 100 nF
CGARX
TXIN 18
VBB 7
n.c. 3
GARX 4
RXOUT 5
VOL 8
RVOL
TNOI 22
CTNOI 4.7 µF
TENV 23
CTENV 470 nF
TSEN 24
RTSEN 10 kΩ
CTSEN 100 nF
RNOI 19
CRNOI 4.7 µF
RENV 20
CRENV 470 nF
RSEN 21
RRSEN 10 kΩ
CRSEN 100 nF
SWR 9
RSWR 365 kΩ
STAB 10
RSTAB 3.65 kΩ
SWT 11
CSWT 220 nF
IDT 12
RIDT 2.2 MΩ
MUTERX 1
MUTETX 15
PD 13
from microcontroller
RXIN 2
CRXIN 100 nF
TXOUT 16
GATX 17
RGATX 30.1 kΩ
CGATX
TXGND 14
GND 6
QR +
MIC −
C7 100 nF
MIC +
C8 100 nF
LN
VCC
R1 620 Ω
SLPE
R9 20 Ω
VEE
C1 100 µF
line
MBG360

Fig.12 Basic application diagram.


tip
ring
interrupter
DP
MICRO-
CONTROLLER
S1
S2
S3
S4 +
MUTET
DTMF
DTMF
R_{DD}
390 Ω
R_{SLPE}
20 Ω
V_{DD}
C_{VDD}
100 µF
SLPE
LN
V_{BB}
TEA1096
MICP
MICM
QRP
QLS
V_{EE}
DLL/
DIL
LSI
S1
C_{DLL}
470
nF
C_{QLS}
47 µF
HFQLS
470 µF
C_{VBB}
R1
100 µF
C_{HSMIC}
R2
100 nF
S3
C_{MICP}
HSMIC
R3
100 nF
C_{MICM}
C1
R4
C_{RXIN}
100 nF
C_{QRP}
10 µF
HSQRP
S2
R5
S4
from
microcontroller
MUTET
MUTETX
MUTERX
PD
15
1
13
TXOUT
16
RXIN
2
TXGND
14
GND
6
TEA1095
7
V_{BB}
18
TXIN
8
VOL
5
RXOUT
R6
C_{HFTXIN}
100 µF
HFTXIN
100
nF
C_{TXIN}
R7
R_{VOL}
100 nF
C_{RXOUT}
MBG361

MODE	SWITCH				MUTET
	S1	S2	S3	S4	
Hands-free	OPEN	OPEN	TXOUT	OPEN	LOW
Handset	CLOSED	CLOSED	HSMIC	OPEN	DON'T CARE
Handset plus listening-in	OPEN	CLOSED	HSMIC	CLOSED	HIGH

Fig.13 Application example.

Speech and listening-in IC TEA1096; TEA1096A

FEATURES

- Line Interface with:
  - active set impedance (adjustable)
  - voltage regulator with adjustable DC voltage
  - low voltage circuit for parallel operation
- Interface to peripheral circuits with:
  - supply V_{DD} for microcontroller
  - stabilized supply voltage (V_{BB}) which is:
    available for peripheral circuits
    adjustable (TEA1096 only)
  - Dual-Tone MultiFrequency (DTMF) signal input
  - power-down function for pulse dialling/flash
  - mute function to disable speech during dialling
- Microphone amplifier with:
  - symmetrical high impedance inputs
  - externally adjustable gain
  - AGC; line-loss compensation
  - dynamic limiter
  - microphone mute function
- Receiving amplifier with:
  - externally adjustable gain
  - confidence tone during dialling
  - double anti-sidetone circuit for long and short lines
  - AGC; line-loss compensation
  - earpiece protection by soft clipping.
- Listening-in circuit with:
  - loudspeaker amplifier
  - dynamic limiter to prevent distortion at any supply condition
  - volume control via a potentiometer
  - fixed gain of 35.5 dB
  - disable function
  - gain control input (TEA1096A only).

APPLICATIONS

- Line-powered telephone sets with listening-in/line monitoring function.

DIFFERENCES BETWEEN TEA1096 AND TEA1096A

The TEA1096 offers via input VBA an adjustable stabilized supply voltage V_{BB}, whereas the TEA1096A offers a fixed stabilized voltage V_{BB}.

The TEA1096A offers a DC gain control input VCI to set the loudspeaker volume, whereas the TEA1096 offers volume control via a potentiometer.

GENERAL DESCRIPTION

The TEA1096 and TEA1096A are bipolar ICs intended for use in line powered telephone sets. They offer a speech/transmission function, listening-in and line monitoring facilities of the received line signal via the loudspeaker.

The devices incorporate a line interface block, a microphone and DTMF amplifier, a receiving amplifier, a supply function, a loudspeaker amplifier, and a dynamic limiter in the transmission channel and the listening-in channel.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1096	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1096A	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TEA1096T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TEA1096AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current	normal condition	15	–	140	mA
		with reduced performance	–	–	15	mA
I_{DD}	current consumption from pin V_{DD} during normal operation	PD = LOW	–	2.4	2.9	mA
$I_{DD(PD)}$	current consumption from capacitor C_{VDD} during power-down	PD = HIGH	–	100	150	μA
$I_{BB(PD)}$	current consumption from capacitor C_{VBB} during power-down	PD = HIGH	–	350	500	μA
V_{SLPE}	stabilized voltage (line interface)		4.2	4.45	4.7	V
V_{DD}	supply voltage for microcontroller	$R_{DD} = 390\ \Omega$; $I_P = 0$ mA	–	3.5	–	V
		$R_{DD} = 390\ \Omega$; $I_P = 1$ mA	–	3.1	–	V
V_{BB}	stabilized supply voltage		3.4	3.6	3.8	V
G_{vtx}	voltage gain from pin MICP or MICM to LN	$V_{MIC} = 2$ mV (RMS); $R_{GAS} = 90.9\ k\Omega$; $I_{line} = 20$ mA	51	52	53	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAS}		–19	–	0	dB
G_{vrx}	voltage gain from pin LN to QRP or QRM	$V_{line} = 50$ mV (RMS); $R_{GAR} = 90.9\ k\Omega$; $I_{line} = 20$ mA	–3.5	–2.5	–1.5	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		–12	–	8	dB
ΔG_{trx}	line-loss compensation	$R_{AGC} = 100\ k\Omega$	5	6	7	dB
G_{vlx}	voltage gain from pin LSI to QLS	$V_{LSI} = 10$ mV (RMS)	34	35.5	37	dB
$V_{LN(p-p)}$	maximum output voltage swing on pin LN (peak-to-peak value)		–	3.65	4.3	V
$V_{QLS(p-p)}$	output voltage between pins QLS and V_{EE} (peak-to-peak value)	$V_{LSI} = 18$ mV; $I_{line} = 20$ mA	2.5	2.9	–	mA
T_{amb}	operating ambient temperature		–25	–	+75	°C

BLOCK DIAGRAMS

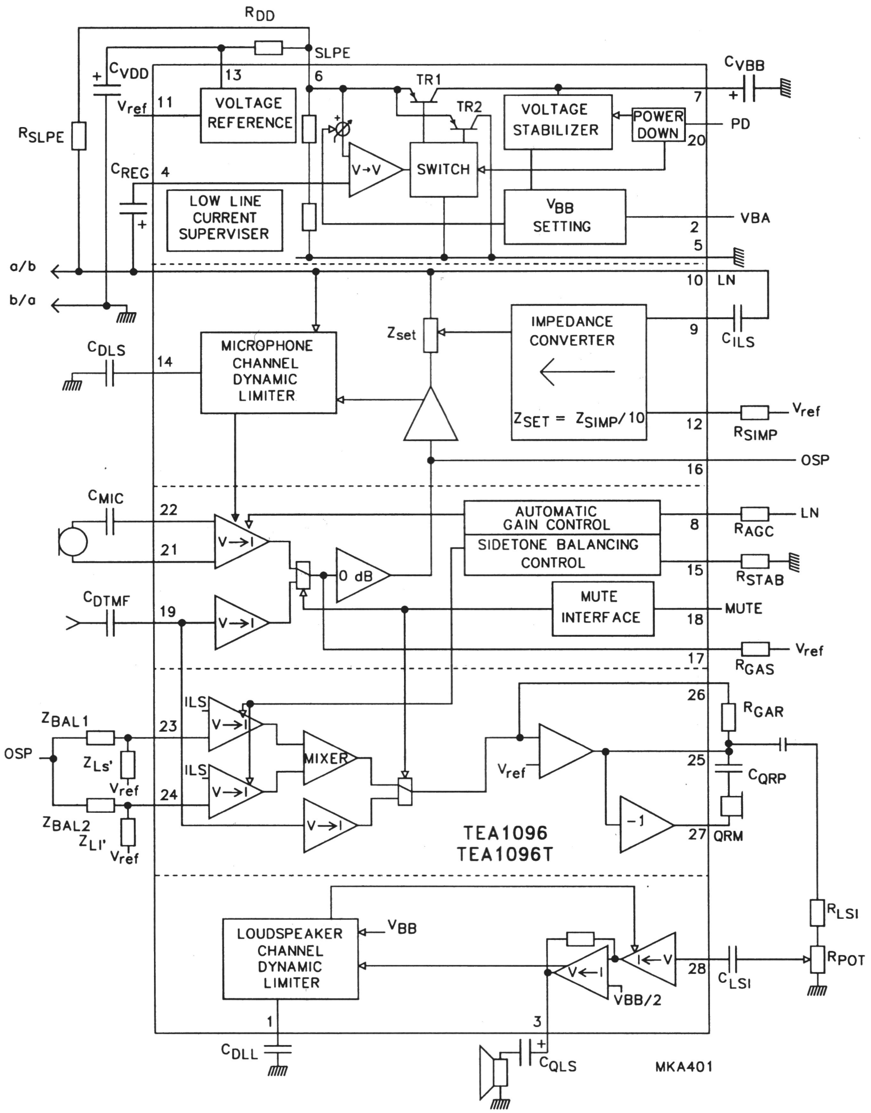

RDD
SLPE
CVDD
13
6
TR1
CVBB
Vref 11
VOLTAGE REFERENCE
TR2
VOLTAGE STABILIZER
7
POWER DOWN
PD
20
RSLPE
CREG 4
V→V
SWITCH
LOW LINE CURRENT SUPERVISER
VBB SETTING
2
VBA
5
a/b
b/a
10 LN
IMPEDANCE CONVERTER
9
CILS
Zset
CDLS
14
MICROPHONE CHANNEL DYNAMIC LIMITER
ZSET = ZSIMP/10
12
Vref
RSIMP
OSP
16
CMIC
22
AUTOMATIC GAIN CONTROL
8
LN
RAGC
21
V→I
SIDETONE BALANCING CONTROL
15
RSTAB
0 dB
CDTMF
19
MUTE INTERFACE
MUTE
18
Vref
RGAS
17
26
RGAR
ZBAL1
ILS
23
OSP
ZLs'
MIXER
Vref
25
CQRP
24
ZBAL2
ZLI'
Vref
−1
27 QRM
TEA1096
TEA1096T
RLSI
LOUDSPEAKER CHANNEL DYNAMIC LIMITER
VBB
I←V
V←I
28
RPOT
CLSI
VBB/2
1
3
CDLL
CQLS
MKA401

Fig.1 Block diagram (TEA1096).

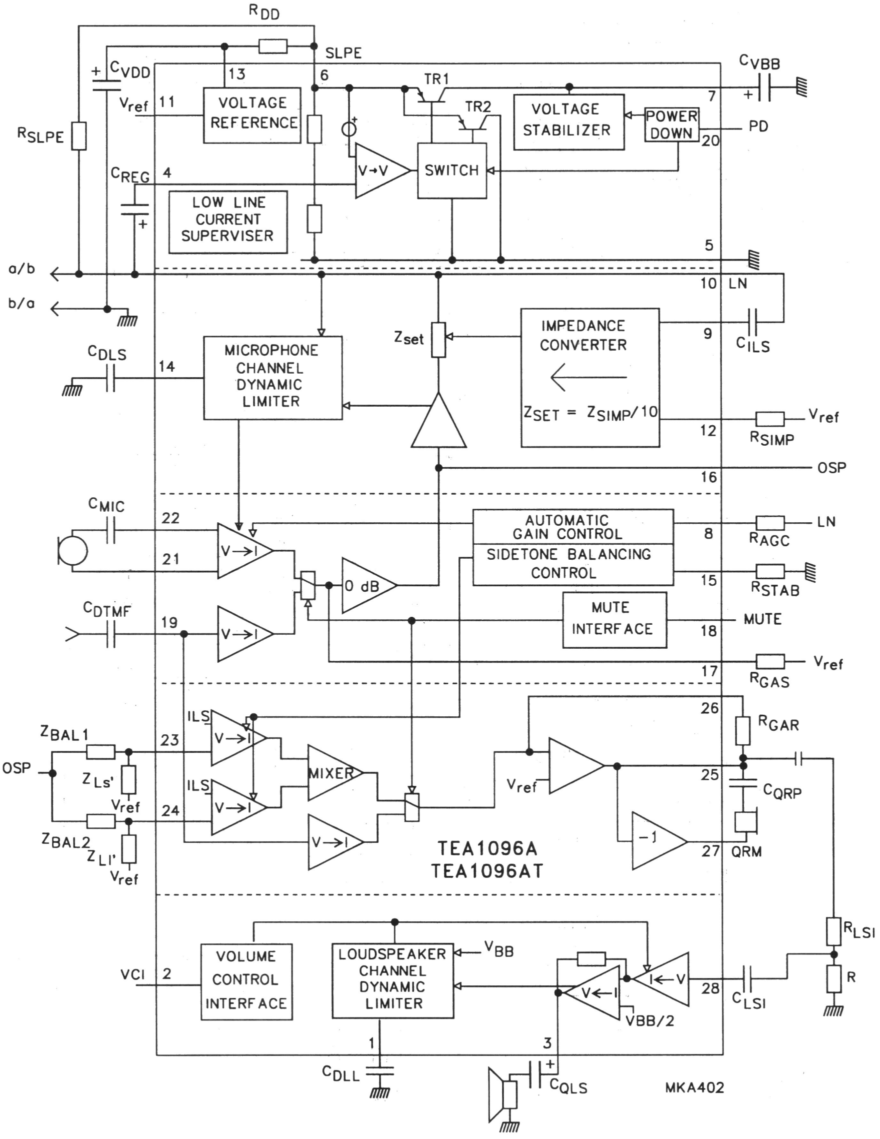

RDD
SLPE
CVDD
13
6
TR1
CVBB
Vref
11
VOLTAGE REFERENCE
TR2
VOLTAGE STABILIZER
7
POWER DOWN
PD
RSLPE
20
CREG
4
V→V
SWITCH
LOW LINE CURRENT SUPERVISER
5
a/b
b/a
10
LN
IMPEDANCE CONVERTER
9
CILS
Zset
CDLS
14
MICROPHONE CHANNEL DYNAMIC LIMITER
ZSET = ZSIMP/10
12
RSIMP
Vref
OSP
16
CMIC
22
AUTOMATIC GAIN CONTROL
8
RAGC
LN
V→I
21
SIDETONE BALANCING CONTROL
15
RSTAB
0 dB
CDTMF
19
V→I
MUTE INTERFACE
18
MUTE
17
RGAS
Vref
26
RGAR
ZBAL1
ILS
23
V→I
OSP
ZLs'
MIXER
Vref
25
CQRP
ILS
24
V→I
Vref
ZBAL2
ZLI'
Vref
V→I
TEA1096A
TEA1096AT
−1
27
QRM
RLSI
VOLUME CONTROL INTERFACE
LOUDSPEAKER CHANNEL DYNAMIC LIMITER
VBB
R
VCI
2
V←I
I←V
28
CLSI
VBB/2
1
3
CDLL
CQLS
MKA402

Fig.2 Block diagram (TEA1096A).

PINNING

SYMBOL	PINS		DESCRIPTION
	TEA1096	TEA1096A	
DLL/DIL	1	1	dynamic limiter and disable input for loudspeaker amplifier
VBA	2	–	V_{BB} voltage adjustment
VCI	–	2	volume control input for loudspeaker amplifier
QLS	3	3	loudspeaker amplifier output
REG	4	4	decoupling line voltage stabilizer
V_{EE}	5	5	negative line terminal (ground reference)
SLPE	6	6	stabilized voltage, connection for slope resistor
V_{BB}	7	7	stabilized supply voltage for listening-in circuitry
AGC	8	8	automatic gain control
ILS	9	9	input line signal
LN	10	10	positive line terminal
V_{ref}	11	11	reference voltage output
SIMP	12	12	set impedance input
V_{DD}	13	13	supply voltage for speech circuitry/peripherals
DLS/$\overline{\text{MMUTE}}$	14	14	dynamic limiter for sending and microphone mute
STAB	15	15	reference current adjustment
OSP	16	16	sending preamplifier output
GAS	17	17	sending gain adjustment
MUTE	18	18	mute input to select speech or DTMF dialling
DTMF	19	19	dual-tone multi-frequency (DTMF) input
PD	20	20	power-down input
MICM	21	21	inverting microphone amplifier input
MICP	22	22	non-inverting microphone amplifier input
BAL1	23	23	connection for balance network 1
BAL2	24	24	connection for balance network 2
QRP	25	25	non-inverting receiving amplifier output
GAR	26	26	receiving gain adjustment
QRM	27	27	inverting receiving amplifier output
LSI	28	28	loudspeaker amplifier input

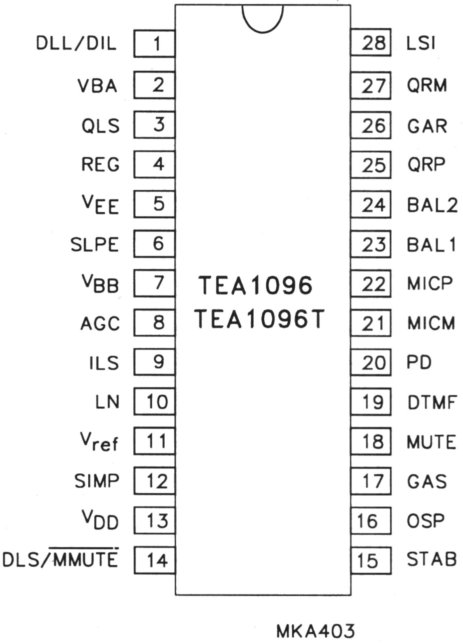

TEA1096
TEA1096T
DLL/DIL 1
VBA 2
QLS 3
REG 4
V_{EE} 5
SLPE 6
V_{BB} 7
AGC 8
ILS 9
LN 10
V_{ref} 11
SIMP 12
V_{DD} 13
DLS/$\overline{MMUTE}$ 14
28 LSI
27 QRM
26 GAR
25 QRP
24 BAL2
23 BAL1
22 MICP
21 MICM
20 PD
19 DTMF
18 MUTE
17 GAS
16 OSP
15 STAB
MKA403

Fig.3 Pin configuration (TEA1096).

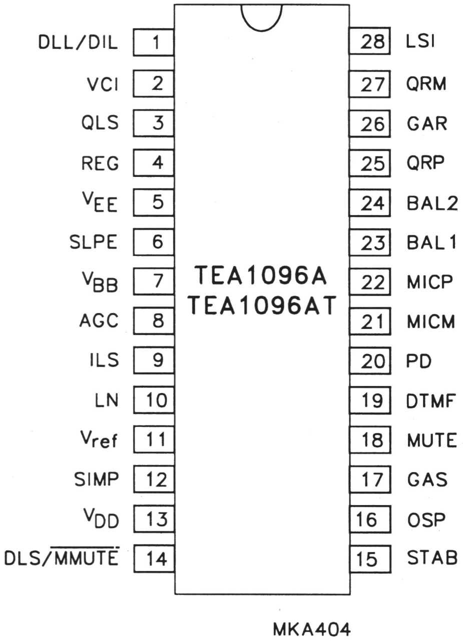

TEA1096A
TEA1096AT
DLL/DIL 1
VCI 2
QLS 3
REG 4
V_{EE} 5
SLPE 6
V_{BB} 7
AGC 8
ILS 9
LN 10
V_{ref} 11
SIMP 12
V_{DD} 13
DLS/$\overline{MMUTE}$ 14
28 LSI
27 QRM
26 GAR
25 QRP
24 BAL2
23 BAL1
22 MICP
21 MICM
20 PD
19 DTMF
18 MUTE
17 GAS
16 OSP
15 STAB
MKA404

Fig.4 Pin configuration (TEA1096A).

FUNCTIONAL DESCRIPTION

Remark: all data given in this chapter are typical values except when otherwise specified.

Supply pins SLPE, LN, V_{EE}, V_{BB}, V_{DD}, REG and PD

The supply for the TEA1096/TEA1096A and its peripherals is obtained from the telephone line. The circuits regulate the line voltage and generate their own supply voltages V_{DD} and V_{BB} to power the transmission part and the loudspeaker amplifier respectively.

As can be seen from Fig.5, the line current (I_{line}) is split between the sending output stage (I_{ln}), the circuitry connected to SLPE (I_{sl}), the transmission circuit (I_{DD}), the peripheral circuits (I_p) and the current switch (I_{SUP}). It can be shown that:

$$I_{SUP} = I_{line} - (I_{ln} + I_{sl} + I_{DD} + I_P)$$

With nominal conditions where:

$I_{ln} = 5$ mA, $I_{sl} = 0.3$ mA and $I_{DD} = 2.4$ mA

it therefore follows that $I_{SUP} \approx I_{line} - 7.7\text{ mA} - I_P$.

The remaining current I_{SUP} is available for the listening-in part. The current consumption I_{BB0} of the listening-in circuitry is 2.5 mA. To power the loudspeaker, the line current has to be more than 10 mA.

The voltage at SLPE is stabilized at 4.45 V nominal. The DC line voltage is regulated at:
$V_{LN} = V_{SLPE} + R_{SLPE} \times (I_{line} - I_{ln})$.

The supply voltage for the transmission part and peripheral circuits (V_{DD}) is generated from V_{SLPE} and is equal to $V_{DD} = V_{SLPE} - R_{DD} \times (I_{DD} + I_p)$.

V_{BB} supplies the listening-in circuitry and is stabilized at 3.6 V nominal.

A resistor connected between pin REG and V_{EE} can be used to decrease the SLPE voltage while maintaining V_{BB} at its nominal value, whereas a resistor connected between pin REG and pin SLPE will increase the SLPE voltage while maintaining V_{BB} at its nominal value. When adjusting the SLPE voltage to a lower value, care should be taken that the V_{SLPE} is at least 0.4 V higher than V_{BB} (V_{BB} supply efficiency).

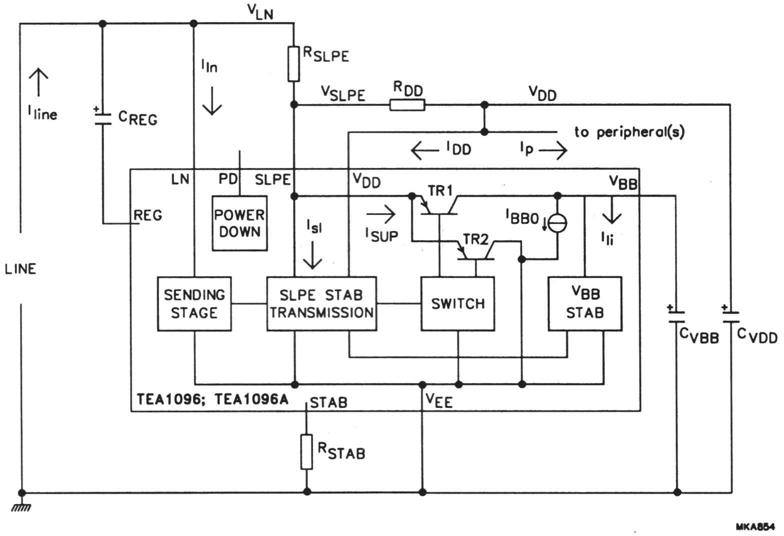

VLN
Iline
CREG
Iln
RSLPE
VSLPE
RDD
VDD
to peripheral(s)
IDD
Ip
LN
PD
SLPE
VDD
VBB
TR1
REG
POWER DOWN
Isl
ISUP
IBB0
Ili
TR2
LINE
SENDING STAGE
SLPE STAB TRANSMISSION
SWITCH
VBB STAB
CVBB
CVDD
TEA1096; TEA1096A
STAB
VEE
RSTAB
MKA854

Fig.5 Supply arrangement.

The function of the current switch TR1-TR2 is to reduce distortion of large line signals. Current I_{SUP} is supplied to V_{BB} via TR1, when V_{SLPE} is higher than V_{BB} + 0.4 V. When V_{SLPE} is lower, this current is shunted to V_{EE} via TR2. All excess line current, not used for internal supply is consumed in the V_{BB} stabilizer or directly shunted to V_{EE}.

To reduce the current consumption during pulse dialling, the TEA1096/TEA1096A are provided with a power-down (PD) input. The PD input has a pull-down structure. When the voltage on PD is HIGH, the current consumption from V_{DD} capacitor C_{VDD} is 100 μA and from the V_{BB} supply point 350 μA. The capacitors C_{VDD} (100 μF) and C_{VBB} (470 μF) are sufficient to power theTEA1096/TEA1096A during pulse dialling/flash.

V_{BB} voltage adjustment: pin VBA (TEA1096 only)

A resistor connected between pins VBA and V_{EE} can be used to increase the V_{BB} voltage, whereas a resistor connected between pins VBA and V_{BB} will decrease the V_{BB} voltage. When adjusting the V_{BB} voltage to a higher value, care should be taken that V_{SLPE} is at least 0.4 V higher than V_{BB} (V_{BB} supply efficiency).

Sending channel: pins MICP, MICM, DTMF, GAS, OSP, LN, MUTE, DLS and AGC

The TEA1096/TEA1096A has symmetrical microphone inputs MICP, MICM with an input resistance of 64 kΩ between MICP and MICM (2 × 32 kΩ). In the speech mode (MUTE = LOW), the overall gain from MICP-MICM to LN can be adjusted from 33 dB to 52 dB to suit specific requirements. The gain is proportional to the value of R_{GAS} and equals 52 dB with R_{GAS} = 90.9 kΩ and I_{line} = 20 mA. A capacitor C_{GAS} connected in parallel with R_{GAS} can be used to provide a first-order low-pass filter.

Automatic gain control (AGC) is provided for line-loss compensation as well as dynamic limitation for reduction of the distortion of the transmitted signal on the line. The microphone amplifier can be disabled by short-circuiting pin DLS to V_{EE} (secret function) and can be muted into DTMF mode by applying a HIGH level on pin MUTE.

The TEA1096/TEA1096A has an asymmetrical DTMF input with an input resistance of 20 kΩ. In the DTMF mode, the overall gain from DTMF to LN is proportional to R_{GAS}, and is 26.5 dB less than the microphone amplifier gain. Switch-over from one mode to the other is click-free.

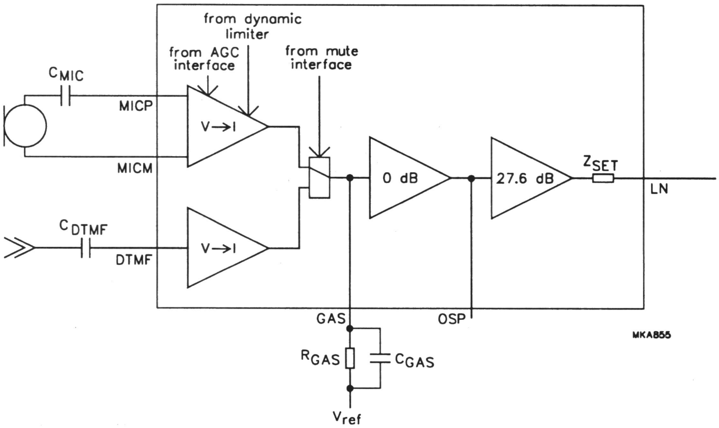


Fig.6 Sending channel.

It can be calculated from Fig.7 that the AC modulator gain can be written:

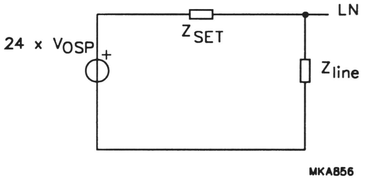
- $\frac{V_{LN}}{V_{OSP}} = \frac{Z_{line}}{(Z_{line} + Z_{SET}) \times 24} = 12$ providing $Z_{SET} = Z_{line}$
- G_v (LN to OSP) = 21.6 dB.

The frequency response for audio frequencies of the sending channel is flat in this case for a complex line termination.

Set impedance: pins ILS, SIMP and LN

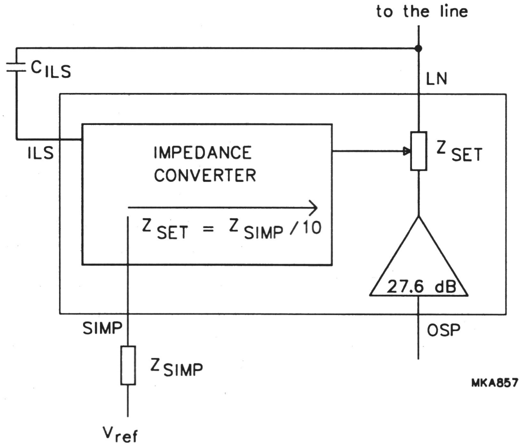
The TEA1096/TEA1096A provides an active set impedance in both the receiving and sending conditions, thus allowing a flat frequency response for a complex line impedance, without the need for any extra compensation network.

As can be derived from Fig.8 the set impedance Z_{SET} is 10 times lower than Z_{SIMP}.



24 x V_{OSP}
+
Z_{SET}
LN
Z_{line}
MKA856

Fig.7 AC modulator equivalent model.



to the line
C_{ILS}
LN
ILS
IMPEDANCE CONVERTER
$Z_{SET} = Z_{SIMP}/10$
Z_{SET}
27.6 dB
SIMP
OSP
Z_{SIMP}
V_{ref}
MKA857

Fig.8 Set impedance.

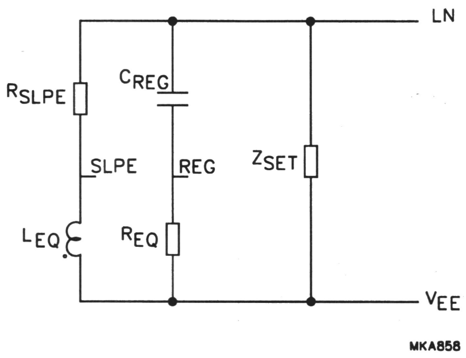


Fig.9 Equivalent AC impedance between LN and V_{EE}.

The equivalent impedance connected between LN and V_{EE} is illustrated in Fig.9.

Where:

- $L_{EQ} = R_{EQ} \times C_{REG} \times R_{SLPE}$
- $R_{EQ} = 40\ k\Omega$
- $Z_{SET} = \frac{1}{10} Z_{SIMP}$.

Remark: a resistor R (REG-V_{EE}) connected between REG and V_{EE} (to lower the regulated voltage) changes R_{EQ} into R_{EQ} // R (REG-V_{EE}), whereas a resistor $R_{REG\text{-}SLPE}$ connected between REG and SLPE (to increase the regulated voltage) has no effect on R_{EQ}.

Dynamic limiter of the microphone channel: pin DLS

The dynamic limiter in the microphone channel of the TEA1096/TEA1096A prevents clipping of the microphone signal, and limits the transmitted signal on LN to a maximum value of typically 3.65 V (4.4 dBm).

Clipping on the microphone channel is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which the gain reduction is effected (clipping attack time) is approximately a few milliseconds. The microphone channel stays in the reduced gain mode until the peaks of the signal no longer cause saturation. The gain of the microphone channel then returns to its normal value within the clipping release time.

Both attack and release time are proportional to the value of the capacitor C_{DLS}. The THD (Total Harmonic Distortion) of the microphone amplifier in the reduced gain mode stays below 2% up to 10 dB of input voltage overdrive [provided that V_{MICP}, V_{MICM} is below 10 mV (RMS)].

The dynamic limiter of the TEA1096/TEA1096A also provides a microphone mute (secret function) when pin DLS is short-circuited to V_{EE}. The microphone gain is then 80 dB lower. The release time after a microphone mute is approximately 10 ms.

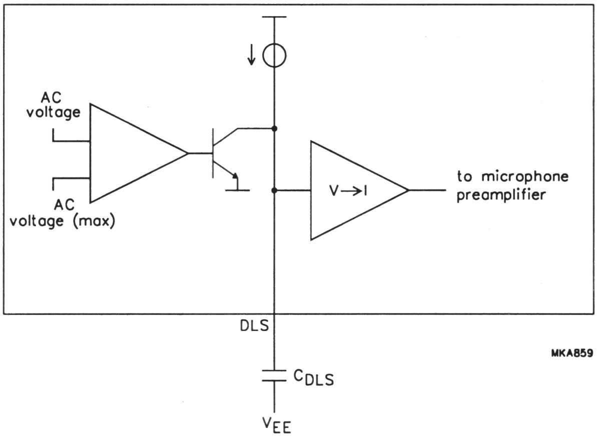


Fig.10 Dynamic limiter of the microphone channel.

Receiving amplifier: pins LN, GAR, QRP and QRM

The receiver gain is defined between the line connection LN and the earpiece complementary outputs QRP (non-inverting) and QRM (inverting). With R_{GAR} equal to 90.9 kΩ the gain from LN to QRP is –2.5 dB. The outputs may be used to connect a dynamic, magnetic or piezoelectric earpiece. When the earpiece impedance exceeds 450 Ω, differential drive (BTL connection) can be used. As both outputs are in opposite phase, the gain from LN to QRP or QRM is 3.5 dB.

By means of the R_{GAR} resistor, the gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer which is used. The permitted range is between –14 dB and +6 dB for single-ended drive (SE), and between –8 dB and +12 dB for bridge-tied load (BTL) drive.

Two external capacitors, C_{GAR} (100 pF) and C_{GARS} (1 nF), ensure stability. The C_{GAR} capacitor is also used to obtain a first-order low-pass filter. The cut-off frequency (corresponding to the time constant $R_{GAR} \times C_{GAR}$) can be adjusted by the C_{GAR} capacitor, but the relationship $C_{GARS} = C_{GAR} \times 10$ must be maintained.

During DTMF dialling, the dialling tones can be heard in the earpiece at a very low level. This is called confidence tone.

Automatic gain control: pin AGC

Automatic compensation of line-loss is obtained by connecting a resistor R_{AGC} between pin LN and pin AGC. This automatic gain control changes the gain of the microphone and receiving amplifiers in accordance with the DC line current.

The control range is 6 dB; This corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable:

DC resistance = 176 Ω /km

average attenuation = 1.2 dB/km.

The value of R_{AGC} must be chosen with reference to the exchange supply voltage and its feeding bridge resistance and has no influence on the ratio (I_{start}/I_{stop}) which remains constant. Figure11 illustrates the gain attenuation when R_{AGC} = 100 kΩ. If automatic line-loss compensation is not required, the AGC pin can be left open circuit, the amplifiers then give their maximum gain and the double sidetone principle is no longer active. Only one network is used. Pins BAL1 and BAL2 must then be short-circuited together.

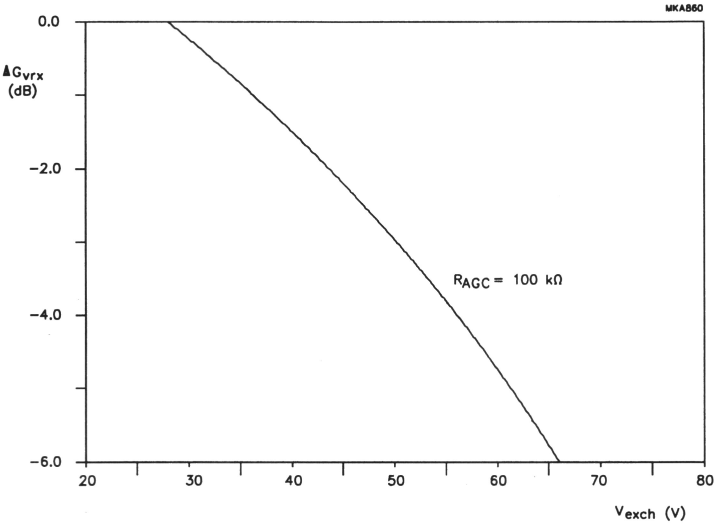


Fig.11 Variation of microphone and receiver gain as a function of the exchange supply voltage with R_{AGC} as a parameter.

Sidetone suppression: pins BAL1, BAL2, OSP and ILS

Suppression of the microphone signal in the earpiece is obtained by subtracting a part of this signal to a fraction of the line signal (see Fig.12). For optimum suppression, the voltage at the BAL inputs (BAL1 and BAL2) should be equal to:

$$V_{BAL} = 0.5 \times \frac{Z_{line}}{Z_{SET} \times Z_{line}} \times V_{SOP}$$

To reach this requirement, an anti-sidetone network using two impedances Z_{BAL} and $Z_{LI'}$ is needed.

In the event of real impedances, the anti-sidetone network is composed of resistors connected as shown in Fig.13.

Where: $R_{LI'} = \alpha \times R_{line}$ and $R_{BAL} = \alpha \times R_{SET}$;

where α is a scale factor allowing to have $R_{LI'}$ in the order of 10 kΩ (DC biasing to V_{ref} has to be ensured on BAL1 and BAL2).

In the event of complex impedances, the equivalent network Z_s, representing Z_{line}, has to be transformed into Z_p in accordance with Fig.14.

The components of Z_p, scaled by a factor α, are applied in anti-sidetone network $Z_{LI'}$. The complete anti-sidetone network is shown in Fig.15.

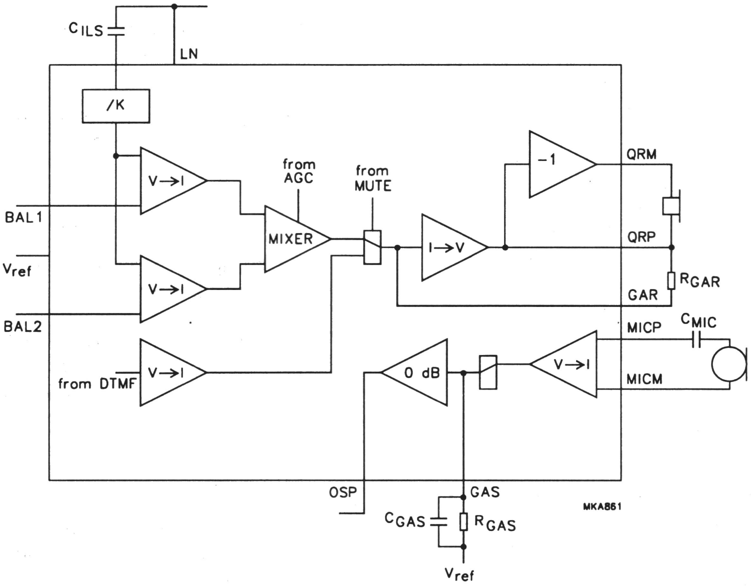

C_ILS
LN
/K
V→I
BAL1
Vref
BAL2
V→I
from DTMF
V→I
from AGC
MIXER
from MUTE
I→V
−1
QRM
QRP
R_GAR
GAR
MICP
C_MIC
MICM
0 dB
V→I
OSP
GAS
C_GAS
R_GAS
Vref
MKA861

Fig.12 Balance networks connection.

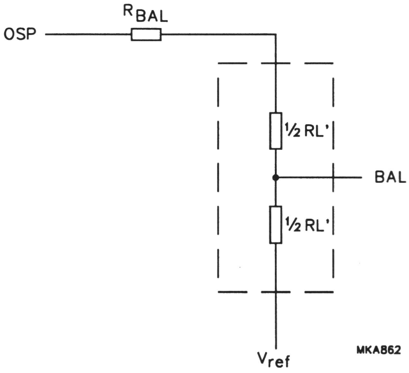
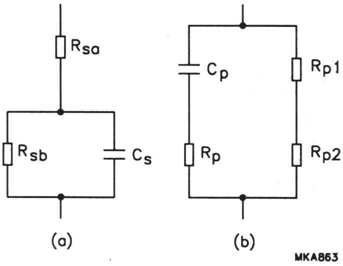

OSP
R_BAL
½RL'
BAL
½RL'
Vref
MKA862

Fig.13 Anti-sidetone network.


Rsa
Rsb
Cs
(a)
Cp
Rp1
Rp
Rp2
(b)
MKA863

(a) Series impedance (Z_s).

(b) Parallel impedance (Z_p).

Fig.14 Equivalent network.

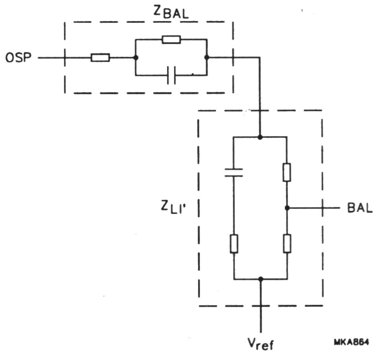


Fig.15 Complete anti-sidetone network.

Again, it means that: $Z_{Ll'} = \alpha \times Z_{line}$ and $Z_{BAL} = \alpha \times Z_{SET}$

Where α is a scale factor allowing $Z_{Ll'}$ to be in the order of 10 kΩ (DC biasing to V_{ref} has to be ensured on BAL1 and BAL2).

As the line impedance Z_{line} varies considerably with the line length, two anti-sidetone networks can be used. One of them $Z_{Ll'}$, connected to BAL2 is optimized for long lines, the other one $Z_{Ls'}$, connected to BAL1 is optimized for short lines:

Where:

$Z_{Ll'} = \alpha \times Z_{line}$ (long)

$Z_{Ls'} = \alpha \times Z_{line}$ (short)

$Z_{BAL1} = \alpha \times Z_{SET}$

$Z_{BAL2} = \alpha \times Z_{SET}$.

Switching from one network to the other is carried out continuously with the line current, when the R_{AGC} resistor is connected. When the R_{AGC} resistor is not connected, switching from one network to the other is not possible (see automatic gain control). Only one network has then to be applied.

It is also possible to use only one anti-sidetone network. In this event, both inputs BAL1 and BAL2 must be short-circuited.

Loudspeaker amplifier: pins LSI and QLS

The loudspeaker amplifier has an asymmetrical input LSI which is referenced to an internal voltage reference of 1.25 V via an internal resistance of 10 kΩ. The input signal can be taken from one of the earpiece outputs QRP or QRM via a potentiometer (R_{POT}). The attenuation has to be chosen in accordance with the gain G_{vrx} of the receiving amplifier.

The input stage can handle up to 200 mV (RMS) at room temperature for 3% of THD.

The gain of the loudspeaker amplifier is fixed at 35.5 dB. The output QLS is referenced to a DC level of $\frac{1}{2}V_{BB}$ to offer rail-to-rail output swing.

The maximum voltage gain from line to loudspeaker has to be fixed in relation to the side-tone transfer of the telephone set. An enlarged listening-in gain improves the listening-in behaviour but can introduce audible instabilities in the form of howling during normal use of the set. The loudspeaker can be disabled by short-circuiting DLL/DIL input to V_{EE}.

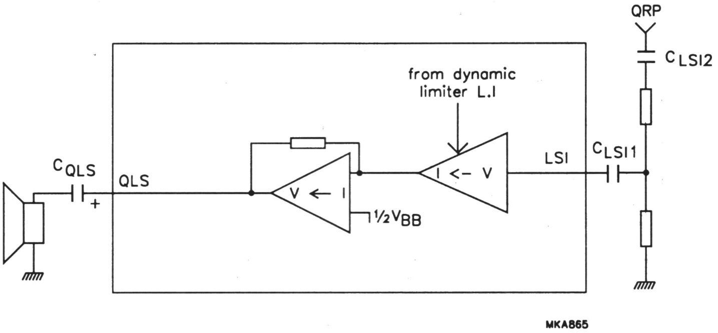


Fig.16 Loudspeaker amplifier channel.

Dynamic limiter/loudspeaker amplifier disabling; pin DLL/DIL

The dynamic limiter in the loudspeaker channel of the TEA1096/TEA1096A prevents clipping of the loudspeaker output stage and protects the functioning of the circuit when low supply conditions are detected.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which the gain reduction is effected (clipping attack time) is approximately a few milliseconds. The loudspeaker amplifier stays in the reduced gain mode until the peaks of the loudspeaker signals no longer start to cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time. Both attack and release time are proportional to the value of the capacitor C_{DLL}. The THD of the loudspeaker amplifier in the reduced gain mode stays below 5% up to 10 dB of input voltage overdrive.

When the supply conditions drop below the required level, the gain of the loudspeaker amplifier is reduced in order to prevent the device from malfunctioning. When the supply current drops below the required level, the supply voltage V_{BB} decreases. In this condition, the gain of the loudspeaker amplifier is reduced slowly (approximately a few seconds). When the supply voltage continues to decrease and drops below an internal threshold of 2.8 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). After returning to normal supply conditions, the gain of the loudspeaker amplifier is raised again.

The dynamic limiter also provides a loudspeaker disable when pin DLL/DIL is short-circuited to V_{EE}. The loudspeaker gain is then typically 80 dB lower. The release time is approximately 10 ms.

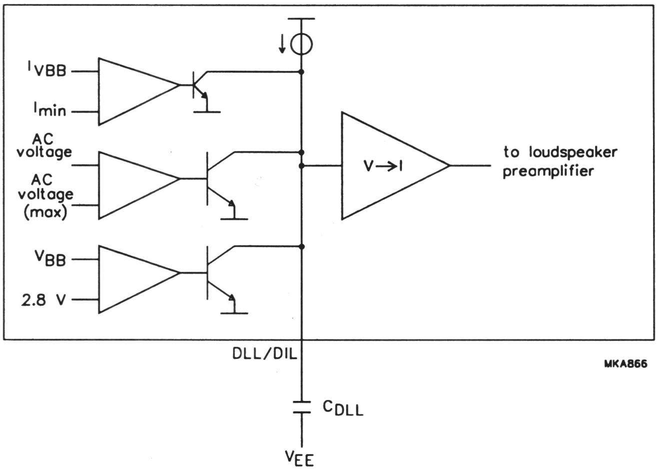

I_VBB
I_min
AC voltage
AC voltage (max)
V_BB
2.8 V
V→I
to loudspeaker preamplifier
DLL/DIL
C_DLL
V_EE
MKA866

Fig.17 Dynamic limiter of the listening-in part.

Volume control: pin VCI (TEA1096A only)

The TEA1096A is provided with a volume control input VCI, to adjust the gain of the loudspeaker channel by means of a controlled DC voltage. A typical application is illustrated in Fig.18. A pulse width modulation on a microcontroller open drain output imposes a DC voltage on the VCI capacitor:

Where $V_{VCI} = \frac{\delta \times K \times V_{BB}}{1 - \delta \times (1 - K)}$

with δ = duty cycle and $K = \frac{R1}{R1 + R2}$

A typical response is given in Fig.19.

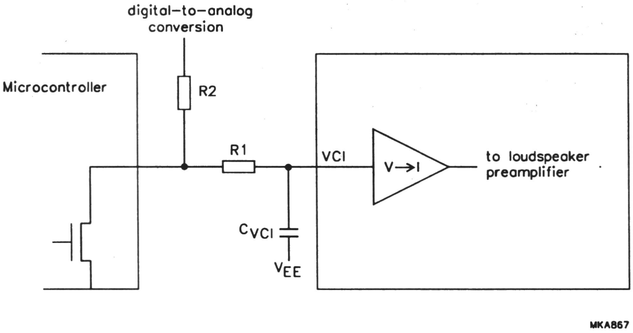

digital-to-analog conversion
Microcontroller
R2
R1
VCI
V→I
to loudspeaker preamplifier
C_VCI
V_EE
MKA867

Fig.18 Digital volume control application.

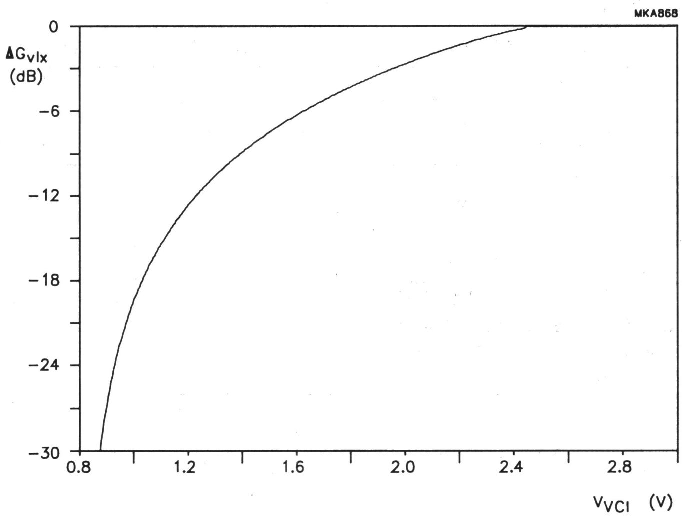


Fig.19 Change of loudspeaker gain as a function of the voltage at VCI.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

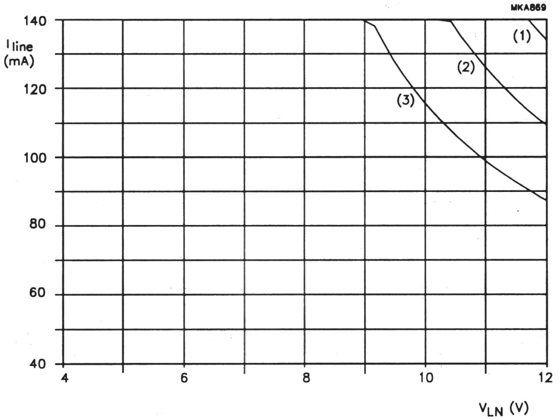
SYMBOLS	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	voltage on pin LN		$V_{EE} - 0.4$	12.0	V
V_{DD}	voltage on pin VDD		$V_{EE} - 0.4$	12.0	V
V_{BB}	voltage on pin VBB		$V_{EE} - 0.4$	12.0	V
V_{n1}	voltage on pins: REG, SLPE, AGC and ILS		$V_{EE} - 0.4$	$V_{LN} + 0.4$	V
V_{n2}	voltage on pins: DLL, VBA or VCI, QLS, LSI		$V_{EE} - 0.4$	$V_{BB} + 0.4$	V
V_{n3}	voltage on pins: V_{ref}, SIMP, STAB, DLS, OSP, GAS, MUTE, DTMF, PD, MICM, MICP, BAL1, BAL2, QRP, QRM, GAR		$V_{EE} - 0.4$	$V_{DD} + 0.4$	V
I_{line}	line current	see also Figs 20 and 21	–	140	mA
P_{tot}	total power dissipation:	T_{amb} = +75 °C; see Figs 20 and 21			
	TEA1096/TEA1096A		–	0.91	W
	TEA1096T/TEA1096AT		–	0.66	W
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOLS	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air:		
	TEA1096; TEA1096A	55	K/W
	TEA1096T; TEA1096AT (note 1)	75	K/W

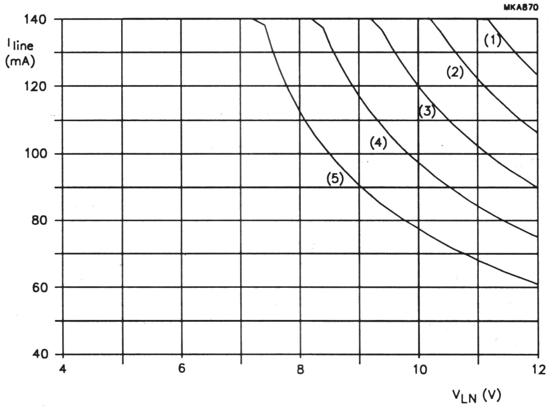
Note

1. Mounted on epoxy board 40.1 × 19.1 × 1.5 mm.



(1) T_{amb} = 55 °C; P_{tot} = 1272 mW.
(2) T_{amb} = 65 °C; P_{tot} = 1091 mW.
(3) T_{amb} = 75 °C; P_{tot} = 910 mW.

Fig.20 TEA1096; TEA1096A safe operating area.



(1) T_{amb} = 35 °C; P_{tot} = 1199 mW.
(2) T_{amb} = 45 °C; P_{tot} = 1066 mW.
(3) T_{amb} = 55 °C; P_{tot} = 933 mW.
(4) T_{amb} = 65 °C; P_{tot} = 800 mW.
(5) T_{amb} = 75 °C; P_{tot} = 667 mW.

Fig.21 TEA1096T; TEA1096AT safe operating area.

CHARACTERISTICS

I_{line} = 20 mA; I_P = 0 mA; V_{EE} = 0 V; PD = LOW; MUTE = LOW; Z_{line} = 600 Ω; Z_{SIMP} = 6 kΩ; Z_{BAL1} = 18 kΩ; $Z_{LI'}$ = 6 kΩ; R_{SLPE} = 20 Ω; R_{DD} = 390 Ω; R_{GAS} = 90.9 kΩ; R_{GAR} = 0.9 kΩ; R_{QLS} = 50 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig.22; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line interface/supply (LN, SLPE, REG, V_{EE}, V_{DD}, V_{BB} and V_{ref})						
V_{SLPE}	stabilized voltage (line interface)		4.2	4.45	4.7	V
$\Delta V_{SLPE(Iline)}$	V_{SLPE} variation with I_{line}	I_{line} = 20 to 140 mA	–	30	–	mV
$\Delta V_{SLPE(T)}$	V_{SLPE} variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–150	±60	+150	mV
V_{BB}	stabilized supply voltage		3.4	3.6	3.8	V
$\Delta V_{BB(Iline)}$	V_{BB} variation with I_{line}	I_{line} = 20 to 140 mA	–	30	–	mV
$\Delta V_{BB(T)}$	V_{BB} variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–150	±50	+150	mV
I_{sink}	current sunk by V_{BB} shunt regulator when a line current equal to 20 mA is available	I_P = 0 mA; note 1	–	9.0	–	mA
I_{DD}	internal current consumption from pin V_{DD}	I_P = 0 mA; R_{DD} = 390 Ω	–	2.4	2.9	mA
V_{DD}	supply voltage for speech and microcontroller	R_{DD} = 390 Ω; I_P = 0 mA	–	3.5	–	V
		R_{DD} = 390 Ω; I_P = 1 mA	–	3.1	–	V
V_{ref}	reference output voltage		–	$0.5V_{DD}$	–	V
$I_{DD(PD)}$	current consumption from C_{VDD} during power-down condition	PD = HIGH; V_{DD} = 4.3 V	–	100	150	μA
$I_{BB(PD)}$	current consumption from C_{VBB} during power-down condition	PD = HIGH; V_{BB} = 3.5 V	–	350	500	μA
V_{LN}	DC line voltage		4.4	4.7	5.0	V
V_{LN}	DC line voltage in low current conditions	R_{DD} = 390 Ω; I_P = 0 mA; I_{line} = 4 mA	–	2.5	–	V
		R_{DD} = 390 Ω; I_P = 0 mA; I_{line} = 6 mA	–	3.3	–	V
Microphone amplifier (MICP, MICM, GAS, LN, and MUTE)						
$\lvert Z_{i1} \rvert$	input impedance between pins MICP or MICM and V_{EE}		25.5	32	38.5	kΩ
$\lvert Z_{i2} \rvert$	input impedance between pins MICP and MICM		51	64	77	kΩ
G_{vtx}	voltage gain from pin MICP or MICM to LN	V_{MIC} = 2 mV (RMS); R_{GAS} = 90.9 kΩ	51	52	53	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C.	V_{MIC} = 2 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.5	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{MIC} = 2 mV (RMS); f = 300 to 3400 Hz	–	±0.5	–	dB
ΔG_{vtxr}	voltage gain adjustment with R_{GAS}	note 2	–19	–	0	dB
ΔG_{txm}	gain reduction with MUTE = HIGH		60	80	–	dB
ΔG_{txd}	gain reduction when DLS/$\overline{\text{MMUTE}}$ is short-circuited to V_{EE}		60	80	–	dB
$V_{LN(p-p)}$	maximum output voltage swing at pin LN (peak-to-peak value)	R_{GAS} = 90.9 kΩ	–	3.65	4.3	V
V_{notx}	noise output voltage at pin LN	pins MICP and MICM short-circuited through 200 Ω; Psophometrically weighted (P53 curve)	–	–72	–	dBmp
CMRR	common mode rejection ratio		–	80	–	dB
Dynamic limiter for sending (DLS/$\overline{\text{MMUTE}}$); related to the microphone amplifier clipping detector						
t_{att}	attack time when V_{MIC} jumps from 3.2 mV to 3.2 mV + 10 dB	R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	–	1.5	5	ms
t_{rel}	release time when V_{MIC} drops from 3.2 mV + 10 dB to 3.2 mV	R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	40	120	–	ms
THD	total harmonic distortion	V_{MIC} = 3.2 mV + 10 dB; R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	–	2	3	%
		V_{MIC} = 3.2 mV + 15 dB; R_{GAS} = 90.9 kΩ; C_{DLS} = 470 nF	–	3	10	%
Receiving amplifier (ILS, BAL1, BAL2, OSP, GAR, QRP, QRM and MUTE)						
G_{vrx}	voltage gain from pin LN to QRP or QRM	R_{GAR} = 90.9 kΩ; V_{line} = 50 mV (RMS); single-ended load; R_{QRP} = 150 Ω	–3.5	–2.5	–1.5	dB
		R_{GAR} = 90.9 kΩ; V_{line} = 50 mV (RMS); bridge tied load; R_{QRM} = 450 Ω	2.5	3.5	4.5	dB
ΔG_{vrxT}	voltage gain variation with temperature referenced to 25 °C.	T_{amb} = –25 to +75 °C	–	±0.5	–	dB
ΔG_{vrxf}	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.5	–	dB
ΔG_{vrxr}	voltage gain adjustment with R_{GAR}		–12	–	8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{QR(rms)}$	maximum output voltage for THD = 2% (RMS value)	R_{GAR} = 90.9 kΩ; single-ended load; R_{QRP} = 150 Ω	0.3	0.375	–	V
		R_{GAR} = 90.9 kΩ; bridge-tied load; R_{QRM} = 450 Ω	0.6	0.72	–	V
		R_{GAR} = 90.9 kΩ; bridge-tied load with 300 Ω series resistor; C_{QRM} = 60 nF; f = 3400 Hz	0.75	0.95	–	V
$V_{norx(rms)}$	noise output voltage (RMS value)	Psophometrically weighted (P53 curve); single-ended load; R_{QRP} = 150 Ω	–	90	–	µV
		Psophometrically weighted (P53 curve); bridge-tied load; R_{QRM} = 450 Ω	–	180	–	µV
DTMF amplifier (DTMF, LN, MUTE)						
$\lvert Z_i \rvert$	input impedance between pins DTMF and V_{EE}		16	20	24	kΩ
G_{vtx}	voltage gain from pin DTMF to LN	V_{DTMF} = 4 mV (RMS); R_{GAS} = 90.9 kΩ	24.5	25.5	26.5	dB
ΔG_{vtxT}	voltage gain variation with temperature referenced to 25 °C	V_{DTMF} = 4 mV (RMS); T_{amb} = –25 to +75 °C	–	±0.5	–	dB
ΔG_{vtxf}	voltage gain variation with frequency referenced to 1 kHz	V_{DTMF} = 4 mV (RMS); f = 300 to 3400 Hz	–	±0.5	–	dB
G_{vtx}	voltage gain from pin DTMF to QRP	MUTE = HIGH; V_{line} = 80 mV (RMS); R_{GAR} = 90.9 kΩ; R_{QRP} = 150 Ω	–	–19	–	dB
Automatic gain control (AGC); controlling the gain from LN to QRP, QRM and the gain from MICP, MICM to LN						
ΔG_{trx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 20 mA	I_{line} = 85 mA; R_{AGC} = 100 kΩ	5	6	7	dB
$I_{line(h)}$	highest line current for maximum gain	R_{AGC} = 100 kΩ	–	28	–	mA
$I_{line(l)}$	lowest line current for minimum gain	R_{AGC} = 100 kΩ	–	66	–	mA
ΔG_{trx}	change of gain when varying I_{line} from 20 mA to 40 mA	R_{AGC} = 100 kΩ	1	1.5	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loudspeaker amplifier (LSI and QLS)						
$\|Z_i\|$	input impedance between pins LSI and V_{EE}		8	10	12	kΩ
G_{vlx}	voltage gain from pin LSI to QLS	V_{LSI} = 10 mV (RMS)	34	35.5	37	dB
ΔG_{vlxT}	voltage gain variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±0.5	–	dB
ΔG_{vlxf}	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.5	–	dB
$V_{QLS(p-p)}$	output voltage between pins QLS and V_{EE} (peak-to-peak value)	V_{LSI} = 18 mV; I_{line} = 16 mA	1.2	1.45	–	V
		V_{LSI} = 18 mV; I_{line} = 20 mA	2.5	2.9	–	V
$V_{nolx(rms)}$	noise output voltage at pin LN (RMS value)	pin LSI open-circuit; Psophometrically weighted (P53 curve)	–	200	–	μV
Dynamic limiter for the loudspeaker amplifier (DLL/DIL); related to the loudspeaker amplifier clipping detector						
THD	total harmonic distortion	V_{LSI} = 18 mV + 0 dB; I_{line} = 30 mA	–	2	5	%
t_{att}	attack time when V_{LSI} jumps from 18 mV to 18 mV + 0 dB	I_{line} = 30 mA; C_{DLL} = 470 nF	–	1.5	5	ms
t_{rel}	release time when V_{LSI} drops from 18 mV + 0 dB to 18 mV	I_{line} = 30 mA; C_{DLL} = 470 nF	30	60	–	ms
Dynamic limiter for the loudspeaker amplifier (DLL/DIL); related to the V_{BB} threshold detector						
$V_{BB(th)}$	V_{BB} limiter threshold detector level		–	2.8	–	V
t_{att}	attack time when V_{BB} jumps below $V_{BB(th)}$	C_{DLL} = 470 nF	–	1	–	ms
Volume control for the loudspeaker amplifier (VCI) (TEA1096A only); related to the loudspeaker amplifier volume control						
$\|Z_i\|$	input impedance		–	1	–	MΩ
V_{VCImin}	minimum DC level on pin VCI for 0 dB control on loudspeaker amplifier	I_{line} = 30 mA; V_{LSI} = 10 mV (RMS)	–	2.8	–	V
V_{VCI}	DC level on pin VCI for −6 dB control on loudspeaker amplifier	I_{line} = 30 mA; v_{LSI} = 10 mV (RMS)	–	1.63	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (PD)						
V_{IL}	LOW level input voltage		–	–	0.5	V
V_{IH}	HIGH level input voltage		1.5	–	V_{DD} +0.4	V
I_{PD}	input current in power-down condition	PD = HIGH	–	6	10	μA
Mute input (MUTE)						
V_{IL}	LOW level input voltage		–	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{DD} +0.4	V
I_{MUTE}	input current	MUTE = HIGH	–	15	20	μA
Microphone mute input (DLS/$\overline{\text{MMUTE}}$)						
V_{IL}	LOW level input voltage		–	–	0.3	V
$I_{sink(DLS)}$	sink current	DLS/$\overline{\text{MMUTE}}$ = LOW	–	60	100	μA
t_{rel}	release time after a LOW level on pin DLS/$\overline{\text{MMUTE}}$	C_{DLS} = 470 nF	–	15	–	ms
ΔG_{txm}	gain reduction when DLS/$\overline{\text{MMUTE}}$ is short-circuited to V_{EE}	DLS/$\overline{\text{MMUTE}}$ = LOW	60	80	–	dB
Disable input for loudspeaker amplifier (DLL/DIL)						
V_{IL}	LOW level input voltage		–	–	0.25	V
$I_{sink(DLL/DIL)}$	sink current	DLL/DIL = LOW	–	75	120	μA
t_{rel}	release time after a LOW level on pin DLL/DIL	I_{line} = 30 mA; C_{DDL} = 470 nF	–	10	–	ms
ΔG_{lm}	gain reduction when DLL is short-circuited to V_{EE}	DLL/DIL = LOW	60	80	–	dB

Notes

1. This gives the current available for receiving, listening-in and peripherals at this line current.
2. Both gains, microphone and sending DTMF, are determined in the same way by the resistor R_{GAS}.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

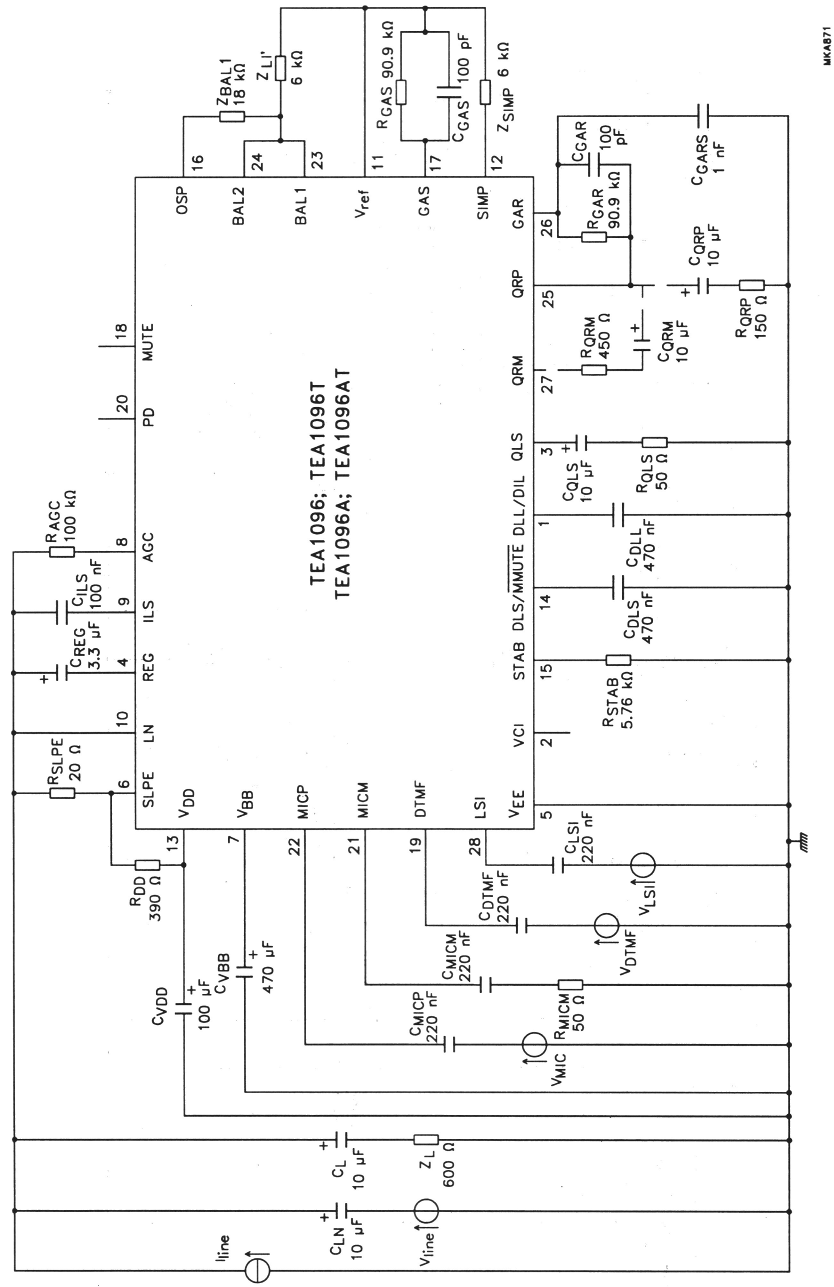

TEA1096; TEA1096T
TEA1096A; TEA1096AT
MKA871
OSP
BAL2
BAL1
V_{ref}
GAS
SIMP
GAR
QRP
QRM
QLS
DLL/DIL
DLS/$\overline{MMUTE}$
STAB
VCI
V_{EE}
LSI
DTMF
MICM
MICP
V_{BB}
V_{DD}
SLPE
LN
REG
ILS
AGC
PD
MUTE
Z_{BAL1} 18 kΩ
Z_{LI}' 6 kΩ
R_{GAS} 90.9 kΩ
C_{GAS} 100 pF
Z_{SIMP} 6 kΩ
C_{GAR} 100 pF
R_{GAR} 90.9 kΩ
C_{GARS} 1 nF
C_{QRP} 10 μF
R_{QRP} 150 Ω
R_{QRM} 450 Ω
C_{QRM} 10 μF
C_{QLS} 10 μF
R_{QLS} 50 Ω
C_{DLL} 470 nF
C_{DLS} 470 nF
R_{STAB} 5.76 kΩ
C_{LSI} 220 nF
V_{LSI}
C_{DTMF} 220 nF
V_{DTMF}
C_{MICM} 220 nF
R_{MICM} 50 Ω
C_{MICP} 220 nF
V_{MIC}
C_{VBB} 470 μF
C_{VDD} 100 μF
R_{DD} 390 Ω
R_{SLPE} 20 Ω
C_{REG} 3.3 μF
C_{ILS} 100 nF
R_{AGC} 100 kΩ
C_L 10 μF
Z_L 600 Ω
C_{LN} 10 μF
V_{line}
I_{line}
16
24
23
11
17
12
26
25
27
3
1
14
15
2
5
28
19
21
22
7
13
6
10
4
9
8
20
18

Fig.22 Test diagram.

APPLICATION INFORMATION

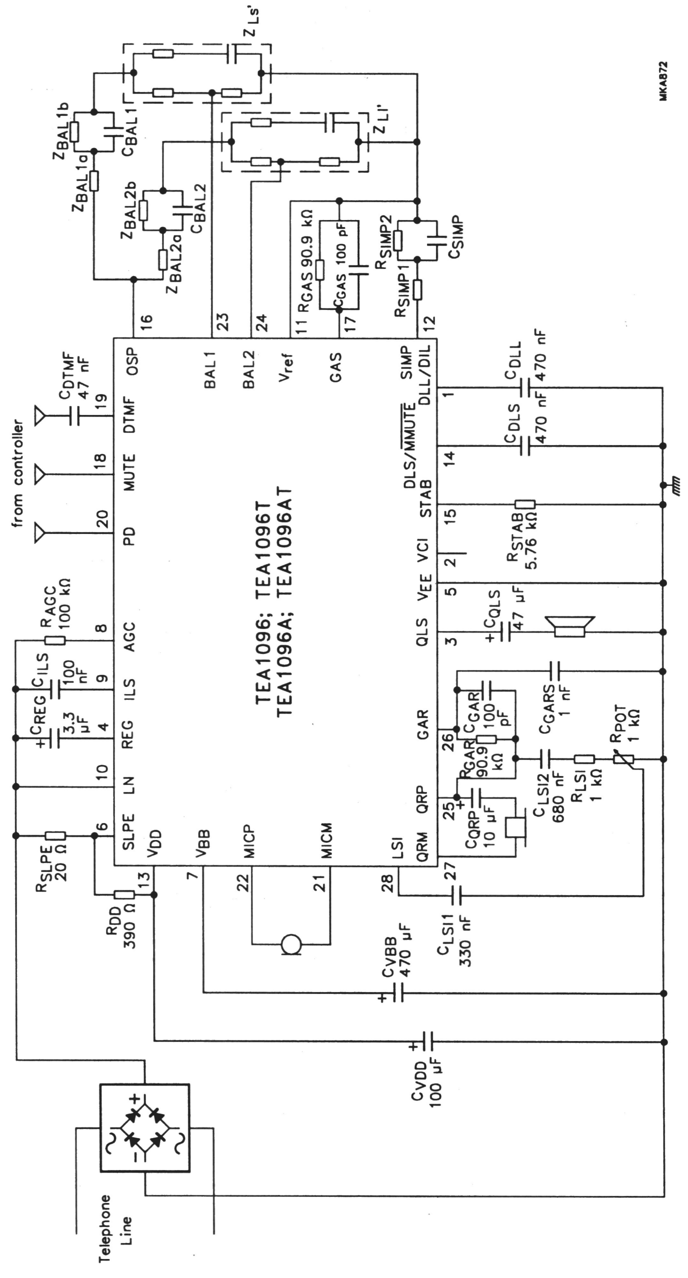

TEA1096; TEA1096T
TEA1096A; TEA1096AT
OSP
BAL1
BAL2
V_{ref}
GAS
SIMP
DLL/DIL
DLS/$\overline{MMUTE}$
STAB
VCI
VEE
QLS
GAR
QRP
QRM
LSI
MICM
MICP
VBB
VDD
SLPE
LN
REG
ILS
AGC
PD
MUTE
DTMF
16
23
24
11
17
12
1
14
15
2
5
3
26
25
27
28
21
22
7
13
6
10
4
9
8
20
18
19
from controller
C_{DTMF} 47 nF
R_{AGC} 100 kΩ
C_{ILS} 100 nF
C_{REG} 3.3 µF
R_{SLPE} 20 Ω
R_{DD} 390 Ω
C_{VBB} 470 µF
C_{VDD} 100 µF
C_{LSI1} 330 nF
C_{QRP} 10 µF
C_{LSI2} 680 nF
R_{LSI} 1 kΩ
R_{GAR} 90.9 kΩ
C_{GAR} 100 pF
C_{GARS} 1 nF
R_{POT} 1 kΩ
C_{QLS} 47 µF
R_{STAB} 5.76 kΩ
C_{DLS} 470 nF
C_{DLL} 470 nF
R_{GAS} 90.9 kΩ
C_{GAS} 100 pF
R_{SIMP1}
R_{SIMP2}
C_{SIMP}
Z_{BAL1a}
Z_{BAL1b}
C_{BAL1}
Z_{BAL2a}
Z_{BAL2b}
C_{BAL2}
$Z_{Ll'}$
$Z_{Ls'}$
Telephone Line
MKA872

Fig.23 Basic application with a complex line impedance.

Low voltage versatile telephone transmission circuits with dialler

TEA1112; TEA1112A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high impedance input (32 kΩ) for electret microphones
- DTMF input with confidence tone
- MUTE input for pulse or DTMF dialling (TEA1112)
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling (TEA1112A)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- AGC line loss compensation for microphone and earpiece amplifiers
- LED on-hook/off-hook status indication
- Microphone mute function.

APPLICATION

- Line powered telephone sets, cordless telephones, fax machines, answering machines.

GENERAL DESCRIPTION

The TEA1112; TEA1112A are bipolar integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between speech and dialling. The ICs operate at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

A current (proportional to the line current and internally limited to a typical value of 19.5 mA) is available to drive an LED which indicates the on-hook/off-hook status.

The microphone amplifier can be disabled during speech condition by means of a microphone mute function.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
$I_{LED(max)}$	maximum supply current available	I_{line} < 18 mA	–	0.5	–	mA
		I_{line} > 76 mA	–	19.5	–	mA
V_{LN}	DC line voltage	I_{line} = 15 mA	3.35	3.65	3.95	V
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; I_p = 0 mA	–	2.9	–	V
G_{vtrx}	typical voltage gain range					
	microphone amplifier	V_{MIC} = 2 mV (RMS)	38.8	–	51.8	dB
	receiving amplifier	V_{IR} = 6 mV (RMS)	19.2	–	31.2	dB
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA; AGC pin connected to V_{EE}	–	5.8	–	dB
ΔG_{vtxm}	microphone amplifier gain reduction		–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1112	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1112A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1112T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TEA1112AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

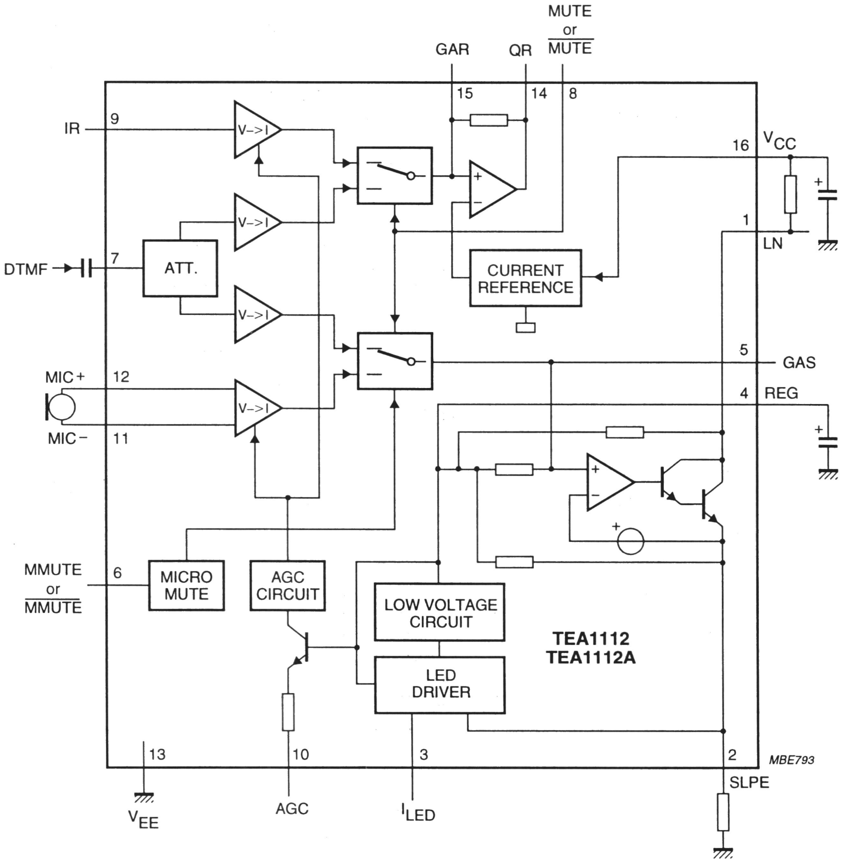

MUTE
or
MUTE
GAR
QR
15
14
8
IR
9
V->I
16
VCC
V->I
1
LN
DTMF
7
ATT.
CURRENT
REFERENCE
V->I
5
GAS
MIC+
12
4
REG
V->I
MIC−
11
MMUTE
or
MMUTE
6
MICRO
MUTE
AGC
CIRCUIT
LOW VOLTAGE
CIRCUIT
TEA1112
TEA1112A
LED
DRIVER
13
10
3
2
MBE793
SLPE
VEE
AGC
ILED

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TEA1112	TEA1112A	
LN	1	1	positive line terminal
SLPE	2	2	slope (DC resistance) adjustment
I_{LED}	3	3	available output current to drive a LED
REG	4	4	line voltage regulator decoupling
GAS	5	5	sending gain adjustment
MMUTE	6	–	microphone mute input
$\overline{\text{MMUTE}}$	–	6	microphone mute input (active LOW)
DTMF	7	7	dual-tone multi-frequency input
MUTE	8	–	mute input to select speech or dialling mode
$\overline{\text{MUTE}}$	–	8	mute input to select speech or dialling mode (active LOW)
IR	9	9	receiving amplifier input
AGC	10	10	automatic gain control/line loss compensation
MIC–	11	11	inverting microphone amplifier input
MIC+	12	12	non-inverting microphone amplifier input
V_{EE}	13	13	negative line terminal
QR	14	14	receiving amplifier output
GAR	15	15	receive gain adjustment
V_{CC}	16	16	supply voltage for speech circuit and peripherals

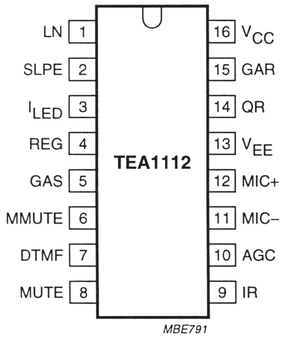

LN 1
SLPE 2
I_{LED} 3
REG 4
GAS 5
MMUTE 6
DTMF 7
MUTE 8
16 V_{CC}
15 GAR
14 QR
13 V_{EE}
12 MIC+
11 MIC–
10 AGC
9 IR
TEA1112
MBE791

Fig.2 Pin configuration (TEA1112).

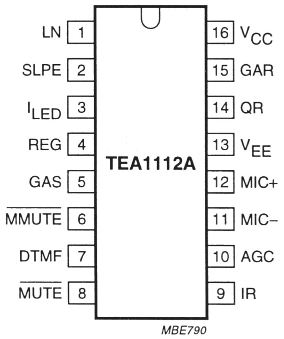

LN 1
SLPE 2
I_{LED} 3
REG 4
GAS 5
$\overline{\text{MMUTE}}$ 6
DTMF 7
$\overline{\text{MUTE}}$ 8
16 V_{CC}
15 GAR
14 QR
13 V_{EE}
12 MIC+
11 MIC–
10 AGC
9 IR
TEA1112A
MBE790

Fig.3 Pin configuration (TEA1112A).

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1112; TEA1112A and their peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.35 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.5), or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section "Set impedance"), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 4 illustrates the supply configuration.

The ICs regulate the line voltage at pin LN, and can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_p - I^* = I_{LED} + I_{sh}$$

Where:

I_{line} = line current

I_{CC} = current consumption of the IC

I_p = supply current for peripheral circuits

I^* = current consumed between LN and V_{EE}

I_{LED} = supply current for the LED component

I_{sh} = the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the LED supply current characteristic, the gain control characteristics, the sidetone level and the maximum output swing on the line.

The internal circuitry of the TEA1112; TEA1112A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula. (see also Fig.6 and Fig.7). R_{CCint} is the internal impedance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$$V_{CC} = V_{CC0} - R_{CCint} \times (I_p - I_{rec})$$

$$V_{CC0} = V_{LN} - R_{CC} \times I_{CC}$$

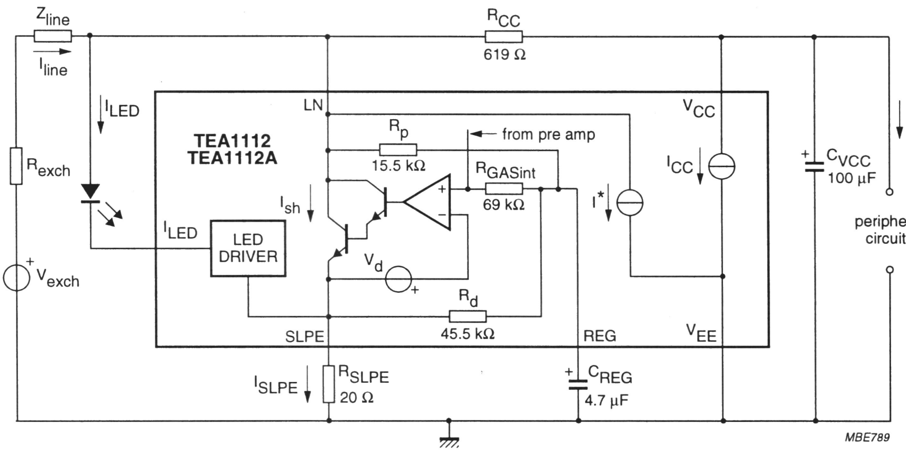
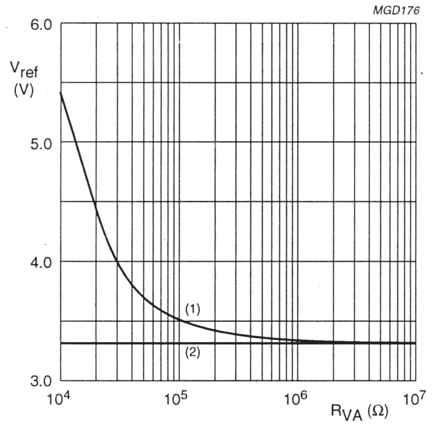


Fig.4 Supply configuration.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.5 Reference voltage adjustment by R_{VA}.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.8.

LED supply (pin I_{LED})

The TEA1112; TEA1112A give an on-hook/off-hook status indication. This is achieved by a current made available to drive an LED connected between pins I_{LED} and LN. In the low voltage area, which corresponds to low line current conditions, no current is available for this LED.

For line currents higher than a threshold, $I_{LEDstart}$, the I_{LED} current increases proportionally to the line current (with a ratio of one third). The I_{LED} current is internally limited to 19.5 mA (see Fig.9). If no LED device is used in the application, the I_{LED} pin should be shorted to pin SLPE.

This LED driver is referenced to SLPE. Consequently, all the I_{LED} supply current will flow through the R_{SLPE} resistor. The AGC characteristics are not disturbed (see Fig.4).

Microphone amplifier (pins MIC+, MIC− and GAS)

The TEA1112; TEA1112A have symmetrical microphone inputs. The input impedance between pins MIC+ and MIC− is 64 kΩ (2 × 32 kΩ). The voltage gain from pins MIC+/MIC− to pin LN is set at 51.8 dB (typ). The gain can be decreased by connecting an external resistor between pins GAS and REG. The adjustment range is 13 dB. A capacitor C_{GAS} connected between pins GAS and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAS} \times R_{GASint}$. R_{GASint} is the internal resistor which sets the gain with a typical value of 69 kΩ.

Automatic gain control is provided on this amplifier for line loss compensation.

Microphone mute (pin MMUTE; TEA1112)

The microphone amplifier can be disabled by activating the microphone mute function. When MMUTE is LOW, the normal speech mode is entered, depending on the level on MUTE (see Table 1). When MMUTE is HIGH, the microphone amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and MIC+/MIC− is attenuated; the gain reduction is 80 dB (typ).

Microphone mute (pin $\overline{\text{MMUTE}}$; TEA1112A)

The microphone amplifier can be disabled by activating the microphone mute function. When $\overline{\text{MMUTE}}$ is LOW, the microphone amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and MIC+/MIC− is attenuated; the gain reduction is 80 dB (typ). When $\overline{\text{MMUTE}}$ is HIGH, the normal speech mode is entered, depending on the level on MUTE (see Table 1).

Receiving amplifier (pins IR, GAR and QR)

The receiving amplifier has one input (IR) and one output (QR). The input impedance between pin IR and pin V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is set at 31.2 dB (typ). The gain can be decreased by connecting an external resistor between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{GARint}$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The relationship $C_{GARS} \geq 20 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltage of the receiving amplifier is specified for continuous wave drive. The maximum output swing depends on the DC line voltage, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_p current consumption of the peripheral circuits and the load impedance.

Automatic gain control is provided on this amplifier for line loss compensation.

Automatic gain control (pin AGC)

The TEA1112; TEA1112A perform automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB (which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km). The ICs have been optimized for an exchange supply voltage of 48 V and a feeding bridge resistance of 600 Ω. In this case, the AGC pin must be connected to pin V_{EE}. An external resistor R_{AGC} can be connected between pins AGC and V_{EE} to comply with other configurations of exchange supply voltage and feeding bridge resistance. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin MUTE; TEA1112)

The mute function performs the switching action between the speech mode and the dialling mode. When MUTE is LOW or open-circuit, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled, depending on the MMUTE level (see Table 1). When MUTE is HIGH, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled.

Mute function (pin $\overline{\text{MUTE}}$; TEA1112A)

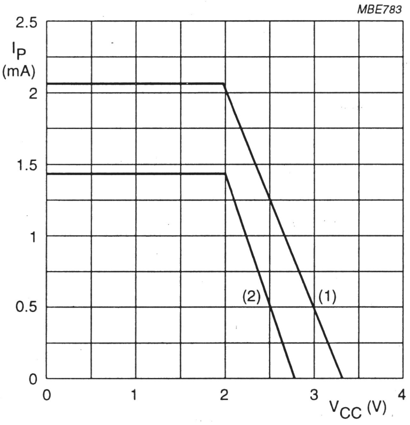
The mute function performs the switching between the speech mode and the dialling mode. When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled. When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled, depending on the MMUTE level (see Table 1).

DTMF amplifier (pin DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1112; TEA1112A have an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is 25.5 dB. When an external resistor is connected between pins REG and GAS to decrease the microphone gain, the DTMF gain varies in the same way (the DTMF gain is 26.3 dB lower than the microphone gain with no AGC control).

The automatic gain control has no effect on the DTMF amplifier.



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.6 Typical current I_p available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

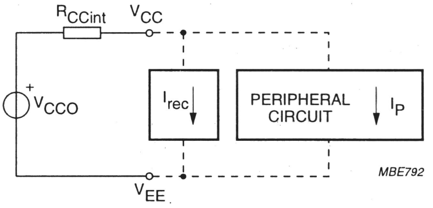
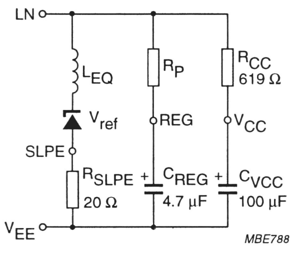

R_{CCint}
V_{CC}
+
V_{CCO}
I_{rec}
PERIPHERAL
CIRCUIT
I_P
MBE792
V_{EE}

Fig.7 V_{CC} supply voltage for peripherals.


LN
L_{EQ}
V_{ref}
SLPE
R_{SLPE}
20 Ω
R_P
REG
+
C_{REG}
4.7 μF
R_{CC}
619 Ω
V_{CC}
+
C_{VCC}
100 μF
V_{EE}
MBE788

$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$
R_p = internal resistance
R_p = 15.5 kΩ

Fig.8 Equivalent impedance between LN and V_{EE}.

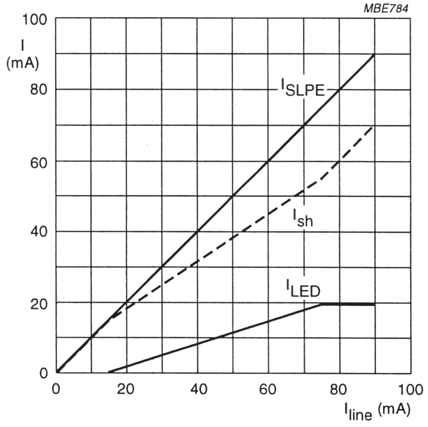


Fig.9 Available current to drive an LED.

MUTE and MMUTE levels for different modes

Table 1 Required MUTE and MMUTE levels to enable the different possible modes

IC	TEA1112		TEA1112A	
Mode	MUTE	MMUTE	MUTE	MMUTE
Speech	L	L	H	H
DTMF dialling	H	X	L	X
Microphone Mute	L	H	H	L

SIDETONE SUPPRESSION

The anti-sidetone network comprising $R_{CC}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Figs.10 and 11) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1112; TEA1112A (see Fig.10) attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Wirebound Telecom Applications Handbook 1995"*, order number 939870672011.

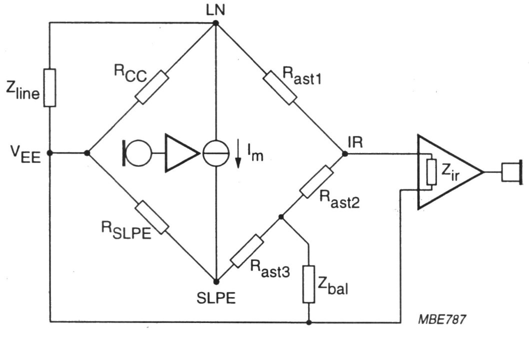


Fig.10 Equivalent circuit of TEA1112; TEA1112A family anti-sidetone bridge.

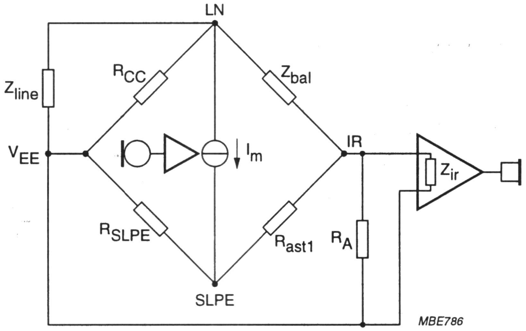


Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

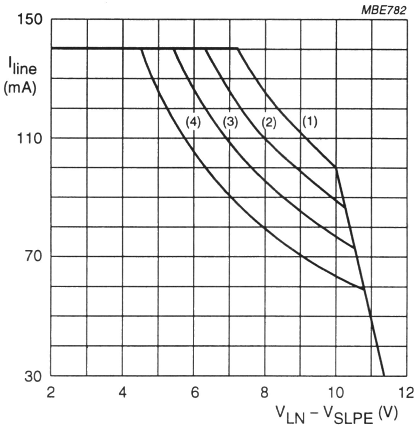
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} – 0.4	12	V
	repetitive line voltage during switch-on or line interruption		V_{EE} – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on pins I_{LED}, SLPE		V_{EE} – 0.4	V_{LN} + 0.4	V
	maximum voltage on all other pins		V_{EE} – 0.4	V_{CC} + 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 12 and 13	–	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 12 and 13			
	TEA1112; TEA1112A		–	625	mW
	TEA1112T; TEA1112AT		–	416	mW
T_{stg}	IC storage temperature		– 40	+125	°C
T_{amb}	operating ambient temperature		– 25	+75	°C

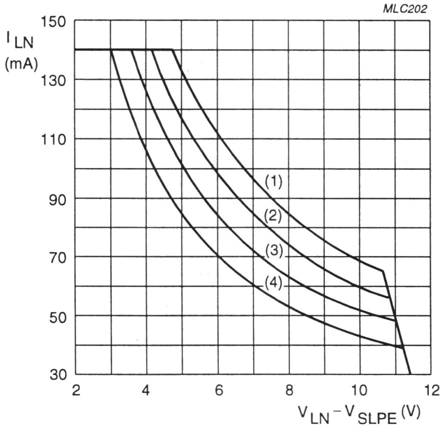
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air (TEA1112; TEA1112A)	80	K/W
	thermal resistance from junction to ambient in free air mounted on epoxy board 40.1 × 19.1 × 1.5 mm (TEA1112T; TEA1112AT)	120	K/W



LINE	T_{amb} (°C)	P_{tot} (MW)
(1)	45	1000
(2)	55	875
(3)	65	750
(4)	75	625

Fig.12 Safe operating area (TEA1112; TEA1112A).



LINE	T_{amb} (°C)	P_{tot} (MW)
(1)	45	666
(2)	55	583
(3)	65	500
(4)	75	416

Fig.13 Safe operating area (TEA1112T; TEA1112AT).

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE	I_{line} = 15 mA	3.1	3.35	3.6	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.45	–	V
		I_{line} = 15 mA	3.35	3.65	3.95	V
		I_{line} = 140 mA	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	I_{line} = 15 mA; $R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.4	–	V
$\Delta V_{LN}/T$	DC line voltage variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = –25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; I_p = 0 mA	–	2.9	–	V
R_{CCint}	equivalent supply voltage impedance	I_{line} = 15 mA; I_p = 0.5 mA	–	550	620	Ω
LED supply (pin I_{LED})						
$I_{line(h)}$	highest line current for I_{LED} < 0.5 mA		–	18	–	mA
$I_{line(l)}$	lowest line current for maximum I_{LED}		–	76	–	mA
$I_{LED(max)}$	maximum supply current available		–	19.5	–	mA
Microphone amplifier (pins MIC+, MIC– and GAS)						
$\lvert Z_i \rvert$	input impedance					
	differential between pins MIC+ and MIC–		–	64	–	kΩ
	single-ended between pins MIC+/MIC– and V_{EE}		–	32	–	kΩ
G_{vtx}	voltage gain from MIC+/MIC– to LN	I_{line} = 15 mA; V_{MIC} = 2 mV (RMS)	50.6	51.8	53	dB
ΔG_{vtxf}	gain variation with frequency referred to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx}T$	gain variation with temperature referred to 25 °C	I_{line} = 15 mA; T_{amb} = –25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
ΔG_{vtxr}	gain voltage reduction range	external resistor connected between GAS and REG	–	–	13	dB
$V_{LN(max)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.4	1.7	–	V
		I_{line} = 4 mA, THD = 10%	–	0.8	–	V
V_{notx}	noise output voltage at pin LN; pins MIC+ / MIC– shorted through 200 Ω	psophometrically weighted (P53 curve)	–	–70.5	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Microphone mute (pins MMUTE; TEA1112 and $\overline{\text{MMUTE}}$; TEA1112A)						
ΔG_{vtxm}	gain reduction	MMUTE = HIGH	–	80	–	dB
		$\overline{\text{MMUTE}}$ = LOW	–	80	–	dB
V_{IL}	LOW level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
V_{IH}	HIGH level input voltage		V_{EE} + 1.5	–	V_{CC} + 0.4	V
I_{MMUTE}	input current	input level = HIGH	–	1.25	3	μA
Receiving amplifier (pins IR, QR and GAR)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	I_{line} = 15 mA; V_{IR} = 6 mV (RMS)	29.7	31.2	32.7	dB
ΔG_{vrxf}	gain variation with frequency referenced to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
ΔG_{vrxT}	gain variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	maximum receiving signal (RMS value)	I_{line} = 15 mA; I_p = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	–	0.25	–	V
		I_{line} = 15 mA; I_p = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	I_{line} = 15 mA; IR open-circuit; R_L = 150 Ω; psophometrically weighted (P53 curve)	–	50	–	μV
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA; AGC pin connected to V_{EE}	–	5.8	–	dB
I_{start}	highest line current for maximum gain	AGC pin connected to V_{EE}	–	26	–	mA
I_{stop}	lowest line current for minimum gain	AGC pin connected to V_{EE}	–	61	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF amplifier (pin DTMF)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vtx}	voltage gain from DTMF to LN	I_{line} = 15 mA; V_{DTMF} = 20 mV (RMS); MUTE or MMUTE = HIGH	24.3	25.5	26.7	dB
ΔG_{vtxf}	gain variation with frequency referenced to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx}T$	gain variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = −25 to +75 °C	–	±0.4	–	dB
G_{vrx}	voltage gain from DTMF to QR (confidence tone)	I_{line} = 15 mA; V_{DTMF} = 20 mV (RMS); R_L = 150 Ω	–	−18	–	dB
Mute function (pins MUTE; TEA1112 and $\overline{\text{MUTE}}$; TEA1112A)						
V_{IL}	LOW level input voltage		$V_{EE} - 0.4$	–	$V_{EE} + 0.3$	V
V_{IH}	HIGH level input voltage		$V_{EE} + 1.5$	–	$V_{CC} + 0.4$	V
I_{MUTE}	input current	input level = HIGH	–	1.25	3	μA
ΔG_{trxm}	gain reduction for microphone and receiving amplifiers					
	TEA1112	MUTE = HIGH	–	80	–	dB
	TEA1112A	$\overline{\text{MUTE}}$ = LOW	–	80	–	dB

APPLICATION INFORMATION

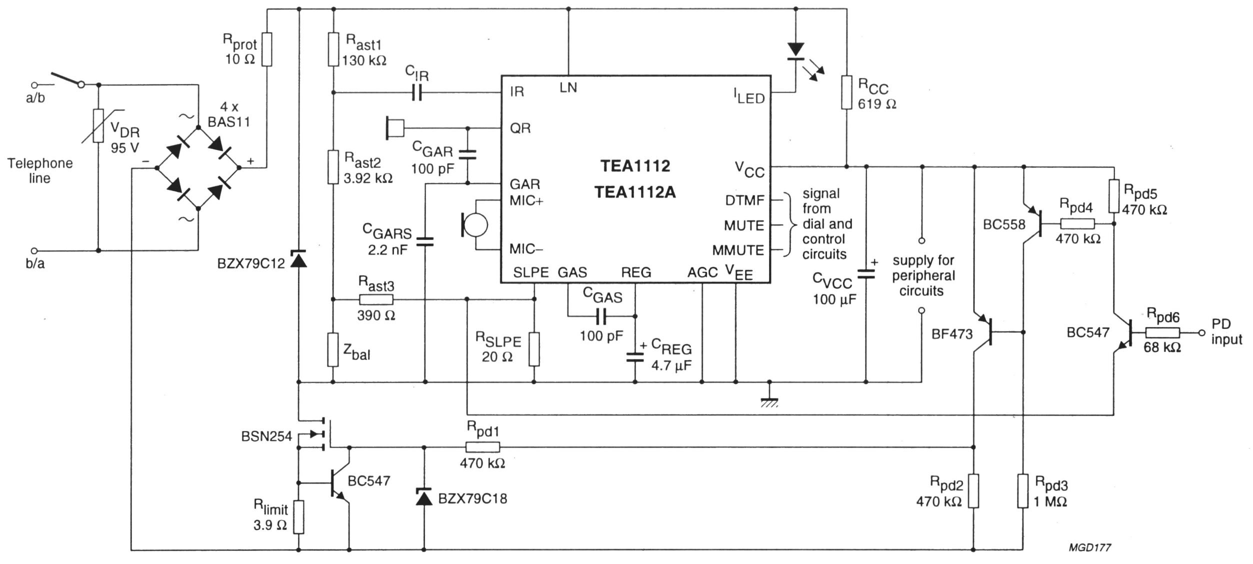

a/b
Telephone line
b/a
V$_{DR}$ 95 V
4 x BAS11
~
~
+
−
R$_{prot}$ 10 Ω
BZX79C12
R$_{ast1}$ 130 kΩ
C$_{IR}$
R$_{ast2}$ 3.92 kΩ
C$_{GAR}$ 100 pF
C$_{GARS}$ 2.2 nF
R$_{ast3}$ 390 Ω
Z$_{bal}$
R$_{SLPE}$ 20 Ω
IR
LN
QR
GAR
MIC+
MIC−
SLPE
GAS
REG
AGC
V$_{EE}$
I$_{LED}$
V$_{CC}$
DTMF
MUTE
MMUTE
TEA1112
TEA1112A
C$_{GAS}$ 100 pF
+ C$_{REG}$ 4.7 μF
R$_{CC}$ 619 Ω
signal from dial and control circuits
+ C$_{VCC}$ 100 μF
supply for peripheral circuits
BF473
BC558
R$_{pd4}$ 470 kΩ
R$_{pd5}$ 470 kΩ
BC547
R$_{pd6}$ 68 kΩ
PD input
BSN254
R$_{pd1}$ 470 kΩ
BC547
R$_{limit}$ 3.9 Ω
BZX79C18
R$_{pd2}$ 470 kΩ
R$_{pd3}$ 1 MΩ
MGD177

Fig.14 Typical application of the TEA1112; TEA1112A in sets with Pulse Dialling or Flash facilities.

Low voltage versatile telephone transmission circuit with dialler interface

TEA1113

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high impedance input (32 kΩ) for electret microphones
- DTMF input with confidence tone
- $\overline{\text{MUTE}}$ input for pulse or DTMF dialling
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Dynamic limitation in the transmit direction to prevent distortion of the transmit line and sidetone signals
- AGC line loss compensation for microphone and earpiece amplifiers
- LED on-hook/off-hook status indication
- Microphone mute function available with switch.

APPLICATION

- Line powered telephone sets, cordless telephones, fax machines and answering machines.

GENERAL DESCRIPTION

The TEA1113 is a bipolar integrated circuit that performs all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between speech and dialling. The IC operates at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

A current (proportional to the line current and internally limited to 19.5 mA) is available to drive an LED which indicates the on-hook/off-hook status.

The transmit signal on the line is dynamically limited to prevent distortion at high transmit levels for both the sending line and sidetone signals. The microphone amplifier can be disabled during speech condition by means of a microphone mute function.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
$I_{LED(max)}$	maximum supply current available	I_{line} < 18 mA	–	0.6	–	mA
		I_{line} > 76 mA	–	19.5	–	mA
V_{LN}	DC line voltage	I_{line} = 15 mA	3.7	4.0	4.3	V
$V_{LN(max, p-p)}$	maximum output voltage swing (peak-to-peak value)	I_{line} = 15 mA	3.8	4.65	–	V
I_{CC}	internal current consumption	V_{CC} = 3.2 V	–	1.3	1.6	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; I_p = 0 mA	2.8	3.2	–	V
G_{vtrx}	typical voltage gain range					
	microphone amplifier	V_{MIC} = 2 mV (RMS)	38.8	–	51.8	dB
	receiving amplifier	V_{IR} = 4 mV (RMS)	19.3	–	31.3	dB
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA; AGC pin connected to V_{EE}	–	5.8	–	dB
ΔG_{vtxm}	microphone amplifier gain reduction		–	80	–	dB

Low voltage versatile telephone transmission circuit with dialler interface

TEA1113

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1113	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1113T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

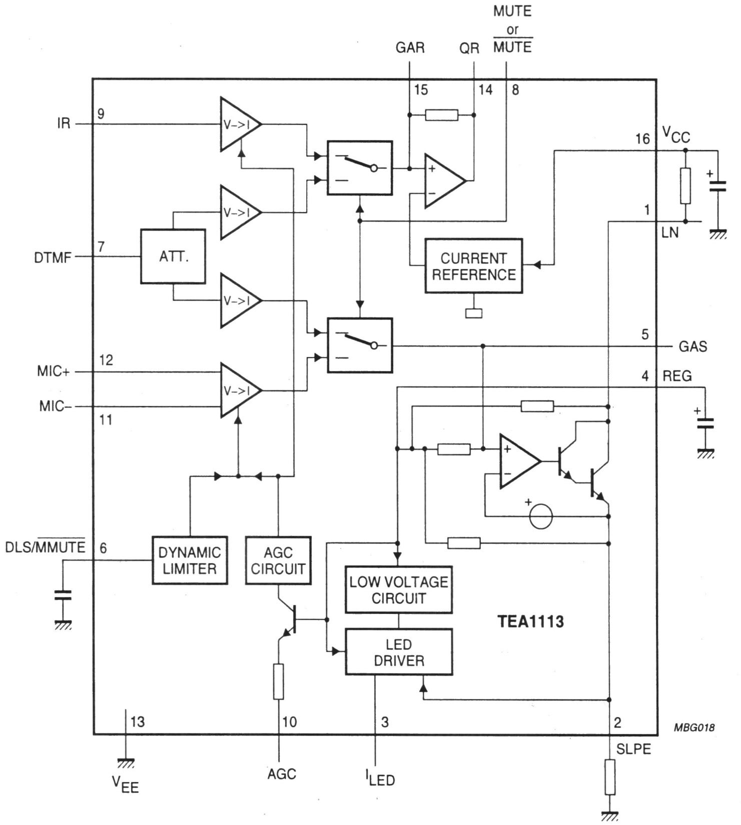

MUTE
or
$\overline{\text{MUTE}}$
GAR
QR
15
14
8
IR
9
V->I
16
V_{CC}
1
LN
DTMF
7
ATT.
CURRENT
REFERENCE
5
GAS
4
REG
MIC+
12
MIC−
11
DLS/$\overline{\text{MMUTE}}$
6
DYNAMIC
LIMITER
AGC
CIRCUIT
LOW VOLTAGE
CIRCUIT
TEA1113
LED
DRIVER
13
10
3
2
SLPE
MBG018
V_{EE}
AGC
I_{LED}

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
SLPE	2	slope (DC resistance) adjustment
I_{LED}	3	available output current to drive an LED
REG	4	line voltage regulator decoupling
GAS	5	sending gain adjustment
DLS/$\overline{\text{MMUTE}}$	6	dynamic limiter timing adjustment and microphone mute input
DTMF	7	dual-tone multi-frequency input
$\overline{\text{MUTE}}$	8	mute input to select speech or dialling mode (active LOW)
IR	9	receiving amplifier input
AGC	10	automatic gain control - line loss compensation
MIC−	11	inverting microphone amplifier input
MIC+	12	non-inverting microphone amplifier input
V_{EE}	13	negative line terminal
QR	14	receiving amplifier output
GAR	15	receive gain adjustment
V_{CC}	16	supply voltage for speech circuit and peripherals

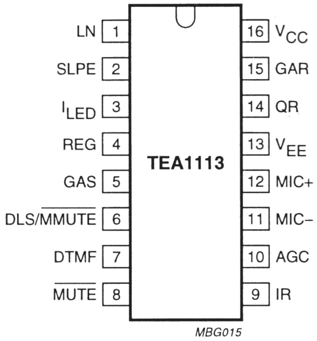


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1113 and its peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.7 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE, or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}. This capacitor, converted into an equivalent inductance (see Section “Set impedance”), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 3 illustrates the supply configuration.

The IC regulates the line voltage at the pin LN, and it can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{CC} - I_{p} - I^{*} = I_{LED} + I_{sh}$$

I_{line}: line current

I_{CC}: current consumption of the IC

I_p: supply current for peripheral circuits

I^*: current consumed between LN and V_{EE}

I_{LED}: supply current for the LED component

I_{sh}: the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the microphone and DTMF gains, the LED supply current characteristic, the gain control characteristics, the sidetone level and the maximum output swing on the line.

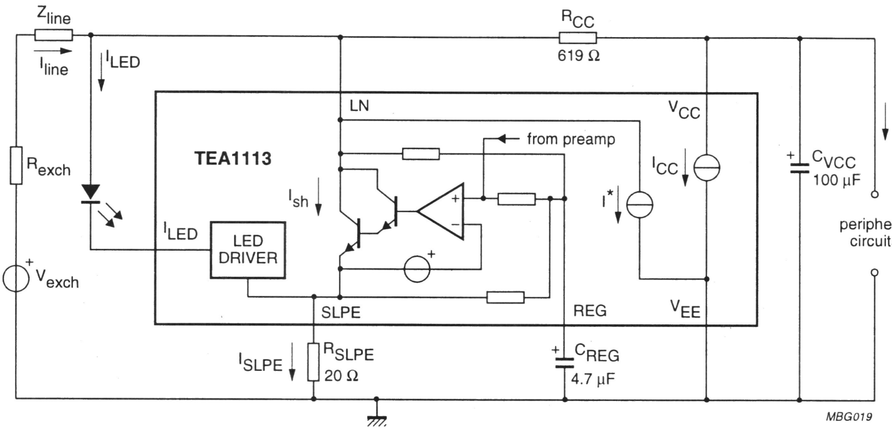
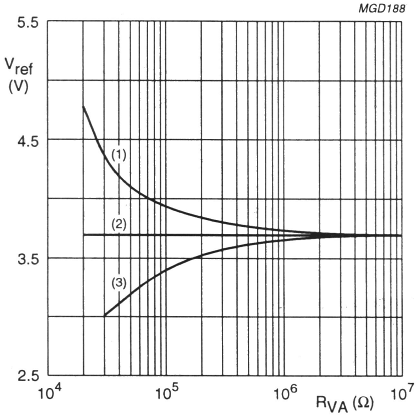

Z_line
I_line
I_LED
R_CC
619 Ω
LN
V_CC
TEA1113
from preamp
R_exch
I_sh
I_CC
I*
C_VCC
100 µF
I_p
I_LED
LED DRIVER
peripheral circuits
V_exch
SLPE
REG
V_EE
I_SLPE
R_SLPE
20 Ω
C_REG
4.7 µF
MBG019

Fig.3 Supply configuration.



(1) R_{VA} between REG and SLPE.
(2) No R_{VA}.
(3) R_{VA} between REG and LN.

Fig.4 Reference voltage adjustment by a R_{VA} resistor.

The internal circuitry of the TEA1113 is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula. (see also Figs 5 and 6). R_{ccint} is the internal impedance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$$V_{CC} = V_{CCO} - R_{ccint} \times (I_p - I_{rec})$$

$$V_{CCO} = V_{LN} - R_{CC} \times I_{CC}$$

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 8 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 8 mA, the circuit has limited sending and receiving levels. This is called the low voltage area.

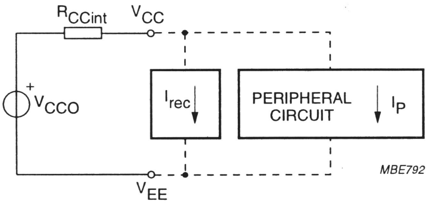


Fig.5 V_{CC} voltage supply for peripherals.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.7.

LED supply (pin I_{LED})

The TEA1113 gives an on-hook/off-hook status indication. This is achieved by a current made available to drive an LED connected between pins I_{LED} and LN. In the low voltage area, which corresponds to low line current conditions, no current is available for this LED. For line currents higher than a threshold current, the I_{LED} current increases proportionally to the line current (with a ratio of one third).The I_{LED} current is internally limited to 19.5 mA (see Fig.8).

This LED driver is referenced to SLPE. Consequently, all the I_{LED} supply current will flow through the R_{SLPE} resistor. The AGC characteristics are not disturbed (see Fig.3 for the supply configuration).

Microphone amplifier (pins MIC+, MIC– and GAS)

The TEA1113 has symmetrical microphone inputs. The input impedance between pins MIC+ and MIC– is 64 kΩ (2 × 32 kΩ). The voltage gain from pins MIC+/MIC– to pin LN is set to 51.8 dB (typ). The gain can be decreased by connecting an external resistor between pins GAS and REG. The adjustment range is 13 dB. A capacitor C_{GAS} connected between pins GAS and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAS} \times R_{GASint}$. R_{GASint} is the internal resistor which sets the gain with a typical value of 69 kΩ.

Automatic gain control is provided on this amplifier for line loss compensation.

Dynamic limiter and microphone mute (pin DLS/$\overline{\text{MMUTE}}$)

The dynamic limiter only acts on the microphone channel, this is to prevent clipping of the line signal. To prevent distortion, the microphone gain is rapidly reduced when peaks on the line signal exceed an internally determined threshold level or when the current in the transmit output stage is insufficient. The time in which the gain reduction is realized is very short (attack time). The microphone channel stays in the reduced gain condition until the peaks on the line signal remain below the threshold level.
The microphone gain then returns to its nominal value after a time determined by the capacitor C_{DLS} (release time).

The maximum output swing on the line depends on the DC voltage setting (V_{ref}). The internal threshold level is automatically adapted.

A LOW level on pin DLS/$\overline{\text{MMUTE}}$ inhibits the microphone inputs MIC+ and MIC− without affecting the DTMF and receiving inputs. Removing the LOW level from pin DLS/$\overline{\text{MMUTE}}$ provides the normal function of the microphone amplifier after a short time which is determined by capacitor C_{DLS}. With the value of the capacitor at 470 nF, the release time is in the order of a few tenths of a millisecond. The microphone mute function can be realized by a simple switch as illustrated in Fig.9.

Receiving amplifier (pins IR, GAR and QR)

The receiving amplifier has one input (IR) and one output (QR). The input impedance between pin IR and pin V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is fixed to 31.3 dB (typ). The gain can be decreased by connecting an external resistor between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{GARint}$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The relationship $C_{GARS} \geq 20 \times C_{GAR}$ must be fulfilled to ensure stability.

The output voltage of the receiving amplifier is specified for continuous wave drive. The maximum output swing depends on the DC line voltage, the R_{CC} resistor, the I_{CC} current consumption of the circuit, the I_p current consumption of the peripheral circuits and the load impedance.

Automatic gain control is provided on this amplifier for line loss compensation.

Automatic gain control (pin AGC)

The TEA1113 performs automatic line loss compensation. The automatic gain control varies the gain of the microphone amplifier and the gain of the receiving amplifier in accordance with the DC line current.
The control range is 5.8 dB (which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km). The ICs have been optimized for an exchange supply voltage of 48 V and a feeding bridge resistance of 600 Ω. In this case, the AGC pin must be connected to pin V_{EE}. An external resistor R_{AGC} can be connected between pins AGC and V_{EE} to comply with other configurations of exchange supply voltage and feeding bridge resistance. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

Mute function (pin $\overline{\text{MUTE}}$)

The mute function performs the switching between the speech mode and the dialling mode. When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifiers inputs are disabled. When $\overline{\text{MUTE}}$ is HIGH, the microphone and receiving amplifiers inputs are enabled while the DTMF input is disabled.

DTMF amplifier (pin DTMF)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1113 has an asymmetrical DTMF input. The input impedance between DTMF and V_{EE} is 20 kΩ. The voltage gain from pin DTMF to pin LN is 25.4 dB. When the resistor R_{GAS} is connected, to decrease the microphone gain, the DTMF gain varies in the same way (the DTMF gain is 26.4 dB lower than the microphone gain with no AGC control).

The automatic gain control has no effect on the DTMF amplifier.

Sidetone suppression

The anti-sidetone network comprising $R_{CC}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Figs.10 and 11) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

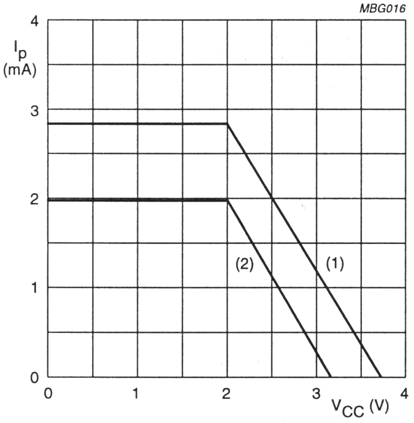
$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

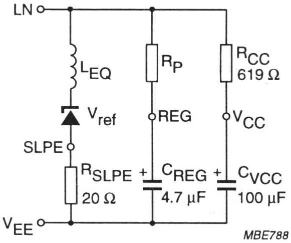
The anti-sidetone network for the TEA1113 (see Fig.10) attenuates the receiving signal from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication "*Wirebound Telecom Applications Handbook 1995*", order number 9398 706 72011 .



(1) With R_{VA} resistor.
(2) Without R_{VA} resistor.

Fig.6 Typical current I_P available from V_{CC} for peripheral circuits at I_{line} = 15 mA.


LN
L_{EQ}
R_P
R_{CC}
619 Ω
V_{ref}
REG
V_{CC}
SLPE
R_{SLPE}
20 Ω
C_{REG}
4.7 μF
C_{VCC}
100 μF
V_{EE}
MBE788

$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$; R_P = internal resistance; R_P = 15.5 kΩ

Fig.7 Equivalent impedance between LN and V_{EE}.

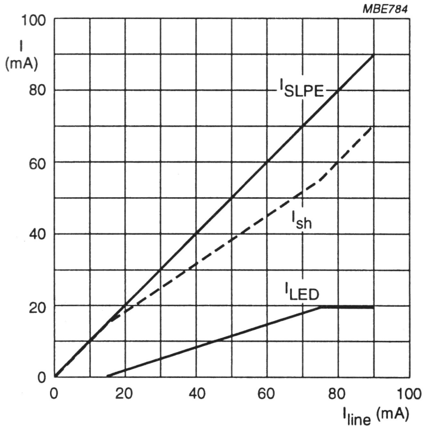


Fig.8 Available current to drive an LED.

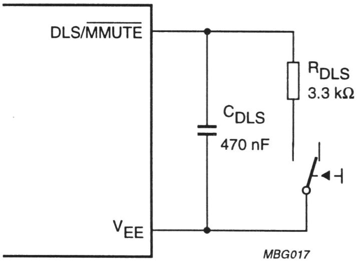

DLS/$\overline{\text{MMUTE}}$
R_{DLS}
3.3 kΩ
C_{DLS}
470 nF
V_{EE}
MBG017

Fig.9 Microphone mute function.

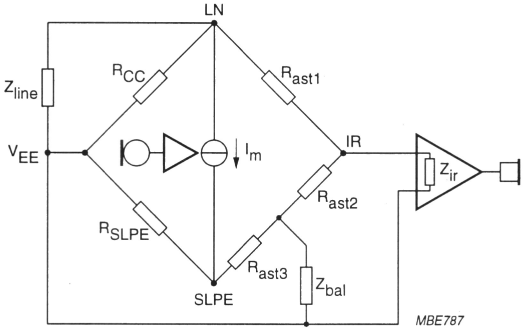

LN
Rcc
Rast1
Zline
VEE
Im
IR
Zir
RSLPE
Rast2
Rast3
Zbal
SLPE
MBE787

Fig.10 Equivalent circuit of TEA1113 family anti-sidetone bridge.

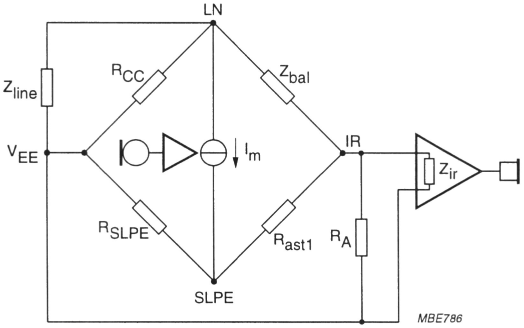

LN
Rcc
Zbal
Zline
VEE
Im
IR
Zir
RSLPE
Rast1
RA
SLPE
MBE786

Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

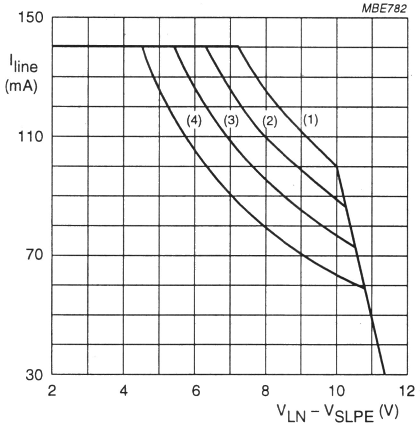
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		V_{EE} − 0.4	12.0	V
	repetitive line voltage during switch-on or line interruption		V_{EE} − 0.4	13.2	V
$V_{n(max)}$	maximum voltage on pins I_{LED}, SLPE		V_{EE} − 0.4	V_{LN} + 0.4	V
	maximum voltage on all other pins		V_{EE} − 0.4	V_{CC}+ 0.4	V
I_{line}	line current	R_{SLPE} = 20 Ω; see Figs 12 and 13	−	140	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 12 and 13			
	TEA1113		−	625	mW
	TEA1113T		−	416	mW
T_{stg}	IC storage temperature		−40	+125	°C
T_{amb}	operating ambient temperature		−25	+75	°C

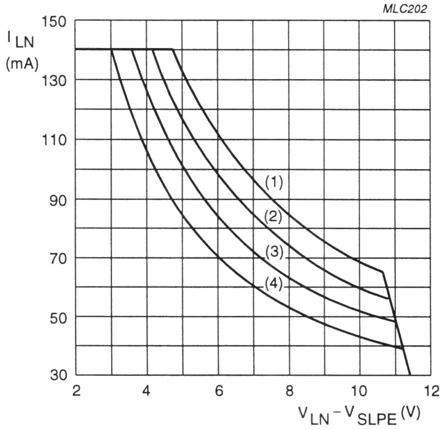
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air (TEA1113)	80	K/W
	thermal resistance from junction to ambient in free air mounted on epoxy board 40.1 × 19.1 × 1.5 mm (TEA1113T)	120	K/W



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	1000
(2)	55	875
(3)	65	750
(4)	75	625

Fig.12 Safe operating area (TEA1113).



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	666
(2)	55	583
(3)	65	500
(4)	75	416

Fig.13 Safe operating area (TEA1113T).

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; C_{DLS} = 470 nF; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE	I_{line} = 15 mA	3.45	3.7	3.95	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.5	–	V
		I_{line} = 15 mA	3.7	4	4.3	V
		I_{line} = 140 mA	–	–	7.0	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	I_{line} = 15 mA; $R_{VA(LN-REG)}$ = 82 kΩ	–	3.6	–	V
		I_{line} = 15 mA; $R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.75	–	V
$\Delta V_{LN}/T$	DC line voltage variation with temperature referenced to 25 °C	I_{line} = 15 mA T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 3.2 V	–	1.3	1.6	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; I_p = 0 mA	2.8	3.2	–	V
R_{ccint}	equivalent supply voltage impedance	I_{line} = 15 mA; I_p = 0.5 mA	–	550	620	Ω
LED supply (pin I_{LED})						
$I_{line(h)}$	highest line current for I_{LED} < 0.6 mA		–	18	–	mA
$I_{line(l)}$	lowest line current for maximum I_{LED}		–	76	–	mA
$I_{LED(max)}$	maximum supply current available		–	19.5	–	mA
Microphone amplifier (pins MIC+, MIC− and GAS)						
$\lvert Z_i \rvert$	input impedance					
	differential between pins MIC+ and MIC−		–	64	–	kΩ
	single-ended between pins MIC+/MIC− and V_{EE}		–	32	–	kΩ
G_{vtx}	voltage gain from MIC+/MIC− to LN	I_{line} = 15 mA; V_{MIC} = 2 mV (RMS)	50.6	51.8	53	dB
ΔG_{vtxf}	gain variation with frequency referenced to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx}T$	gain variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = −25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
ΔG_{vtxr}	gain voltage reduction range	external resistor connected between GAS and REG	–	–	13	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{notx}	noise output voltage at pin LN; pins MIC+ / MIC– shorted through 200 Ω	psophometrically weighted (P53 curve)	–	–70.5	–	dBmp
Dynamic limiter and microphone mute (pin DLS/$\overline{\text{MMUTE}}$)						
DYNAMIC LIMITER BEHAVIOUR						
$V_{LN(max,p-p)}$	maximum output voltage swing on the line (peak-to-peak value)	I_{line} = 15 mA; V_{ref} = 3.7 V	3.8	4.65	–	V
		I_{line} = 4 mA	–	1.6	–	
THD	total harmonic distortion	V_{MIC} = 4 mV (RMS) + 10 dB	–	–	2	%
		V_{MIC} = 4 mV (RMS) + 15 dB	–	–	10	%
t_{att}	attack time, V_{MIC} jumps from 2 mV up to 20 mV	C_{DLS} = 470 nF	–	1.5	5	ms
t_{rel}	release time, V_{MIC} jumps from 20 mV down to 2 mV	C_{DLS} = 470 nF	50	150	–	ms
MICROPHONE MUTE INPUT						
ΔG_{vtxm}	gain reduction	DLS/$\overline{\text{MMUTE}}$ = LOW	–	80	–	dB
V_{IL}	LOW level input voltage		V_{EE} – 0.4	–	V_{EE} + 0.3	V
I_{IL}	LOW level input current		40	60	–	μA
t_{rel}	release time after a LOW level on pin DLS/$\overline{\text{MMUTE}}$	C_{DLS} = 470 nF	–	30	–	ms
Receiving amplifier (pins IR, QR and GAR)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	I_{line} = 15 mA; V_{IR} = 4 mV (RMS)	30.3	31.3	32.3	dB
ΔG_{vrxf}	gain variation with frequency referenced to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx}T$	gain variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = –25 to 75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	Maximum output voltage (RMS value)	I_{line} = 15 mA; I_p = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	240	290	–	mV
		I_{line} = 15 mA; I_p = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	350	410	–	mV
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	I_{line} = 15 mA; R_L = 150 Ω; IR open-circuit; psophometrically weighted (P53 curve)	–	50	–	μV
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for microphone and receiving amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA; AGC pin connected to V_{EE}	–	5.8	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{start}	highest line current for maximum gain	AGC pin connected to V_{EE}	–	25	–	mA
I_{stop}	lowest line current for minimum gain	AGC pin connected to V_{EE}	–	59	–	mA
DTMF amplifier (pin DTMF)						
$\|Z_i\|$	input impedance		–	20	–	kΩ
G_{vdtmf}	voltage gain from DTMF to LN	I_{line} = 15 mA; V_{DTMF} = 25 mV (RMS); $\overline{MUTE}$ = HIGH	24.2	25.4	26.6	dB
ΔG_{vdtmff}	gain variation with frequency referenced to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
ΔG_{vdtmfT}	gain variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = −25 to +75 °C	–	±0.5	–	dB
G_{vct}	voltage gain from DTMF to QR (confidence tone)	I_{line} = 15 mA; R_L = 150 Ω; V_{DTMF} = 25 mV (RMS);	–	−18	–	dB
Mute function (pin $\overline{MUTE}$)						
V_{IL}	LOW level input voltage		$V_{EE} - 0.4$	–	$V_{EE} + 0.3$	V
V_{IH}	HIGH level input voltage		$V_{EE} + 1.5$	–	$V_{CC} + 0.4$	V
I_{MUTE}	input current	input level = HIGH	–	1.25	3	μA
ΔG_{vtrxm}	gain reduction for microphone and receiving amplifiers	$\overline{MUTE}$ = LOW	–	80	–	dB

APPLICATION INFORMATION

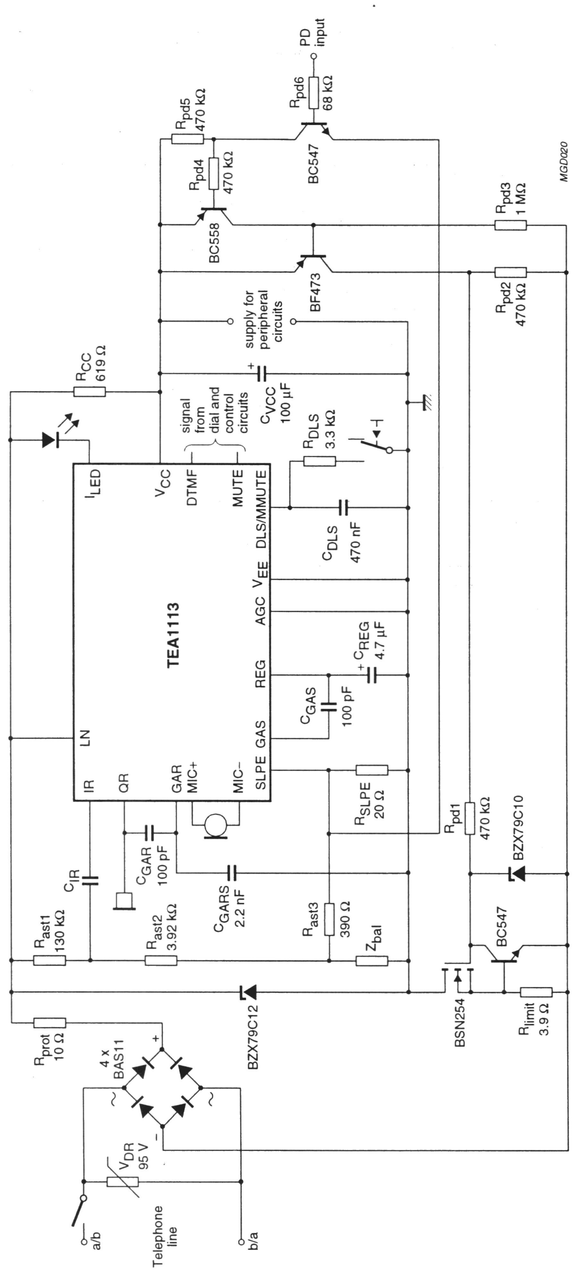

TEA1113
ILED
VCC
DTMF
MUTE
DLS/MMUTE
VEE
AGC
REG
GAS
SLPE
MIC–
GAR
MIC+
QR
IR
LN
PD input
Rpd6 68 kΩ
BC547
Rpd5 470 kΩ
Rpd4 470 kΩ
BC558
Rpd3 1 MΩ
BF473
Rpd2 470 kΩ
MGD020
supply for peripheral circuits
RCC 619 Ω
signal from dial and control circuits
CVCC 100 µF
RDLS 3.3 kΩ
CDLS 470 nF
CREG 4.7 µF
CGAS 100 pF
RSLPE 20 Ω
Rpd1 470 kΩ
BZX79C10
CIR
CGAR 100 pF
CGARS 2.2 nF
Rast1 130 kΩ
Rast2 3.92 kΩ
Rast3 390 Ω
Zbal
BC547
BSN254
Rlimit 3.9 Ω
BZX79C12
Rprot 10 Ω
4 x BAS11
VDR 95 V
a/b
Telephone line
b/a

Fig.14 Typical application of the TEA1113 in sets with Pulse Dialling or Flash facilities.

Versatile cordless transmission circuit TEA1118; TEA1118A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- Provides a supply for external circuits
- Symmetrical high impedance transmit inputs (64 kΩ) with large signals handling capabilities [up to 1 V (RMS value) with less than 2% THD]
- Receive amplifier for dynamic, magnetic or piezoelectric earpieces
- AGC line loss compensation for transmit and earpiece amplifiers
- DTMF input with confidence tone (TEA1118A only)
- MUTE input for pulse or DTMF dialling (TEA1118A only)
- Transmit mute function, also enabling the DTMF input (TEA1118A only).

APPLICATIONS

- Cordless telephone base stations
- Fax machines
- Answering machines.

GENERAL DESCRIPTION

The TEA1118 and TEA1118A are bipolar integrated circuits that perform all speech and line interface functions required in cordless telephone base stations. The ICs operate at a line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of telephone sets connected in parallel.

The TEA1118A offers in addition to the TEA1118 electronic switching between speech and dialling. Moreover the transmit amplifier can be disabled during speech condition by means of a transmit mute function.

All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	1	–	11	mA
V_{LN}	DC line voltage	I_{line} = 15 mA	3.35	3.65	3.95	V
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; I_P = 0 mA	–	2.9	–	V
G_{vtrx}	typical voltage gain range					
	transmit amplifier (TEA1118A only)	V_{TX} = 200 mV (RMS)	–	–	11	dB
	transmit amplifier (TEA1118 only)	V_{TX} = 200 mV (RMS)	tbf	–	11	dB
	receive amplifier	V_{IR} = 4 mV (RMS)	19	–	31	dB
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA; AGC pin connected to V_{EE}	–	5.8	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1118M	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TEA1118AM	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1
TEA1118AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

BLOCK DIAGRAMS

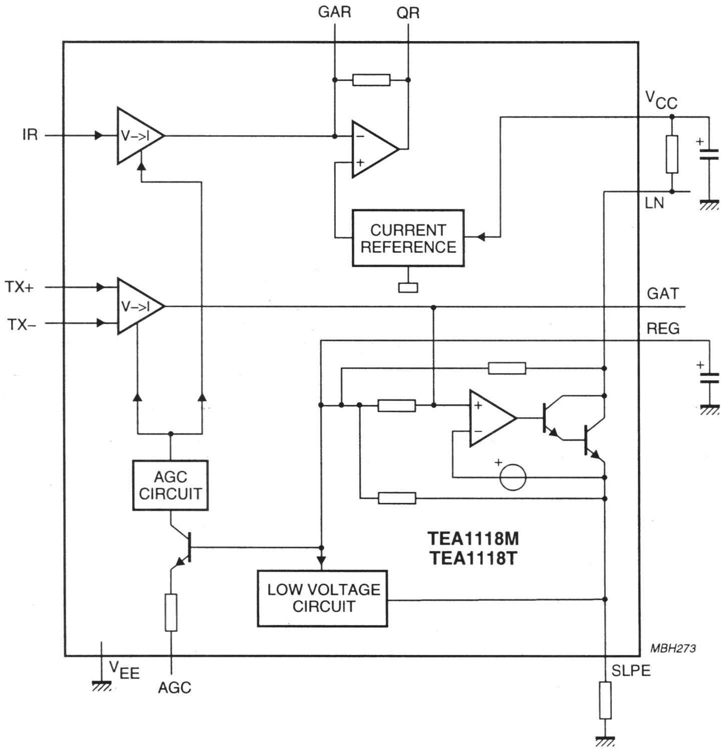

GAR
QR
IR
V->I
V_{CC}
LN
CURRENT REFERENCE
TX+
TX−
V->I
GAT
REG
AGC CIRCUIT
TEA1118M
TEA1118T
LOW VOLTAGE CIRCUIT
MBH273
V_{EE}
AGC
SLPE

Fig.1 Block diagram (TEA1118).

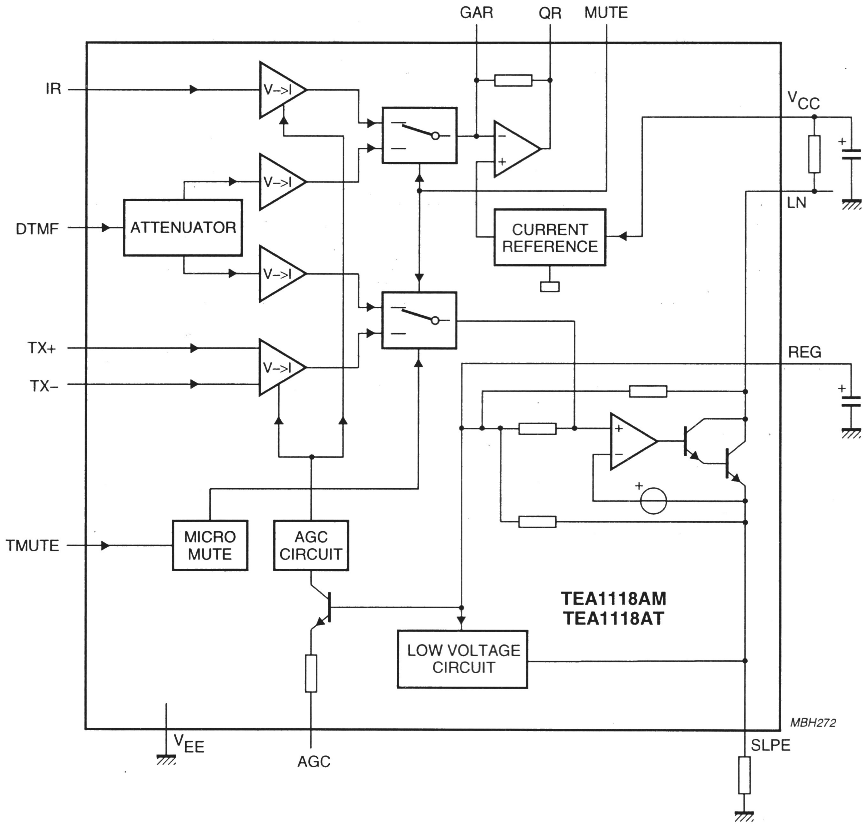

GAR
QR
MUTE
IR
V->I
V->I
V->I
V->I
DTMF
ATTENUATOR
VCC
LN
CURRENT REFERENCE
TX+
TX−
REG
TMUTE
MICRO MUTE
AGC CIRCUIT
TEA1118AM
TEA1118AT
LOW VOLTAGE CIRCUIT
VEE
AGC
SLPE
MBH272

Fig.2 Block diagram (TEA1118A).

PINNING

SYMBOL	TEA1118		TEA1118A		DESCRIPTION
	SO14	SSOP16	SO14	SSOP16	
LN	1	1	1	1	positive line terminal
SLPE	2	2	2	2	slope (DC resistance) adjustment
REG	3	3	3	3	line voltage regulator decoupling
GAT	4	4	–	–	transmit gain adjustment
TMUTE	–	–	4	5	transmit mute input
DTMF	–	–	5	6	dual-tone multi-frequency input
MUTE	–	–	6	8	mute input to select speech or dialling mode
IR	7	9	7	9	receive amplifier input
AGC	8	10	8	10	automatic gain control/line loss compensation
TX–	9	11	9	11	inverting transmit amplifier input
TX+	10	12	10	12	non-inverting transmit amplifier input
V_{EE}	11	13	11	13	negative line terminal
QR	12	14	12	14	receive amplifier output
GAR	13	15	13	15	receive gain adjustment
V_{CC}	14	16	14	16	supply voltage for speech circuit and peripherals
n.c.	5 and 6	5 to 8	–	4 and 7	not connected

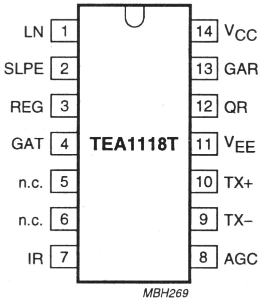

TEA1118T
LN 1
SLPE 2
REG 3
GAT 4
n.c. 5
n.c. 6
IR 7
8 AGC
9 TX−
10 TX+
11 V_{EE}
12 QR
13 GAR
14 V_{CC}
MBH269

Fig.3 Pin configuration (TEA1118T).

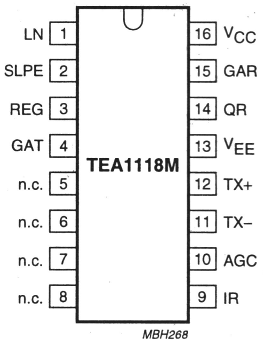

TEA1118M
LN 1
SLPE 2
REG 3
GAT 4
n.c. 5
n.c. 6
n.c. 7
n.c. 8
9 IR
10 AGC
11 TX−
12 TX+
13 V_{EE}
14 QR
15 GAR
16 V_{CC}
MBH268

Fig.4 Pin configuration (TEA1118M).

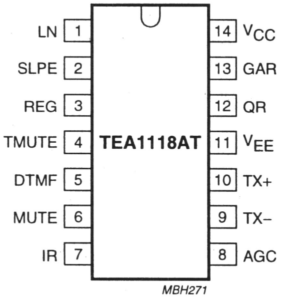

TEA1118AT
LN 1
SLPE 2
REG 3
TMUTE 4
DTMF 5
MUTE 6
IR 7
8 AGC
9 TX−
10 TX+
11 V_{EE}
12 QR
13 GAR
14 V_{CC}
MBH271

Fig.5 Pin configuration (TEA1118AT).

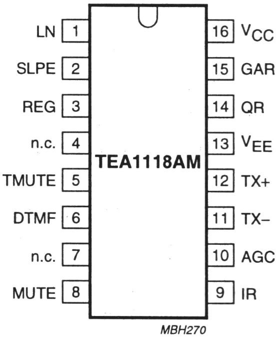

TEA1118AM
LN 1
SLPE 2
REG 3
n.c. 4
TMUTE 5
DTMF 6
n.c. 7
MUTE 8
9 IR
10 AGC
11 TX−
12 TX+
13 V_{EE}
14 QR
15 GAR
16 V_{CC}
MBH270

Fig.6 Pin configuration (TEA1118AM).

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supplies (pins LN, SLPE, V_{CC} and REG)

The supply for the TEA1118 and TEA1118A and their peripherals is obtained from the telephone line.

The ICs generate a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 3.35 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}).
It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.11), or decreased by connecting the R_{VA} resistor between pins REG and LN. The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to V_{EE}.
This capacitor, converted into an equivalent inductance (see Section “Set impedance”), realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (R_{CC} in the audio-frequency range). The voltage at pin SLPE is proportional to the line current. Figure 7 illustrates the supply configuration.

The ICs regulate the line voltage at pin LN, and it can be calculated as follows:

$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$

$I_{SLPE} = I_{line} - I_{CC} - I_P - I^* = I_{sh}$

where:

- I_{line}: line current
- I_{CC}: current consumption of the IC
- I_P: supply current for peripheral circuits
- I^*: current consumed between LN and V_{EE}
- I_{sh}: the excess line current shunted to SLPE (and V_{EE}) via LN.

The preferred value for R_{SLPE} is 20 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the transmit gain and the DTMF gain (TEA1118A only), the gain control characteristics, the sidetone level and the maximum output swing on the line.

The internal circuitry of the TEA1118 and TEA1118A is supplied from pin V_{CC}. This voltage supply is derived from the line voltage by means of a resistor (R_{CC}) and must be decoupled by a capacitor C_{VCC}. It may also be used to supply peripheral circuits such as dialling or control circuits. The V_{CC} voltage depends on the current consumed by the IC and the peripheral circuits as shown by the formula (see also Figs 8 and 9). R_{CCint} is the internal equivalent resistance of the voltage supply point, and I_{rec} is the current consumed by the output stage of the earpiece amplifier.

$V_{CC} = V_{CCO} - R_{CCint} \times (I_P - I_{rec})$

$V_{CCO} = V_{LN} - R_{CC} \times I_{CC}$

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the telephone line (R_{line}) and the reference voltage (V_{ref}). With line currents below 7.5 mA, the internal reference voltage (generating V_{ref}) is automatically adjusted to a lower value.
This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At currents below 7.5 mA, the circuit has limited transmit and receive levels. This is called the low voltage area.

Set impedance

In the audio frequency range, the dynamic impedance is mainly determined by the R_{CC} resistor. The equivalent impedance of the circuits is illustrated in Fig.10.

Transmit amplifier (pins TX+, TX− and GAT)

The TEA1118 and TEA1118A have symmetrical transmit inputs. The input impedance between pins TX+ and TX− is 64 kΩ (2 times 32 kΩ). The voltage gain from pins TX+/TX− to pin LN is set at 11 dB.

Automatic gain control is provided on this amplifier for line loss compensation.

The gain of the TEA1118 can be decreased by connecting an external resistor between pins GAT and REG. The adjustment range is still to be fixed. A capacitor C_{GAT} connected between pins GAT and REG can be used to provide a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAT} \times R_{GATint}$ transmit. R_{GATint} is the internal resistor which sets the gain with a typical value which still has to be defined.

Transmit mute (pin TMUTE; TEA1118A only)

The transmit amplifier can be disabled by activating the transmit mute function. When TMUTE is LOW, the normal speech mode is entered, depending on the level on MUTE. When TMUTE is HIGH, the transmit amplifier inputs are disabled while the DTMF input is enabled (no confidence tone is provided). The voltage gain between LN and TX+/TX− is attenuated; the gain reduction is 80 dB.

Receive amplifier (pins IR, GAR and QR)

The receive amplifier has one input (IR) and one output (QR). The input impedance between pins IR and V_{EE} is 20 kΩ. The voltage gain from pin IR to pin QR is set at 31 dB. The gain can be decreased by connecting an external resistor between pins GAR and QR; the adjustment range is 12 dB. Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and V_{EE}) ensure stability. The C_{GAR} capacitor provides a first-order low-pass filter. The cut-off frequency corresponds to the time constant $C_{GAR} \times R_{GARint}$. R_{GARint} is the internal resistor which sets the gain with a typical value of 100 kΩ. The relationship $C_{GARS} \geq 20 \times C_{GAR}$ must be fulfilled to ensure stability.

Automatic gain control is provided on this amplifier for line loss compensation.

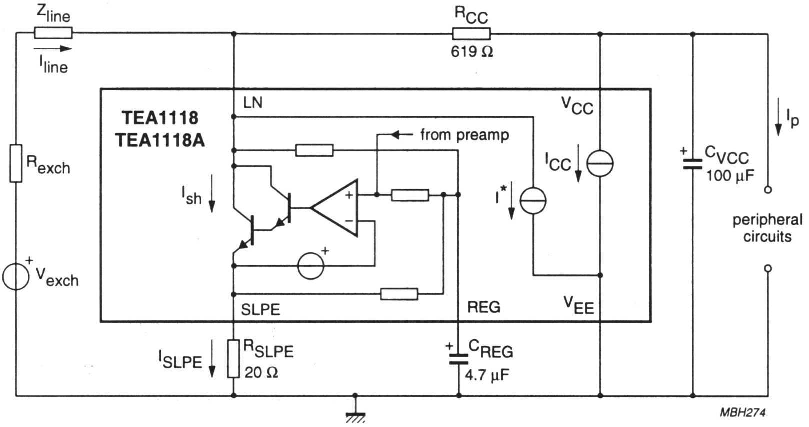
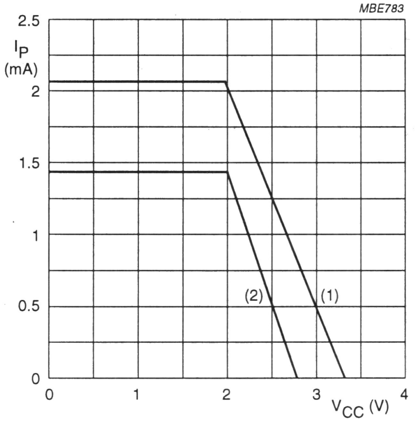

Z_line
I_line
R_exch
V_exch
+
R_CC
619 Ω
TEA1118
TEA1118A
LN
V_CC
from preamp
I_sh
I_CC
I*
SLPE
REG
V_EE
I_SLPE
R_SLPE
20 Ω
C_REG
4.7 μF
C_VCC
100 μF
I_p
peripheral circuits
MBH274

Fig.7 Supply configuration.



(1) With R_{VA} resistor.

(2) Without R_{VA} resistor.

Fig.8 Typical current I_P available from V_{CC} for peripheral circuits at I_{line} = 15 mA.

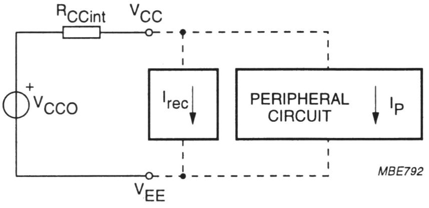
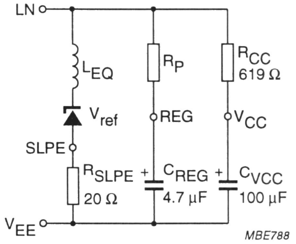

R_{CCint}
V_{CC}
V_{CCO}
+
I_{rec}
PERIPHERAL CIRCUIT
I_P
V_{EE}
MBE792

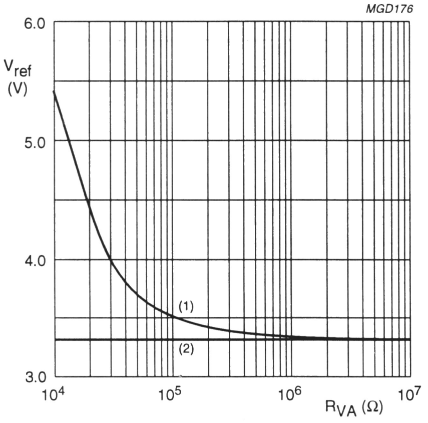
Fig.9 V_{CC} voltage supply for peripheral.


LN
L_{EQ}
R_P
R_{CC}
619 Ω
V_{ref}
REG
V_{CC}
SLPE
R_{SLPE}
20 Ω
C_{REG}
4.7 μF
C_{VCC}
100 μF
V_{EE}
MBE788

$L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$.

R_P = internal resistance (15.5 kΩ).

Fig.10 Equivalent impedance between LN and V_{EE}.



(1) Influence of R_{VA} on V_{ref}.

(2) V_{ref} without influence of R_{VA}.

Fig.11 Reference voltage adjustment by R_{VA}.

Automatic Gain Control (pin AGC)

The TEA1118 and TEA1118A perform automatic line loss compensation. The automatic gain control varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current.
The control range is 5.8 dB (which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km). The ICs have been optimized for an exchange supply voltage of 48 V and a feeding bridge resistance of 600 Ω. In this case, the AGC pin must be connected to pin V_{EE}. An external resistor R_{AGC} can be connected between pins AGC and V_{EE} to comply with other configurations of exchange supply voltage and feeding bridge resistance. This resistor enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by the resistor). The AGC function is disabled when pin AGC is left open-circuit.

DTMF amplifier (pin DTMF; TEA1118A only)

When the DTMF amplifier is enabled, dialling tones may be sent on line. These tones can be heard in the earpiece at a low level (confidence tone).

The TEA1118A has an asymmetrical DTMF input.
The input impedance between DTMF and V_{EE} is 20 kΩ.
The voltage gain from pin DTMF to pin LN is 17 dB.

The automatic gain control has no effect on the DTMF amplifier.

Mute function (pin MUTE; TEA1118A only)

The mute function performs the switching action between the speech mode and the dialling mode. When MUTE is LOW or open-circuit, the transmit and receive amplifiers inputs are enabled while the DTMF input is disabled, depending on the TMUTE level. When MUTE is HIGH, the DTMF input is enabled and the transmit and receive amplifiers inputs are disabled.

Sidetone suppression

The anti-sidetone network comprising $R_{CC}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Figs 12 and 13) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{[R_{ast2} \times (R_{ast3} + R_{SLPE})]}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length. Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.
The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the TEA1118 and TEA1118A (see Fig.12) attenuates the receive signal from the line by 32 dB before it enters the receive amplifier. The attenuation is almost constant over the whole audio frequency range.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *"Wirebound Telecom Applications Handbook 1995"*, order number 9398 706 72011.

MUTE and TMUTE levels for different modes (TEA1118A only)

Table 1 Required MUTE and TMUTE levels to enable the different possible modes

MODE	CHANNEL				MUTE	TMUTE
	TRANSMIT	RECEIVE	DTMF	CONFIDENCE TONE		
Speech	on	on	off	off	L	L
DTMF dialling	off	off	on	on	H	X(1)
Transmit mute	on	off	on	off	L	H

Note

1. X = don't care.

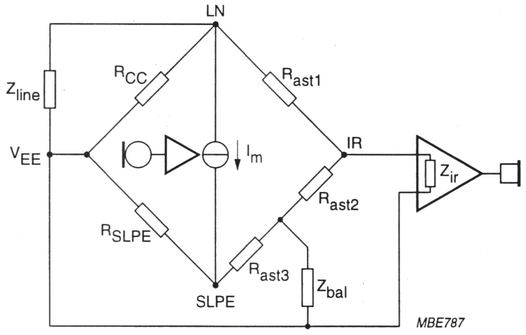

LN
Z_{line}
R_{CC}
R_{ast1}
IR
V_{EE}
I_m
Z_{ir}
R_{ast2}
R_{SLPE}
R_{ast3}
Z_{bal}
SLPE
MBE787

Fig.12 Equivalent circuit of TEA1118 and TEA1118A family anti-sidetone bridge.

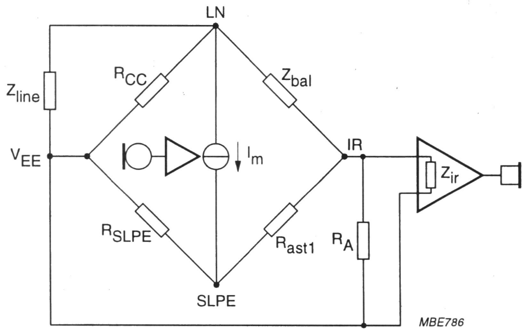

LN
Z_{line}
R_{CC}
Z_{bal}
IR
V_{EE}
I_m
Z_{ir}
R_{SLPE}
R_{ast1}
R_A
SLPE
MBE786

Fig.13 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

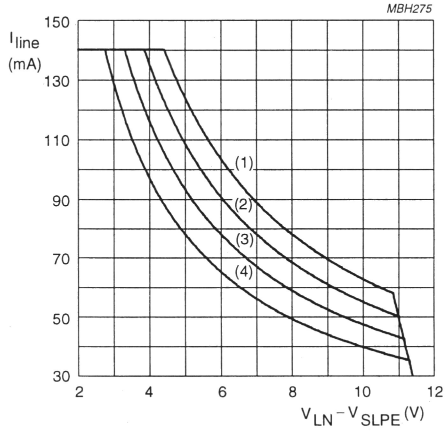
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		$V_{EE} - 0.4$	12	V
	repetitive line voltage during switch-on or line interruption		$V_{EE} - 0.4$	13.2	V
$V_{n(max)}$	maximum voltage on all pins		$V_{EE} - 0.4$	$V_{CC} + 0.4$	V
I_{line}	line current	$R_{SLPE} = 20\ \Omega$; see Figs 14 and 15	–	140	mA
P_{tot}	total power dissipation	$T_{amb} = 75$ °C; see Figs 14 and 15			
	TEA1118T; TEA1118AT		–	393	mW
	TEA1118M; TEA1118AM		–	317	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

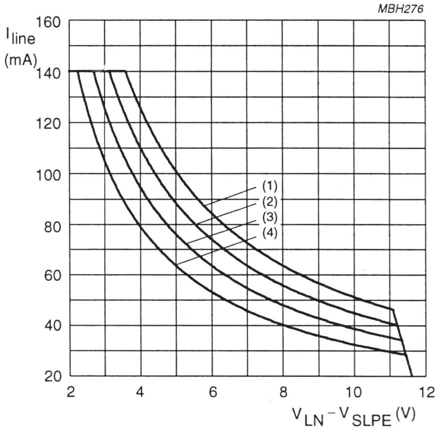
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air			
	TEA1118T; TEA1118AT		130	K/W
	TEA1118M; TEA1118AM	mounted on epoxy board 40.1 × 19.1 × 1.5 mm	160	K/W



(1) $T_{amb} = 45$ °C; $P_{tot} = 624$ mW.
(2) $T_{amb} = 55$ °C; $P_{tot} = 546$ mW.
(3) $T_{amb} = 65$ °C; $P_{tot} = 470$ mW.
(4) $T_{amb} = 75$ °C; $P_{tot} = 393$ mW.

Fig.14 SO14 safe operating area.



(1) $T_{amb} = 45$ °C; $P_{tot} = 503$ mW.
(2) $T_{amb} = 55$ °C; $P_{tot} = 441$ mW.
(3) $T_{amb} = 65$ °C; $P_{tot} = 379$ mW.
(4) $T_{amb} = 75$ °C; $P_{tot} = 317$ mW.

Fig.15 SSOP16 safe operating area.

CHARACTERISTICS

I_{line} = 15 mA; V_{EE} = 0 V; R_{SLPE} = 20 Ω; AGC pin connected to V_{EE}; Z_{line} = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{LN}, V_{CC}, SLPE and REG)						
V_{ref}	stabilized voltage between LN and SLPE	I_{line} = 15 mA	3.1	3.35	3.6	V
V_{LN}	DC line voltage	I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	2.45	–	V
		I_{line} = 15 mA	3.35	3.65	3.95	V
		I_{line} = 140 mA	–	–	6.9	V
$V_{LN(exR)}$	DC line voltage with an external resistor R_{VA}	I_{line} = 15 mA; $R_{VA(SLPE-REG)}$ = 27 kΩ	–	4.4	–	V
$\Delta V_{LN}/T$	DC line voltage variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = −25 to +75 °C	–	±30	–	mV
I_{CC}	internal current consumption	V_{CC} = 2.9 V	–	1.15	1.4	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; I_P = 0 mA	–	2.9	–	V
R_{CCint}	equivalent supply voltage resistance	I_{line} = 15 mA; I_P = 0.5 mA	–	550	620	Ω
Transmit amplifier (pins TX+, TX− and GAT)						
$\lvert Z_i \rvert$	input impedance					
	differential between pins TX+ and TX−		–	64	–	kΩ
	single-ended between pins TX+/TX− and V_{EE}		–	32	–	kΩ
G_{vtx}	voltage gain from TX+/TX− to LN	I_{line} = 15 mA; V_{TX} = 200 mV (RMS)	tbf	11	tbf	dB
ΔG_{vtxf}	gain variation with frequency referred to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx}T$	gain variation with temperature referred to 25 °C	I_{line} = 15 mA; T_{amb} = −25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	80	–	dB
ΔG_{vtxr}	gain voltage reduction range (TEA1118 only)	external resistor connected between GAT and REG	–	–	tbf	dB
$V_{LN(max)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.4	1.7	–	V
		I_{line} = 4 mA; THD = 10%	–	0.8	–	V
$V_{TX(max)}$	maximum transmit input voltage (RMS value)	I_{line} = 15 mA; THD = 2%	–	0.45	–	V
		I_{line} = 75 mA; THD = 2%	–	0.9	–	V
V_{notx}	noise output voltage at pin LN; pins TX+/TX− shorted through 200 Ω	psophometrically weighted (P53 curve)	–	−84	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmit mute (pin TMUTE; TEA1118A only)						
ΔG_{vtxm}	gain reduction	TMUTE = HIGH	–	80	–	dB
V_{IL}	LOW level input voltage		$V_{EE} - 0.4$	–	$V_{EE} + 0.3$	V
V_{IH}	HIGH level input voltage		$V_{EE} + 1.5$	–	$V_{CC} + 0.4$	V
I_{TMUTE}	input current	input level = HIGH	–	1.25	3	μA
Receive amplifier (pins IR, QR and GAR)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vrx}	voltage gain from IR to QR	I_{line} = 15 mA; V_{IR} = 6 mV (RMS)	30	31	32	dB
ΔG_{vrxf}	gain variation with frequency referenced to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vrx}T$	gain variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = –25 to +75 °C	–	±0.3	–	dB
ΔG_{vrxr}	gain voltage reduction range	external resistor connected between GAR and QR	–	–	12	dB
$V_{o(rms)}$	maximum receive signal (RMS value)	I_{line} = 15 mA; I_P = 0 mA sine wave drive; R_L = 150 Ω; THD = 2%	–	0.25	–	V
		I_{line} = 15 mA; I_P = 0 mA sine wave drive; R_L = 450 Ω; THD = 2%	–	0.35	–	V
$V_{norx(rms)}$	noise output voltage at pin QR (RMS value)	I_{line} = 15 mA; IR open-circuit; R_L = 150 Ω; psophometrically weighted (P53 curve)	–	50	–	μV
Automatic gain control (pin AGC)						
ΔG_{vtrx}	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 85 mA; AGC pin connected to V_{EE}	–	5.8	–	dB
I_{start}	highest line current for maximum gain	AGC pin connected to V_{EE}	–	26	–	mA
I_{stop}	lowest line current for minimum gain	AGC pin connected to V_{EE}	–	61	–	mA
DTMF amplifier (pin DTMF; TEA1118A only)						
$\lvert Z_i \rvert$	input impedance		–	20	–	kΩ
G_{vtx}	voltage gain from DTMF to LN	I_{line} = 15 mA; V_{DTMF} = 100 mV (RMS); MUTE or TMUTE = HIGH	tbf	17	tbf	dB
ΔG_{vtxf}	gain variation with frequency referenced to 1 kHz	I_{line} = 15 mA; f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{vtx}T$	gain variation with temperature referenced to 25 °C	I_{line} = 15 mA; T_{amb} = –25 to + 75 °C	–	±0.4	–	dB
G_{vrx}	voltage gain from DTMF to QR (confidence tone)	I_{line} = 15 mA; V_{DTMF} = 100 mV (RMS); R_L = 150 Ω	–	–18	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mute function (pin MUTE; TEA1118A only)						
V_{IL}	LOW level input voltage		$V_{EE} - 0.4$	–	$V_{EE} + 0.3$	V
V_{IH}	HIGH level input voltage		$V_{EE} + 1.5$	–	$V_{CC} + 0.4$	V
I_{MUTE}	input current	input level = HIGH	–	1.25	3	μA
ΔG_{trxm}	gain reduction for transmit and receive amplifiers	MUTE = HIGH	–	80	–	dB

APPLICATION INFORMATION

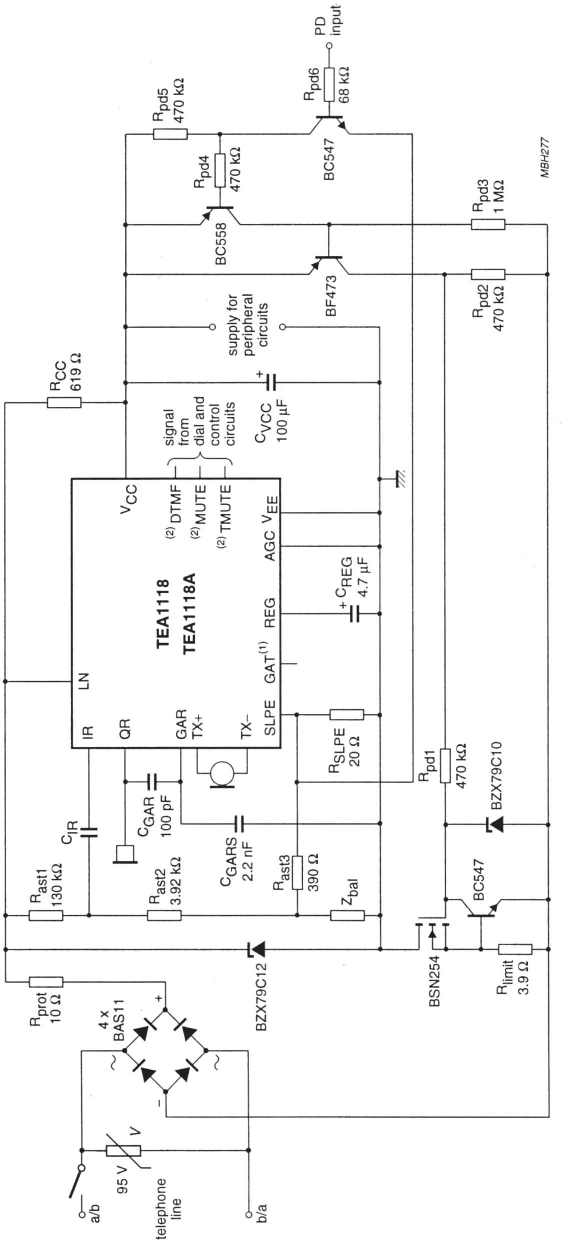

PD input
R_{pd6} 68 kΩ
R_{pd5} 470 kΩ
BC547
MBH277
R_{pd4} 470 kΩ
BC558
R_{pd3} 1 MΩ
BF473
R_{pd2} 470 kΩ
supply for peripheral circuits
R_{CC} 619 Ω
C_{VCC} 100 µF
signal from dial and control circuits
V_{CC}
(2) DTMF
(2) MUTE
(2) TMUTE
V_{EE}
AGC
REG
$GAT^{(1)}$
SLPE
LN
IR
QR
GAR
TX+
TX−
TEA1118
TEA1118A
C_{REG} 4.7 µF
R_{SLPE} 20 Ω
R_{pd1} 470 kΩ
BZX79C10
C_{IR}
C_{GAR} 100 pF
C_{GARS} 2.2 nF
R_{ast1} 130 kΩ
R_{ast2} 3.92 kΩ
R_{ast3} 390 Ω
Z_{bal}
BC547
BSN254
R_{limit} 3.9 Ω
BZX79C12
R_{prot} 10 Ω
4 x BAS11
95 V
V
a/b
telephone line
b/a

Fig.16 Typical application of the TEA1118 and TEA1118A in sets with pulse dialling or flash facilities.

(1) TEA1118 only.
(2) TEA1118A only.

Line interrupter driver and ringer UBA1702; UBA1702A

FEATURES

Speech part

- Driver for the line interrupter that can be either a PMOST when UBA1702 is used or a PNP when UBA1702A is used
- Adjustable over-current protection
- Adjustable over-voltage protection for transmission circuit
- Adjustable mute (dialling mode voltage; DMO or NSA)
- Adjustable current loop detection (hook switch status)
- Microcontroller supply
- Provision for electronic hook switch.

Ringer part

- Over-voltage protection
- Ringer frequency output for frequency discrimination
- Adjustable ringer threshold for piezo-driver enable
- Three bits ringer volume control
- Bridge-tied-load (BTL) output stage for piezo transducer
- Fast start-up microcontroller supply.

Miscellaneous

- Separated ground pins for transmission circuit interface and control signals (e.g. for TEA1064A)
- Possibility to supply the microcontroller with an external voltage source.

APPLICATIONS

- Telephone sets with software controlled ringer function
- Telephone sets with electronic hook switch.

GENERAL DESCRIPTION

The UBA1702; UBA1702A performs the high voltage interface and ringer functions of the corded analog telephone set in close cooperation with a microcontroller and transmission circuit.

The UBA1702; UBA1702A incorporates several protections, a driver for the line interrupter and a ringer. Because of the practical division of functions between the microcontroller, the transmission circuit and the UBA1702; UBA1702A, it is possible to have a higher integration level thereby reducing significantly the number of discrete components in a telephone set.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1702	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
UBA1702A	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
UBA1702T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UBA1702AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

Speech part: I_{line} = 20 mA; DPI = LOW; T_{amb} = 25 °C; V_{EE} = 0 V; unless otherwise specified.
Ringer part: $V_{line(rms)}$ = 45 V; f = 25 Hz; using an RC combination of 2.2 kΩ and 820 nF and a diode bridge between the line and the RPI input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Speech part						
SWITCH DRIVER AND REFERENCES (PINS SDI, SDO, EHI AND DPI); UBA1702A ONLY						
R_{SDO}	resistance between pins SDO and V_{EE}		–	2.2	–	kΩ
SWITCH DRIVER AND REFERENCES (PINS SDI, SDO, EHI AND DPI); UBA1702 AND UBA1702A						
$R_{SDI-SDO}$	resistance between pins SDI and SDO	V_{SDI} - V_{SDO} < 12 V	–	1.1	–	MΩ
R_{SDI}	resistance between pins SDI and V_{EE}	V_{SDI} = 240 V; DPI = HIGH	5	–	–	MΩ
MUTE SWITCH AND ADJUSTABLE PROTECTION ZENER VOLTAGE (PINS MSI, MSA AND ZPA)						
$V_{SPO(M)}$	adjustable mute voltage referenced to V_{EE}	MSI = HIGH; MSA open-circuit	–	2.7	3	V
$V_{SPO(Z)}$	adjustable zener voltage referenced to V_{EE}	MSI = LOW; ZPA open-circuit	11	12	13	V
CURRENT MANAGEMENT (PINS SPI, SPO, CDA, CLA AND CDO)						
$I_{SPI(lim)}$	current limitation (pin SPI)	CLA shorted to V_{EE}	–	120	–	mA
$I_{SPI(det)}$	current detection (pin SPI)	CDA open-circuit	2	3	4	mA
MICROCONTROLLER SUPPLY (V_{DD} AND V_{BB})						
V_{DD}	supply output voltage referenced to V_{SS}	V_{BB} > 3.7 V; I_{DD} = −1 mA	3.0	3.3	3.6	V
Ringer part						
PROTECTION (PIN RPI)						
$I_{RPI(max)}$	maximum input current		70	–	–	mA
RINGER THRESHOLD AND FREQUENCY DETECTION (PINS V_{RR}, RTA AND RFO)						
$V_{RR(th)}$	ringer supply threshold voltage referenced to V_{SS}	RTA open-circuit	–	11	–	V
VOLUME CONTROL (PINS RV0, RV1 AND RV2)						
ΔG_s	step resolution	(RV2, RV1, RV0) from (0, 0, 0) to (1, 1, 0); note 1	–	6	–	dB
ΔG_{ls}	last step resolution	(RV2, RV1, RV0) from (1, 1, 0) to (1, 1, 1); note 2	–	9.5	12	dB
RINGER MELODY INPUT AND PIEZO DRIVER (PINS RMI, ROA AND ROB)						
$V_{o(max\ p-p)}$	maximum output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 1; RV1 = 1; RV0 = 1	–	28.7	32	V

Notes

1. Independent of V_{RR} if greater than 10 V.
2. Without piezo transducer, dependent on V_{RR}.

BLOCK DIAGRAM

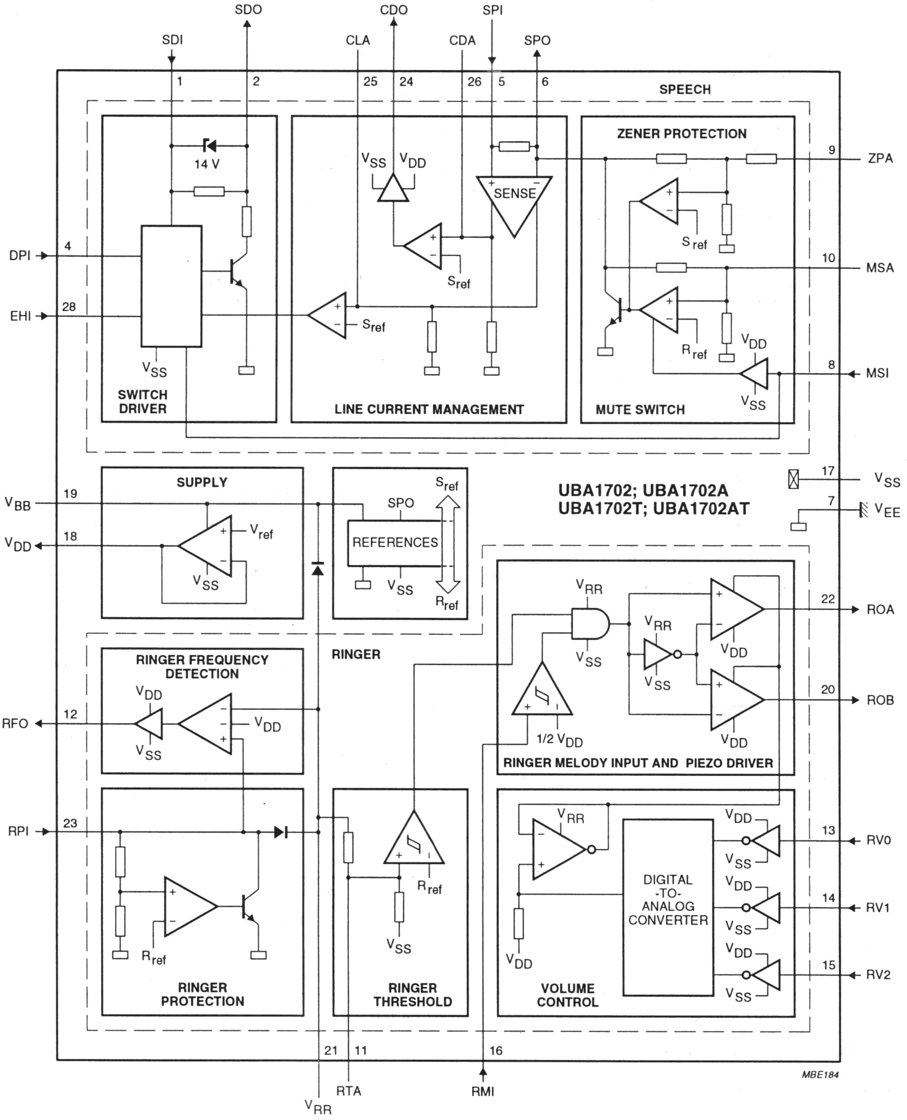

SDO
CDO
SPI
SDI
CLA
CDA
SPO
1
2
25
24
26
5
6
SPEECH
14 V
VSS
VDD
SENSE
ZENER PROTECTION
9
ZPA
S ref
10
MSA
DPI
4
Sref
EHI
28
Sref
Rref
VDD
8
MSI
VSS
VSS
SWITCH DRIVER
LINE CURRENT MANAGEMENT
MUTE SWITCH
SUPPLY
Sref
SPO
17
VSS
UBA1702; UBA1702A
UBA1702T; UBA1702AT
VBB
19
7
VEE
Vref
REFERENCES
VDD
18
VSS
VSS
Rref
VRR
VRR
VSS
22
ROA
VDD
RINGER
RINGER FREQUENCY DETECTION
VDD
VSS
20
ROB
RFO
12
VDD
VSS
1/2 VDD
VDD
RINGER MELODY INPUT AND PIEZO DRIVER
VRR
VDD
RPI
23
13
RV0
Rref
VSS
DIGITAL -TO- ANALOG CONVERTER
VDD
14
RV1
VSS
VSS
VDD
VDD
15
RV2
Rref
VSS
RINGER PROTECTION
RINGER THRESHOLD
VOLUME CONTROL
21
11
16
MBE184
RTA
RMI
VRR

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDI	1	switch driver input
SDO	2	switch driver output
n.c.	3	not connected
DPI	4	dialling pulse input
SPI	5	speech part input
SPO	6	speech part output
V_{EE}	7	ground for transmission circuit
MSI	8	mute switch input
ZPA	9	Zener protection adjustment input
MSA	10	mute switch adjustment input
RTA	11	ringer threshold adjustment input
RFO	12	ringer frequency output
RV0	13	ringer volume input; bit 0
RV1	14	ringer volume input; bit 1
RV2	15	ringer volume input; bit 2
RMI	16	ringer melody input
V_{SS}	17	ground for microcontroller and ringer
V_{DD}	18	microcontroller supply voltage
V_{BB}	19	supply voltage from transmission circuit
ROB	20	ringer output B
V_{RR}	21	ringer supply voltage
ROA	22	ringer output A
RPI	23	ringer part input
CDO	24	current detection output
CLA	25	current limitation adjustment input
CDA	26	current detection adjustment input
n.c.	27	not connected
EHI	28	electronic hook switch input

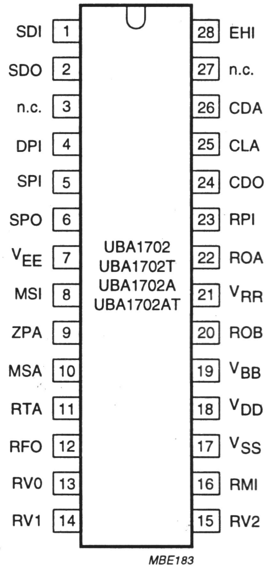

SDI 1
SDO 2
n.c. 3
DPI 4
SPI 5
SPO 6
VEE 7
MSI 8
ZPA 9
MSA 10
RTA 11
RFO 12
RV0 13
RV1 14
28 EHI
27 n.c.
26 CDA
25 CLA
24 CDO
23 RPI
22 ROA
21 VRR
20 ROB
19 VBB
18 VDD
17 VSS
16 RMI
15 RV2
UBA1702
UBA1702T
UBA1702A
UBA1702AT
MBE183

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The values given in this functional description are typical values except when otherwise specified.

Speech part

The speech part consists of three blocks, the switch driver, the line current management and the mute switch (DMO or NSA) combined with an adjustable over-voltage (zener) protection circuit. The reference block, which generates reference voltages and currents, is also used in the speech part (see Fig.1) by the mute switch block.

SWITCH DRIVER (PINS SDI, SDO, EHI AND DPI)

UBA1702

The UBA1702 switch driver block is intended to generate the appropriate signal to drive an external PMOST interrupter. The source and gate of this PMOST are respectively connected to SDI and SDO. The electronic hook switch input (EHI) and the dialling pulse input (DPI) signals control the state of this PMOST.

The EHI pin is provided with high voltage capability. When the voltage applied at pin EHI is HIGH, the switch driver block will start and generate the proper signals to switch on the external PMOST interrupter.

When the telephone set is equipped with a mechanical hook switch, pin EHI can be connected directly to the switch driver input (pin SDI). For electronic hook switch applications, the EHI pin can be driven by the microcontroller output.

In some special applications, the EHI pin can be current driven. In such a case, the current available at SDO to turn on the PMOST interrupter is approximately 10 times the EHI input current (providing $I_{EHI} < 2$ μA).

The EHI pin presents an impedance of 250 kΩ at low input voltage. When the applied voltage at EHI goes above approximately 30 V, the EHI input current remains constant (see Fig.3) so that the EHI impedance increases.

The DPI is designed to switch on or off the external PMOST interrupter (providing EHI is HIGH). When the voltage applied at pin DPI is HIGH, the switch driver block turns off the external PMOST interrupter. When the voltage applied at pin DPI is LOW, the switch driver block turns on the external PMOST interrupter.

The external PMOST interrupter is controlled by the voltage between the switch driver input and output (pins SDI and SDO).

When the voltage applied at pin EHI is HIGH and the voltage applied at pin DPI is LOW, the voltage at SDO is pulled down to a value less than 0.2 V in order to create a high source-gate voltage (V_{SG}) for the external PMOST. However, in order to avoid break-down of the external PMOST, the voltage difference between SDI and SDO is internally limited to 14 V.

When the voltage applied at pin EHI and the one applied at pin DPI are both HIGH, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes very high (a few MΩ).

When the voltage applied at pin EHI is LOW, whatever the one applied at DPI is, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes almost infinite.

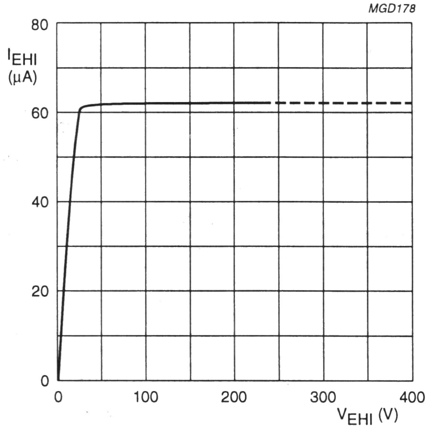


Fig.3 EHI input characteristics.

UBA1702A

The UBA1702A switch driver block is intended to generate the appropriate signal to drive an external PNP interrupter. The emitter and base of this PNP are respectively connected to SDI and SDO. The EHI and DPI signals control the state of this PNP.

The EHI pin is provided with high voltage capability. When the voltage applied at pin EHI is HIGH, the switch driver block will start and generate the appropriate signals to switch on the external PNP interrupter.

When the telephone set is equipped with a mechanical hook switch, pin EHI can be connected directly to pin SDI. For electronic hook switch applications, the EHI pin can be driven by the microcontroller output.

The EHI pin presents an impedance of 250 kΩ at low input voltage. When the applied voltage at EHI goes above approximately 30 V, the EHI input current remains constant (see Fig.3) so that the EHI impedance increases.

The DPI is designed to switch on or off the external PNP interrupter (providing EHI is HIGH). When the voltage applied at pin DPI is HIGH, the switch driver block turns off the external PNP interrupter. When the voltage applied at pin DPI is LOW, the switch driver block turns on the external PNP interrupter.

The external PNP interrupter is controlled by the current flowing into pin SDO.

When the voltage applied at pin EHI is HIGH and the voltage applied at pin DPI is LOW, pin SDO can be considered as being connected to pin V_{EE} via a 2.2 kΩ resistor in order to create a base current for the external PNP.

When the voltage applied at pin EHI and the one applied at pin DPI are both HIGH, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes very high (a few MΩ).

When the voltage applied at pin EHI is LOW, whatever the one applied at DPI is, pin SDO can be considered as being connected to pin SDI via a 1.1 MΩ pull-up resistor while the impedance between SDI and V_{EE} becomes almost infinite.

LINE CURRENT MANAGEMENT (PINS SPI, SPO, CDA, CLA AND CDO)

The line current is measured by an internal 2 Ω resistor and a sense circuit connected between the speech part input and output (pins SPI and SPO). The circuit delivers information about the hook switch status at the current detection output (pin CDO) and controls the line current limitation.

When the SPI current exceeds a certain level (3 mA), the sense circuit injects some image of the SPI current into an internal resistor (see Fig.1). The created voltage becomes higher than an internal reference (approximately 0.3 V) and CDO goes HIGH. This current detection level can be increased by connecting a resistor between pins CDA (current detection adjustment) and V_{EE}. It is also possible to connect a capacitor between pins CDA and V_{EE} to filter unwanted AC components of the line current signal. Line current interruption during pulse dialling influences the CDO output.

When the SPI current exceeds another current level (45 mA), the sense circuit injects some image of the SPI current into an internal resistor (see Fig.1). The created voltage becomes higher than an internal reference (approximately 0.4 V) and an internal signal is generated in order to limit the current in the external interrupter thus resulting in a line current limitation. This line current limitation level can be increased up to a maximum value of 120 mA by connecting a resistor between pins CLA (current limitation adjustment) and V_{EE}.

When a PMOST (UBA1702) is used as an interrupter, the SPI current equals the drain or source current of the PMOST and thus also equals the line current.

When a PNP (UBA1702A) is used as an interrupter, the SPI current equals the collector current of the PNP and thus differs from the line current (the PNP base current does not flow into the SPI pin).

MUTE SWITCH AND ZENER PROTECTION (PINS MSI, MSA AND ZPA)

The mute switch is, in fact, a switchable and electronic zener diode connected between the speech part output (pin SPO) and V_{EE}.

When the voltage applied at the mute switch input (pin MSI) is LOW, the switch is in over-voltage protection mode and the maximum SPO voltage is limited to 12 V. This level can be increased or decreased by connecting a resistor between pins ZPA (zener protection adjustment) and V_{EE} or ZPA and SPO respectively.

When the voltage applied at pin MSI is HIGH, the switch is in mute mode (DMO or NSA) resulting in a SPO voltage below 3 V. This level can be decreased by connecting a resistor between pins MSA (mute switch adjustment) and SPO. It should be noted that the mute switch stage is supplied from V_{DD} thus a minimum voltage of approximately 2.1 V is required on V_{DD}.

REFERENCE

The bias currents and voltages for the various speech blocks are generated by the reference block which is, in most cases, supplied from pin SPO. This block guarantees a high AC impedance at the SPO pin operating down to a low SPO voltage. Therefore, most speech part blocks operate independently from V_{DD}.

Ringer part

The ringer part consists of five blocks, the ringer protection, the ringer threshold, the ringer frequency detection, the volume control and the piezo driver. The reference block which generates reference voltages and currents is also used in the ringer part (see Fig.1).

RINGER PROTECTION (PINS RPI AND V_{RR})

The ringer protection block converts the ringing current into a limited voltage between the ringer part input (pin RPI) and V_{EE}. This voltage is used (via an internal diode) to generate the ringer supply voltage V_{RR} which is mainly used for all ringer parts. The voltage at pin V_{RR} must be filtered with a 22 μF capacitor connected between pins V_{RR} and V_{SS}.

In electronic hook switch applications and also in speech mode (see Fig.8), pin RPI is always connected to the telephone line (through a series RC network and a diode bridge). In order not to disturb normal speech operation, a high AC impedance is present at pin RPI (providing the speech level is less than 1.5 V (RMS) i.e. 5.7 dBm).

In the DMO or NSA mode (i.e. MSI is HIGH), the voltage across RPI and V_{EE} is limited to 2.1 V. With this feature and in electronic hook switch applications, several additional ringers can be placed in parallel without tinkling during pulse dialling phase.

RINGER THRESHOLD (PIN RTA)

The piezo driver is internally enabled when the voltage at pin V_{RR} exceeds a threshold level of 11 V. This threshold level can be increased or decreased by connecting a resistor between pins RTA (ringer threshold adjustment) and V_{SS} or RTA and V_{RR} respectively.

Because of the built-in 6.5 V hysteresis, a voltage change at pin V_{RR} (coming from current consumption increase when the piezo output is driven with a melody) will have no influence on this internal enabling signal.

RINGER FREQUENCY DETECTION (PIN RFO)

The ringer frequency detection block generates a square wave signal at the ringer frequency output (pin RFO) with twice the ringer signal frequency. This RFO signal can be used by the microcontroller for frequency discrimination.

When the voltage at pin RPI drops below the voltage at pin V_{DD}, RFO goes LOW. Pin RFO goes HIGH when the voltage at pin RPI exceeds the voltage at pin V_{RR}.
This $V_{RR} - V_{DD}$ hysteresis allows the frequency detection circuit to ignore parasitic signals superimposed on the ringing signal.

VOLUME CONTROL (PINS RV0, RV1 AND RV2)

The volume control input has three bits RV2, RV1 and RV0 to realize eight volume levels. The volume is controlled by regulating the supply voltage of the piezo output stage. The first six steps have a fixed value of 6 dB, the value of the last step (maximum volume) is dependent on the available voltage at pin V_{RR}.

Default setting during start-up is (RV2 = 0, RV1 = 0, RV0 = 0) which corresponds to minimum volume. In order not to damage the piezo transducer, the differential output ROA – ROB is internally limited to a value less than 32 V (p-p).

RINGER MELODY INPUT AND PIEZO DRIVER (PINS RMI, ROA AND ROB)

The input signal at the ringer melody input (pin RMI) may be a square wave or a sine wave which is generated by the microcontroller. The input stage incorporates a small hysteresis (between $0.49V_{DD}$ and $0.51V_{DD}$) and is referenced to $\frac{1}{2}V_{DD}$ which is also the DC level of the signal coming from the microcontroller. Nevertheless, when a sine wave is used, a coupling capacitor of 10 nF (connected between pin RMI and the output of the microcontroller) is required. This 10 nF capacitor value is enough since the RMI input impedance is approximately 250 kΩ.

The piezo driver is an output stage for a piezo transducer which has to be connected between ringer output A and ringer output B (pins ROA and ROB) as a Bridged Tied Load (BTL) or between ROA and V_{SS} as a Single-Ended Load (SEL). The ROA and ROB output signals are square wave and in opposite phase driven by the ringer melody input stage. The minimum output current capability of the ROA and ROB outputs is greater than 80 mA at maximum volume setting (RV2 = 1, RV1 = 1, RV0 = 1) and becomes even greater during output switching. This gives fast rise and fall times resulting in a lot of harmonics.

To obtain maximum efficiency, the piezo driver stage is supplied in series with the V_{DD} supply.

REFERENCE

The bias current for the various ringer blocks is generated by the reference block while this block is supplied from pin V_{RR} or V_{DD}.

Supply part (pins V_{BB} and V_{DD})

The supply block regulates the voltage at pin V_{DD}, referenced to V_{SS}, to a typical value of 3.3 V and can deliver a minimum of 2 mA. This is sufficient to supply most normal microcontrollers. The voltage at pin V_{DD} must be filtered with a 22 µF capacitor connected between pins V_{DD} and V_{SS}.

In speech mode, this block is supplied from the transmission circuit using pin V_{BB}. The voltage drop between V_{BB} and V_{DD} has been minimized (100 mV at 1 mA, providing $2.5\ V < V_{BB} < 3.0\ V$) in order to allow low voltage operation of the transmission circuit.

In ringer mode, this block is supplied from the ringer part using pin V_{RR} and pin V_{BB} which are tied together through an internal diode (see Fig.1).

When an external (mains or battery) supply is connected to V_{BB} and no speech or ringer signal is applied, V_{DD} (3.3 V) is still present.

During on-hook phase, and when a small current is derived from the line to the microcontroller supply, the circuit stays in a kind of stand-by mode to provide sufficient voltage at pin V_{DD}. This is done to ensure memory retention in the microcontroller.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SDI}, V_{SDO}	maximum input/output switch driver voltage (pins SDI or SDO)	DC; note 1	–	240	V
		pulsed; note 2	–	400	V
V_{EHI}	maximum hook switch input voltage (pin EHI)	DC; note 1	–	240	V
		pulsed; note 2	–	400	V
$V_{i(max)}$	maximum voltage at all logic inputs (pins DPI, MSI, RV0, RV1, RV2 and RMI)		$V_{SS} - 0.4$	$V_{DD} + 0.4$	V
$V_{n(max)}$	maximum voltage at all other pins		–	24	V
$I_{SPI(max)}$	maximum speech part input current (pin SPI)		–	150	mA
$I_{RPI(max)}$	maximum ringer part input current (pin RPI)		–	70	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C			
	UBA1702		–	1	W
	UBA1702T		–	0.625	W
T_{stg}	IC storage temperature		–40	+150	°C
T_{amb}	operating ambient temperature		–25	+75	°C

Notes

1. Continuous.
2. 2 kV surge:
   a) according to IEC 805-1 part 5. Test generator 10 μs/700 μs according to CCITT (Rm1 = 15 Ω and Rm2 = 25 Ω).
   b) pulse sequence > 60 s
   c) number of surges: 10
   d) polarity change after 5 surges
   e) test circuit in combination with 150 V Voltage Dependent Resistor (VDR) and a 3.9 Ω resistor connected in series with the source of the PMOST interrupter (UBA1702).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	UBA1702, UBA1702A	45	K/W
	UBA1702T, UBA1702AT	70	K/W

CHARACTERISTICS

Speech part: I_{line} = 20 mA; DPI = LOW; T_{amb} = 25 °C; V_{EE} = 0 V; unless otherwise specified.
Ringer part: $V_{line(rms)}$ = 45 V; f = 25 Hz; using an RC combination of 2.2 kΩ and 820 nF and a diode bridge between the line and the RPI input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Speech Part						
Switch driver and references (pins SDI, SDO, EHI and DPI); UBA1702 only						
I_{EE}	V_{EE} current consumption	V_{SPO} = 4.2 V	–	–330	–	μA
V_{SDO}	switch driver output voltage	V_{SDI} < 12 V	–	–	0.2	V
Switch driver and references (pins SDI, SDO, EHI and DPI); UBA1702A only						
I_{EE}	V_{EE} current consumption; excluding PNP interrupter base current	V_{SDO} = 4.2 V	–	–510	–	μA
R_{SDO}	resistance between pins SDO and V_{EE}		–	2.2	–	kΩ
$I_{SDO(max)}$	maximum input current (pin SDO)		7.5	–	–	mA
Switch driver and references (pins SDI, SDO, EHI and DPI); UBA1702 and UBA1702A						
I_{SS}	V_{SS} current consumption	V_{SPO} = 4.2 V; note 1	–	–280	–	μA
$V_{SDI-SDO}$	internal voltage limitation between pins SDI and SDO		–	14	–	V
$R_{SDI\text{-}SDO}$	resistance between pins SDI and SDO	$V_{SDI} - V_{SDO}$ < 12 V	–	1.1	–	MΩ
R_{SDI}	resistance between pins SDI and V_{EE}	$V_{SDI} = V_{EHI}$ = 48 V; DPI = HIGH	–	4	–	MΩ
		$V_{SDI} = V_{EHI}$ = 240 V; DPI = HIGH	5	20	–	MΩ
R_{EHI}	resistance between pins EHI and V_{EE}	V_{EHI} = 4.2 V	100	250	–	kΩ
		V_{EHI} = 48 V	–	740	–	kΩ
		V_{EHI} = 240 V	–	3.5	–	MΩ
$\lvert Z_{SPO} \rvert$	impedance between pins SPO and V_{EE}	f = 0.3 to 3.4 kHz	20	–	–	kΩ
$\lvert Z_{VSS} \rvert$	impedance between pins V_{SS} and V_{EE}	f = 0.3 to 3.4 kHz	10	–	–	kΩ
V_{IH}	HIGH level input voltage (pin EHI)		V_{SS} + 1.5	–	240	V
V_{IL}	LOW level input voltage (pin EHI)		V_{SS}	–	V_{SS} + 0.3	V
I_{IH}	HIGH level input current (pin EHI)	V_{EHI} = 4.2 V	0	10	20	μA
I_{IL}	LOW level input current (pin EHI)	V_{EHI} = LOW	–	0	–	μA
V_{IH}	HIGH level input voltage (pin DPI)		V_{SS} + 1.5	–	V_{DD}	V
V_{IL}	LOW level input voltage (pin DPI)		V_{SS}	–	V_{SS} + 0.3	V
I_{IH}	HIGH level input current (pin DPI)	V_{DPI} = HIGH	0	–	10	μA
I_{IL}	LOW level input current (pin DPI)	V_{DPI} = LOW	–	0	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE SWITCH AND ZENER PROTECTION (PINS MSI, MSA AND ZPA)						
$V_{SPO(M)}$	adjustable mute voltage referenced to V_{EE}	MSI = HIGH; MSA open-circuit	–	2.7	3	V
		MSI = HIGH; MSA shorted to SPO	–	1.7	–	V
$V_{SPO(Z)}$	adjustable zener voltage referenced to V_{EE}	MSI = LOW; ZPA open-circuit	11.0	12.0	13.0	V
		MSI = LOW; ZPA shorted to SPO	8.3	9.0	9.7	V
		MSI = LOW; ZPA shorted to V_{EE}	16.4	18.0	19.6	V
I_{SPI}	current capability (pin SPI)		150	–	–	mA
V_{IH}	HIGH level input voltage (pin MSI)		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage (pin MSI)		V_{SS}	–	$V_{SS} + 0.3$	V
I_{IH}	HIGH level input current (pin MSI)	V_{MSI} = HIGH	0	–	10	μA
I_{IL}	LOW level input current (pin MSI)	V_{MSI} = LOW	–	0	–	μA
CURRENT MANAGEMENT (PINS SPI, SPO, CDA, CLA AND CDO)						
$I_{SPI(lim)}$	current limitation (pin SPI)	CLA open-circuit	–	45	–	mA
		CLA shorted to V_{EE}	–	120	–	mA
$I_{SPI(det)}$	current detection (pin SPI)	CDA open-circuit	2	3	4	mA
$R_{SPI\text{-}SPO}$	series resistance between pins SPI and SPO		–	2	–	Ω
I_{OH}	HIGH level output current (pin CDO)	$V_{CDO} = V_{DD} - 0.5$ V	–	–	−100	μA
I_{OL}	LOW level output current (pin CDO)	$V_{CDO} = V_{SS} + 0.5$ V	100	–	–	μA
MICROCONTROLLER SUPPLY (PINS V_{DD} AND V_{BB})						
V_{DD}	supply output voltage referenced to V_{SS}	$V_{BB} > 3.7$ V; $I_{DD} = -1$ mA	3.0	3.3	3.6	V
$\Delta V_{DD}/\Delta T$	supply output voltage temperature gradient		–	−0.2	–	mV/K
I_{DD}	supply output current capability	$V_{BB} > 3.7$ V	–	–	−2	mA
$V_{BB}-V_{DD}$	voltage drop between V_{BB} and V_{DD}	$I_{DD} = -1$ mA; $2.5\ \text{V} < V_{BB} < 3.0\ \text{V}$	–	100	–	mV
V_{DDM}	voltage at pin V_{DD} when neither speech nor ringer signal is applied	$I_{DD} = 9$ μA	–	1.4	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ringer part						
PROTECTION (PIN RPI)						
I_{SS}	current consumption	RV2 = 0; RV1 = 0; RV0 = 0	–	–850	–	µA
$I_{RPI(max)}$	maximum input current		70	–	–	mA
V_{RPI}	voltage limit referenced to V_{EE}		–	21	–	V
V_{RPId}	voltage limit in DMO or NSA mode referenced to V_{EE}	I_{RPI} = 30 mA; MSI = HIGH	–	2.1	–	V
$\lvert Z_{RPI} \rvert$	AC input impedance referenced to V_{EE}	f = 0.3 to 3.4 kHz; V_{RPI} < 1.5 V (RMS)	100	220	–	kΩ
RINGER THRESHOLD AND FREQUENCY DETECTION (PINS V_{RR}, RTA AND RFO)						
V_{RRth}	ringer supply threshold voltage referenced to V_{SS}	RTA open-circuit;	–	11	–	V
V_{RRhys}	ringer threshold hysteresis voltage		–	6.5	–	V
V_{RPIhys}	ringer frequency detection hysteresis voltage referenced to V_{EE}	RFO = HIGH	–	V_{RR}	–	V
		RFO = LOW	–	V_{DD}	–	V
I_{OH}	HIGH level output current (pin RFO)	$V_{RFO} = V_{DD} - 0.5$ V	–	–	–100	µA
I_{OL}	LOW level output current (pin RFO)	$V_{RFO} = V_{SS} + 0.5$ V	100	–	–	µA
VOLUME CONTROL (PINS RV0, RV1 AND RV2)						
ΔG	gain adjustment range	(RV2, RV1, RV0) from (0, 0, 0) to (1 ,1, 0); note 2	–	36	–	dB
ΔG_s	step resolution	(RV2, RV1, RV0) from (0, 0, 0) to (1, 1, 0); note 2	–	6	–	dB
ΔG_{ls}	last step resolution	(RV2, RV1, RV0) from (1, 1, 0) to (1, 1, 1); note 3	–	9.5	12	dB
V_{IH}	HIGH level input voltage (pins RVx)		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage (pins RVx)		V_{SS}	–	$0.3V_{DD}$	V
I_{IH}	HIGH level input current (pins RVx)	V_{RVx} = HIGH	0	–	5	µA
I_{IL}	LOW level input current (pins RVx)	V_{RVx} = LOW	0	–	5	µA
RINGER MELODY INPUT AND PIEZO DRIVER (PINS RMI, ROA AND ROB)						
V_{IH}	HIGH level input voltage (pin RMI)		$0.51V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage (pin RMI)		V_{SS}	–	$0.49V_{DD}$	V
I_{IH}	HIGH level input current (pin RMI)	V_{RMI} = HIGH	0	–	10	µA
I_{IL}	LOW level input current (pin RMI)	V_{RMI} = LOW	–10	–	0	µA
$V_{o(min\ p\text{-}p)}$	minimum output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 0; RV1 = 0; RV0 = 0	–	0.15	–	V
$V_{o(p\text{-}p)}$	output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 1; RV1 = 1; RV0 = 0	–	9.6	–	V
$V_{o(max\ p\text{-}p)}$	maximum output voltage between pins ROA and ROB (peak-to-peak value)	RV2 = 1; RV1 = 1; RV0 = 1	–	28.7	32	V
$\lvert I_{RO} \rvert$	ROA or ROB output current capability	sink and source; RV2 = 1; RV1 = 1; RV0 = 1	80	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REGULATED MICROCONTROLLER SUPPLY (PIN V_{DD})						
V_{DD}	supply output voltage referenced to V_{SS}	$I_{DD} = -1$ mA	3.0	3.35	3.6	V
$\Delta V_{DD}/\Delta T$	supply output voltage temperature gradient		–	0	–	mV/K
I_{DD}	supply output current capability		–	–	−2	mA

Notes

1. I_{SS} has no influence on AGC characteristics of the TEA106x transmission circuit when V_{SS} is connected to the SLPE pin of TEA106x.
2. Independent of V_{RR} if greater than 10 V.
3. Without piezo transducer, dependent on V_{RR}.

TEST AND APPLICATION INFORMATION

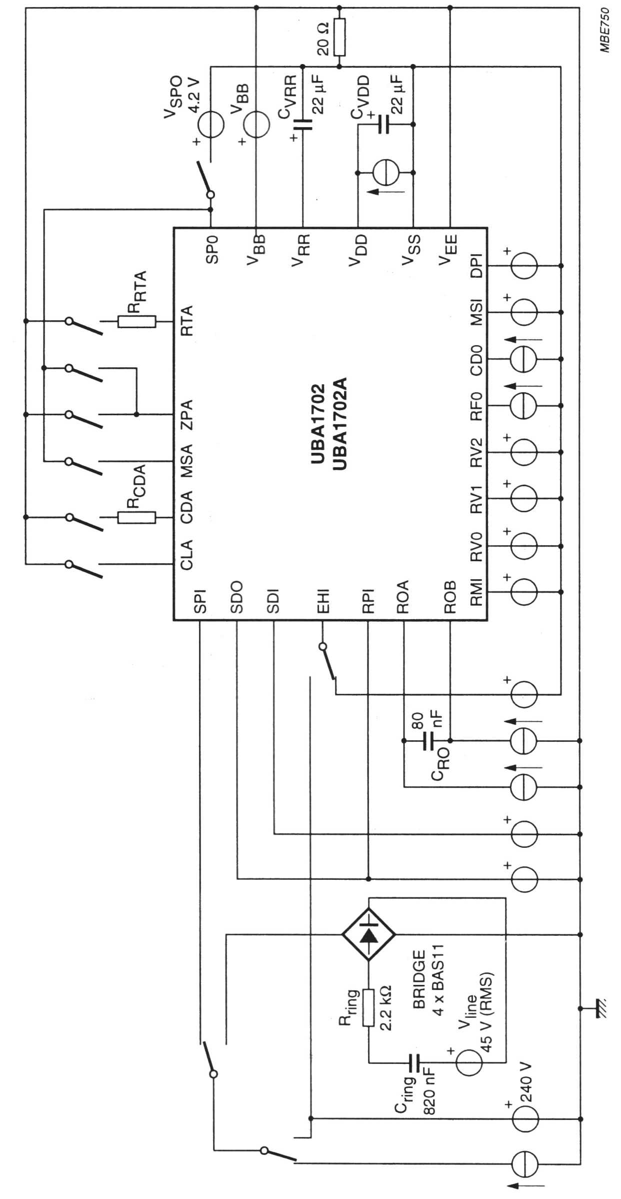

V_SPO
4.2 V
V_BB
C_VRR
22 µF
20 Ω
C_VDD
22 µF
MBE750
SP0
V_BB
V_RR
V_DD
V_SS
V_EE
DPI
MSI
CD0
RF0
RV2
RV1
RV0
RMI
R_RTA
RTA
ZPA
MSA
R_CDA
CDA
CLA
UBA1702
UBA1702A
SPI
SDO
SDI
EHI
RPI
ROA
ROB
80 nF
C_RO
R_ring
2.2 kΩ
BRIDGE
4 x BAS11
V_line
45 V (RMS)
C_ring
820 nF
240 V
+

Fig.4 Test circuit.

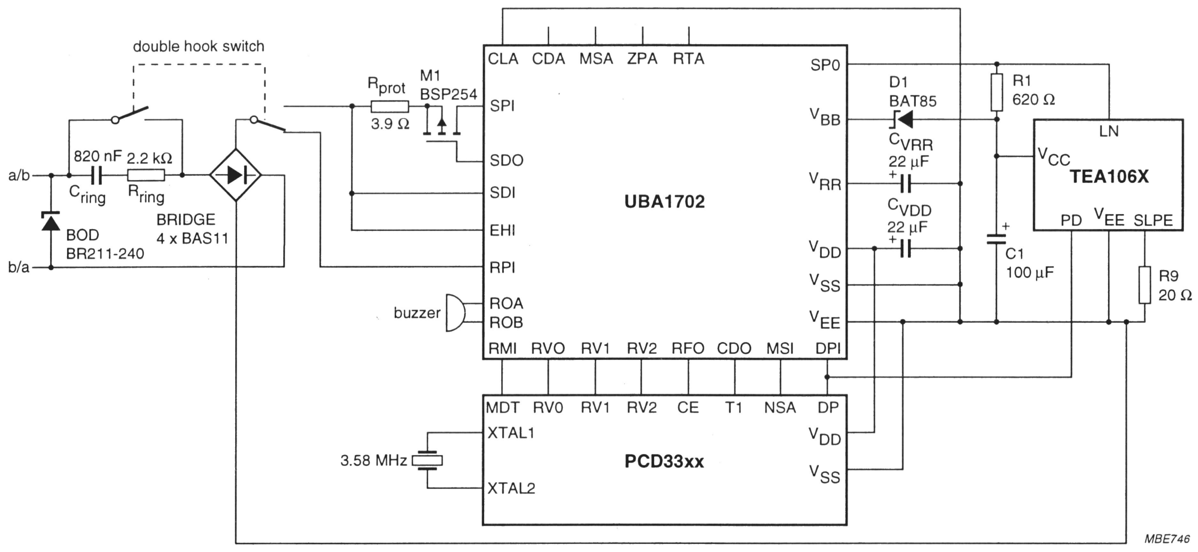

double hook switch
a/b
b/a
820 nF
C_{ring}
2.2 kΩ
R_{ring}
BOD
BR211-240
BRIDGE
4 x BAS11
R_{prot}
3.9 Ω
M1
BSP254
buzzer
3.58 MHz
UBA1702
CLA
CDA
MSA
ZPA
RTA
SPI
SDO
SDI
EHI
RPI
ROA
ROB
RMI
RVO
RV1
RV2
RFO
CDO
MSI
DPI
SP0
V_{BB}
V_{RR}
V_{DD}
V_{SS}
V_{EE}
PCD33xx
MDT
RV0
RV1
RV2
CE
T1
NSA
DP
XTAL1
XTAL2
V_{DD}
V_{SS}
D1
BAT85
C_{VRR}
22 μF
C_{VDD}
22 μF
R1
620 Ω
C1
100 μF
TEA106X
LN
V_{CC}
PD
V_{EE}
SLPE
R9
20 Ω
MBE746

Fig.5 Simplified basic application of the UBA1702 with the TEA106x.

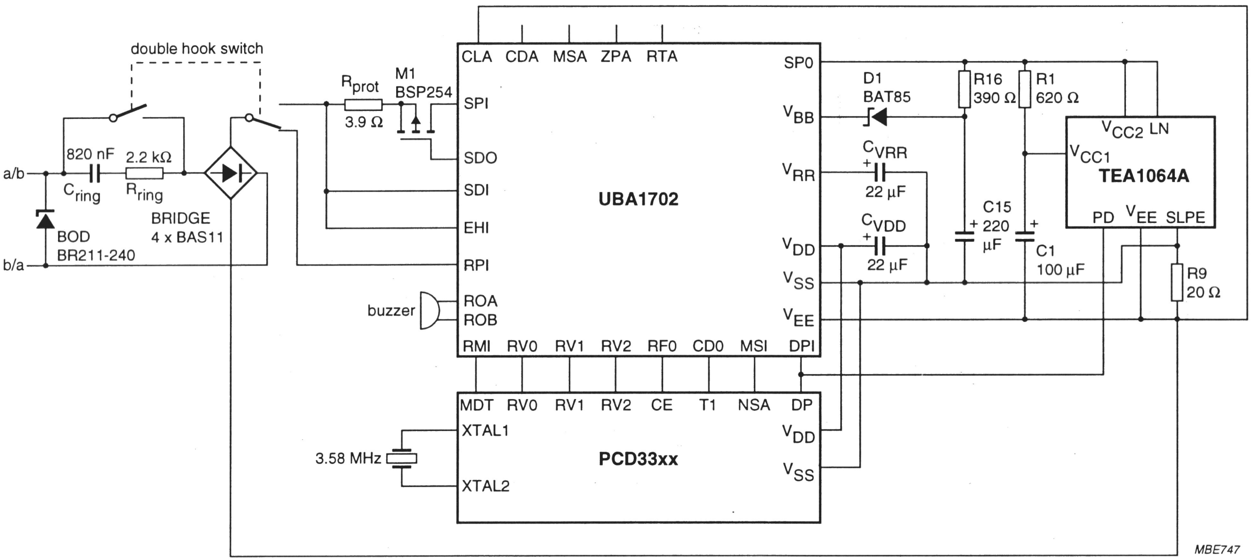

double hook switch
a/b
b/a
820 nF
C_{ring}
2.2 kΩ
R_{ring}
BOD
BR211-240
BRIDGE
4 x BAS11
R_{prot}
3.9 Ω
M1
BSP254
buzzer
3.58 MHz
UBA1702
CLA
CDA
MSA
ZPA
RTA
SPI
SDO
SDI
EHI
RPI
ROA
ROB
RMI
RV0
RV1
RV2
RF0
CD0
MSI
DPI
SP0
V_{BB}
V_{RR}
V_{DD}
V_{SS}
V_{EE}
PCD33xx
MDT
RV0
RV1
RV2
CE
T1
NSA
DP
XTAL1
XTAL2
V_{DD}
V_{SS}
D1
BAT85
C_{VRR}
22 μF
C_{VDD}
22 μF
R16
390 Ω
R1
620 Ω
C15
220 μF
C1
100 μF
TEA1064A
V_{CC2}
LN
V_{CC1}
PD
V_{EE}
SLPE
R9
20 Ω
MBE747

Fig.6 Simplified basic application of the UBA1702 with the TEA1064A.

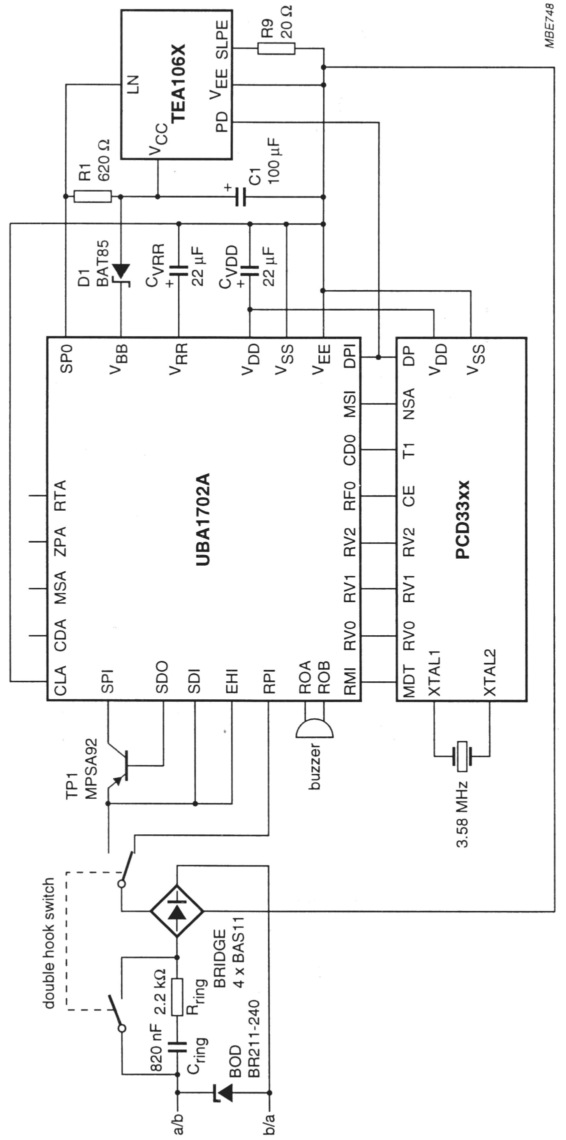
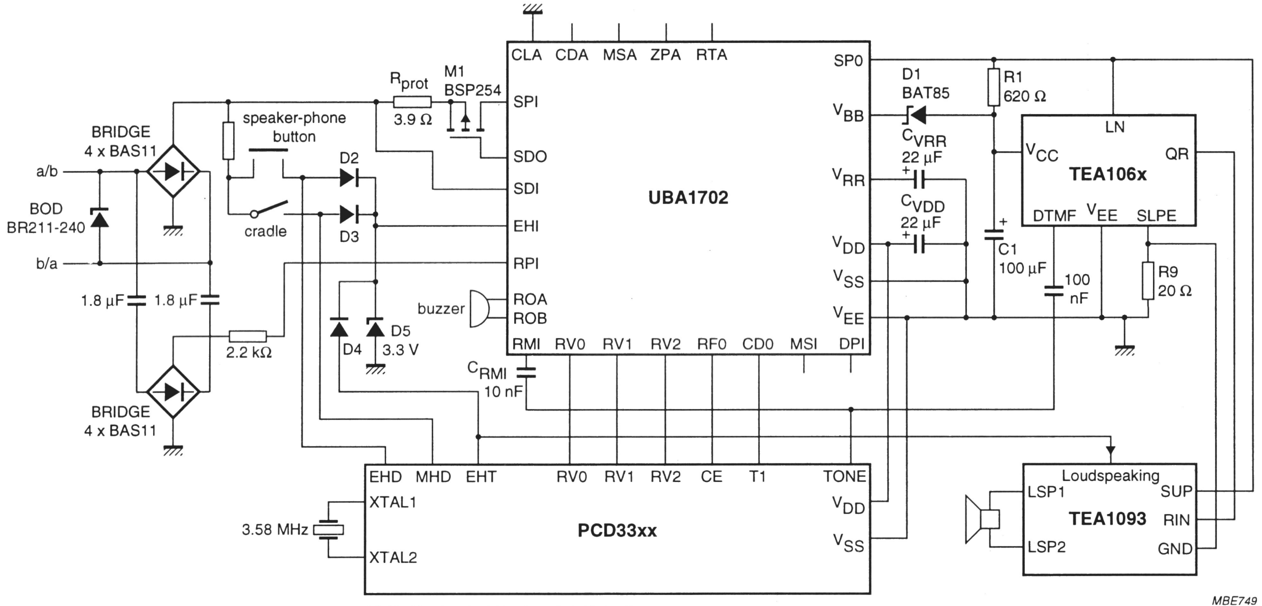

TEA106X
LN
V_{CC}
PD
V_{EE}
SLPE
R9
20 Ω
MBE748
R1
620 Ω
C1
100 μF
D1
BAT85
C_{VRR}
22 μF
C_{VDD}
22 μF
UBA1702A
SP0
V_{BB}
V_{RR}
V_{DD}
V_{SS}
V_{EE}
DPI
MSI
CD0
RF0
RV2
RV1
RV0
RMI
RTA
ZPA
MSA
CDA
CLA
SPI
SDO
SDI
EHI
RPI
ROA
ROB
PCD33xx
DP
V_{DD}
V_{SS}
NSA
T1
CE
RV2
RV1
RV0
MDT
XTAL1
XTAL2
3.58 MHz
buzzer
TP1
MPSA92
double hook switch
BRIDGE
4 x BAS11
2.2 kΩ
R_{ring}
820 nF
C_{ring}
BOD
BR211-240
a/b
b/a

Fig.7 Simplified basic application of the UBA1702A with the TEA106x.


CLA
CDA
MSA
ZPA
RTA
SP0
SPI
SDO
SDI
EHI
RPI
ROA
ROB
RMI
RV0
RV1
RV2
RF0
CD0
MSI
DPI
V_BB
V_RR
V_DD
V_SS
V_EE
UBA1702
R_prot
3.9 Ω
M1
BSP254
BRIDGE
4 x BAS11
a/b
BOD
BR211-240
b/a
speaker-phone
button
cradle
D2
D3
D4
D5
3.3 V
1.8 µF
1.8 µF
2.2 kΩ
BRIDGE
4 x BAS11
buzzer
C_RMI
10 nF
D1
BAT85
C_VRR
22 µF
C_VDD
22 µF
R1
620 Ω
C1
100 µF
100
nF
R9
20 Ω
LN
V_CC
QR
TEA106x
DTMF
V_EE
SLPE
EHD
MHD
EHT
RV0
RV1
RV2
CE
T1
TONE
XTAL1
XTAL2
V_DD
V_SS
PCD33xx
3.58 MHz
Loudspeaking
LSP1
LSP2
SUP
RIN
GND
TEA1093
MBE749

MHD: Mechanical Hook switch Detection
EHD: Electronic Hook switch Detection
EHT: Electronic Hook switch Take-over

Fig.8 Simplified proposal for electronic hook switch application of the UBA1702 in combination with a transmission and a hands-free circuit.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

FEATURES

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	240	V
V_{GSth}	gate-source threshold voltage	2	V
I_D	drain current (DC)	210	mA
R_{DSon}	drain-source on-state resistance	6	Ω

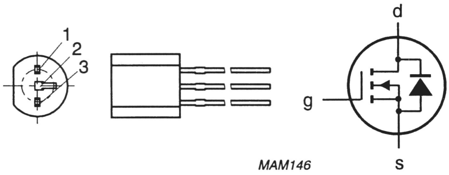


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON P-N-P HIGH-VOLTAGE TRANSISTORS

P-N-P high-voltage small-signal transistors for general purposes and especially in telephony applications and encapsulated in a TO-92 package.

N-P-N complements are 2N5550 and 2N5551.

QUICK REFERENCE DATA

			2N5400	2N5401	
Collector-base voltage (open emitter)	$-V_{CBO}$	max.	130	160	V
Collector-emitter voltage (open base)	$-V_{CEO}$	max.	120	150	V
Collector current	$-I_C$	max.	600	600	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	500	500	mW
Junction temperature	T_j	max.	150	150	°C
Collector-emitter saturation voltage I_C = 50 mA; I_B = 5 mA	V_{CEsat}	max.	0,5	0,5	V
D.C. current gain I_C = 10 mA; V_{CE} = −5 V	h_{FE}	min.	40	60	

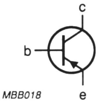
MECHANICAL DATA

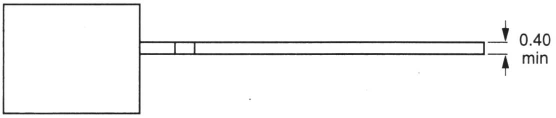
Dimensions in mm

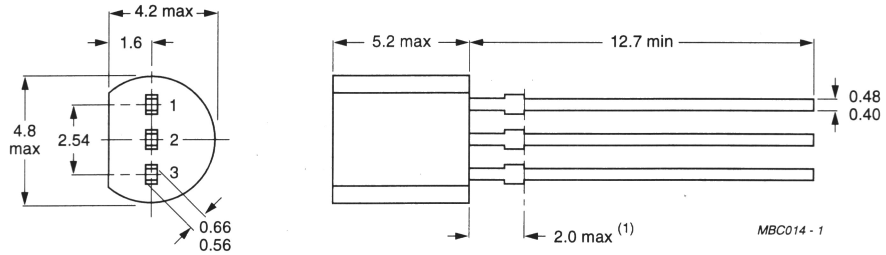
Fig. 1 TO-92.

Pinning

1 = collector
2 = base
3 = emitter







Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

FOR MORE DETAILED INFORMATION SEE LATEST ISSUE OF HANDBOOK SC04 OR DATA SHEET

SILICON N-P-N HIGH-VOLTAGE TRANSISTORS

N-P-N high-voltage small-signal transistors for general purposes and especially telephony applications and encapsulated in a TO-92 package.

P-N-P complements are 2N5400 and 2N5401.

QUICK REFERENCE DATA

			2N5550	2N5551	
Collector-base voltage (open emitter)	V_{CBO}	max.	160	180	V
Collector-emitter voltage (open base)	V_{CEO}	max.	140	160	V
Collector current	I_C	max.	600	600	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	500	500	mW
Junction temperature	T_j	max.	150	150	°C
Collector-emitter saturation voltage I_C = 50 mA; I_B = 5 mA	V_{CEsat}	max.	0,25	0,20	V
D.C. current gain I_C = 10 mA; V_{CE} = 5 V	h_{FE}	min.	60	80	

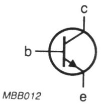
MECHANICAL DATA

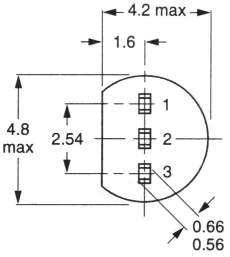
Dimensions in mm

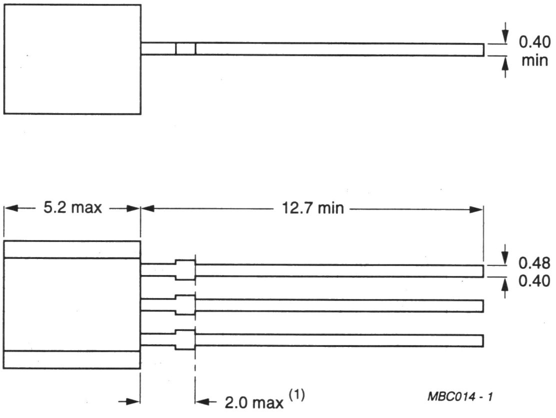
Fig. 1 TO-92.

Pinning

1 = collector
2 = base
3 = emitter







Note (1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Data sheet	
status	Product specification
date of issue	April 1995

2N7000

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	280	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

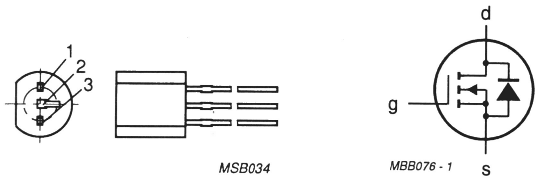


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

2N7002
N-channel vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	3	V

PIN CONFIGURATION

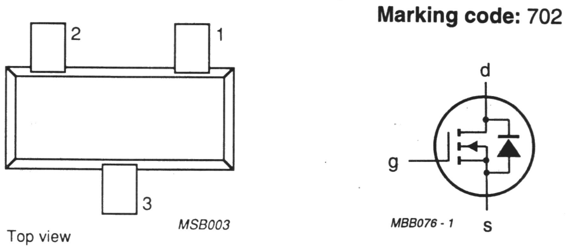


Fig.1 Simplified outline and symbol.

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

PACKAGE INFORMATION

Page

Package outlines 874

Soldering 897

PACKAGES

Packages in ascending order of packages outline version

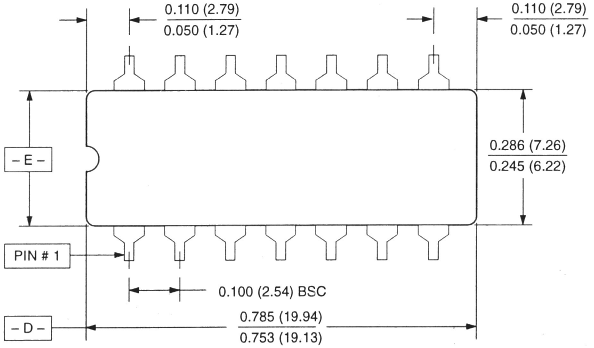
PACKAGE OUTLINE VERSION CODE (RENAMED)	PACKAGE VERSION CODE (NON-STANDARD)	PACKAGE NAME	DESCRIPTION	PAGE
SOT27-1	SOT27	DIP14	plastic dual in-line package; 14 leads (300 mil)	878
SOT38-1	SOT38	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	879
SOT38-4		DIP16	plastic dual in-line package; 16 leads (300 mil)	880
SOT96-1	SOT96A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	888
SOT97-1	SOT97; SOT97D	DIP8	plastic dual in-line package; 8 leads (300 mil)	877
SOT101-1	SOT101B; SOT101L	DIP24	plastic dual in-line package; 24 leads (600 mil)	883
SOT102-1	SOT102	DIP18	plastic dual in-line package; 18 leads (300 mil)	881
SOT108-1		SO14	plastic small outline package; 14 leads; body width 3.9 mm	890
SOT109-1		SO16	plastic small outline package; 16 leads; body width 3.9 mm	891
SOT117-1	SOT117	DIP28	plastic dual in-line package; 28 leads (600 mil)	884
SOT136-1	SOT136A	SO28	plastic small outline package; 28 leads; body width 7.5 mm	895
SOT137-1	SOT137A	SO24	plastic small outline package; 24 leads; body width 7.5 mm	894
SOT146-1	SOT146	DIP20	plastic dual in-line package; 20 leads (300 mil)	882
SOT162-1	SOT162A; SOT162AG	SO16	plastic small outline package; 16 leads; body width 7.5 mm	892
SOT163-1	SOT163A	SO20	plastic small outline package; 20 leads; body width 7.5 mm	893
SOT176-1	SOT176C	SO8	plastic small outline package; 8 leads; body width 7.5 mm	889
SOT205-1		QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	886
SOT270-1		SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	887
SOT358-1		LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	885
SOT369-1		SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	896
–	0581B	CDIP14	ceramic dual in-line (F) package; 14 leads (300 mil)	876

Packages in ascending order of package name

PACKAGE NAME	PACKAGE OUTLINE VERSION CODE (RENAMED)	PACKAGE VERSION CODE (NON-STANDARD)	DESCRIPTION	PAGE
CDIP				
CDIP14	–	0581B	ceramic dual in-line (F) package; 14 leads (300 mil)	876
DIP				
DIP8	SOT97-1	SOT97; SOT97D	plastic dual in-line package; 8 leads (300 mil)	877
DIP14	SOT27-1	SOT27	plastic dual in-line package; 14 leads (300 mil)	878
DIP16	SOT38-1	SOT38	plastic dual in-line package; 16 leads (300 mil); long body	879
DIP16	SOT38-4		plastic dual in-line package; 16 leads (300 mil)	880
DIP18	SOT102-1	SOT102	plastic dual in-line package; 18 leads (300 mil)	881
DIP20	SOT146-1	SOT146	plastic dual in-line package; 20 leads (300 mil)	882
DIP24	SOT101-1	SOT101B; SOT101L	plastic dual in-line package; 24 leads (600 mil)	883
DIP28	SOT117-1	SOT117	plastic dual in-line package; 28 leads (600 mil)	884
LQFP				
LQFP32	SOT358-1		plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	885
QFP				
QFP44	SOT205-1		plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	886
SDIP				
SDIP42	SOT270-1		plastic shrink dual in-line package; 42 leads (600 mil)	887
SO				
SO8	SOT96-1	SOT96A	plastic small outline package; 8 leads; body width 3.9 mm	888
SO8	SOT176-1	SOT176C	plastic small outline package; 8 leads; body width 7.5 mm	889
SO14	SOT108-1		plastic small outline package; 14 leads; body width 3.9 mm	890
SO16	SOT109-1		plastic small outline package; 16 leads; body width 3.9 mm	891
SO16	SOT162-1	SOT162A; SOT162AG	plastic small outline package; 16 leads; body width 7.5 mm	892
SO20	SOT163-1	SOT163A	plastic small outline package; 20 leads; body width 7.5 mm	893
SO24	SOT137-1	SOT137A	plastic small outline package; 24 leads; body width 7.5 mm	894
SO28	SOT136-1	SOT136A	plastic small outline package; 28 leads; body width 7.5 mm	895
SSOP				
SSOP16	SOT369-1		plastic shrink small outline package; 16 leads; body width 4.4 mm	896

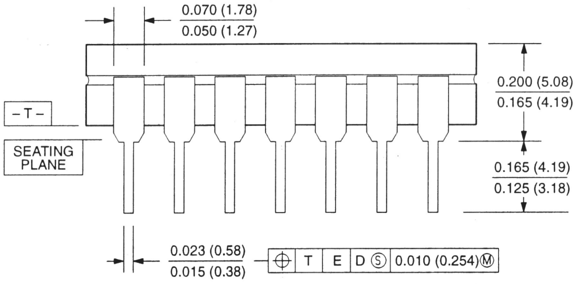
CDIP

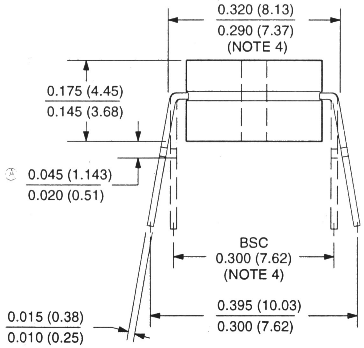
Ceramic Dual In-Line (F) package; 14 leads (300 mil) **0581B**


0.110 (2.79)
0.050 (1.27)
0.110 (2.79)
0.050 (1.27)
– E –
0.286 (7.26)
0.245 (6.22)
PIN # 1
0.100 (2.54) BSC
– D –
0.785 (19.94)
0.753 (19.13)

NOTES:

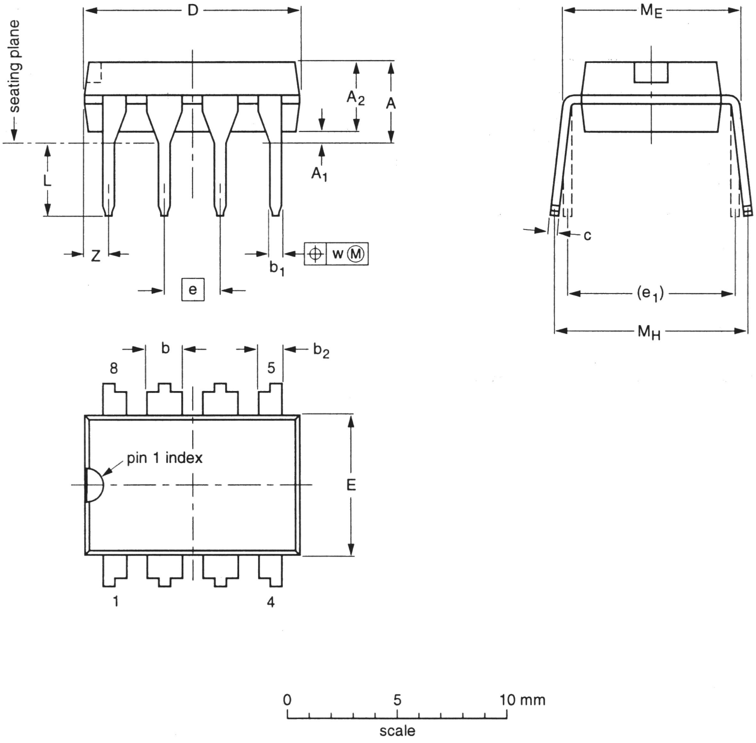
1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.


0.070 (1.78)
0.050 (1.27)
– T –
SEATING PLANE
0.200 (5.08)
0.165 (4.19)
0.165 (4.19)
0.125 (3.18)
0.023 (0.58)
0.015 (0.38)
T
E
D Ⓢ
0.010 (0.254)Ⓜ


0.320 (8.13)
0.290 (7.37)
(NOTE 4)
0.175 (4.45)
0.145 (3.68)
0.045 (1.143)
0.020 (0.51)
BSC
0.300 (7.62)
(NOTE 4)
0.015 (0.38)
0.010 (0.25)
0.395 (10.03)
0.300 (7.62)

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

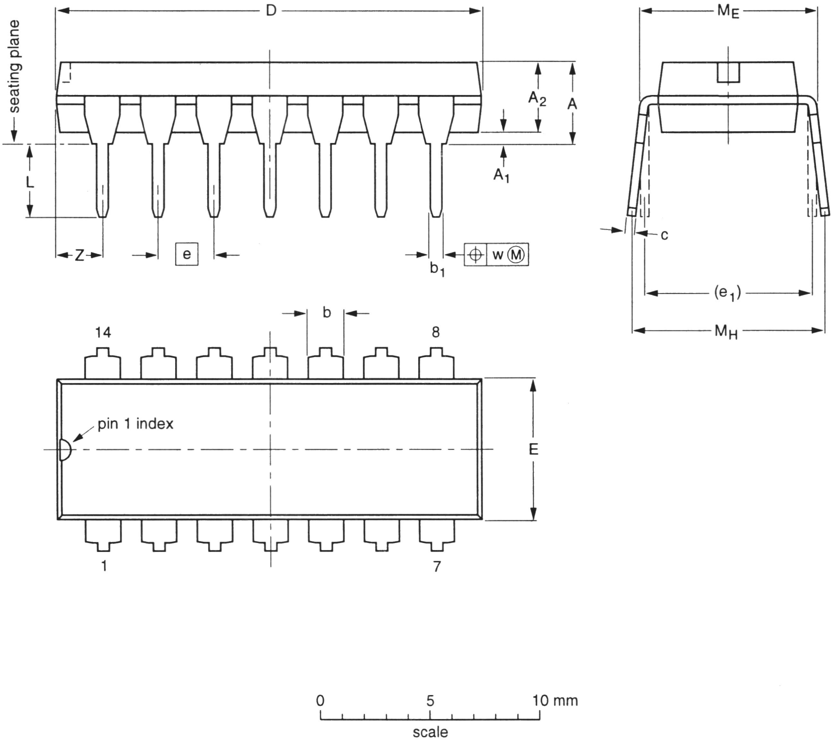
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

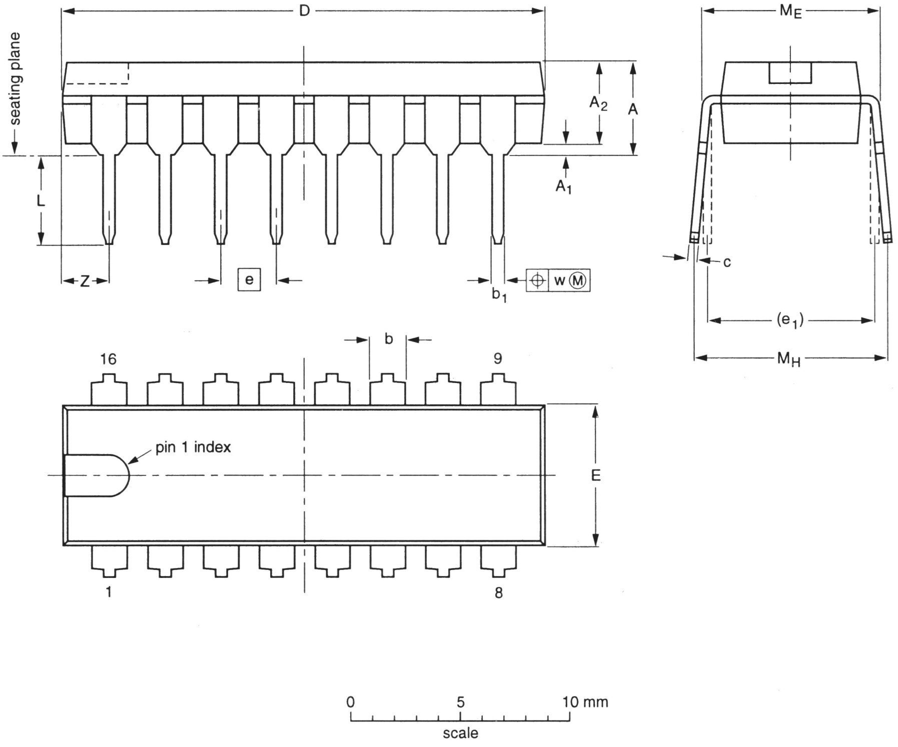
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

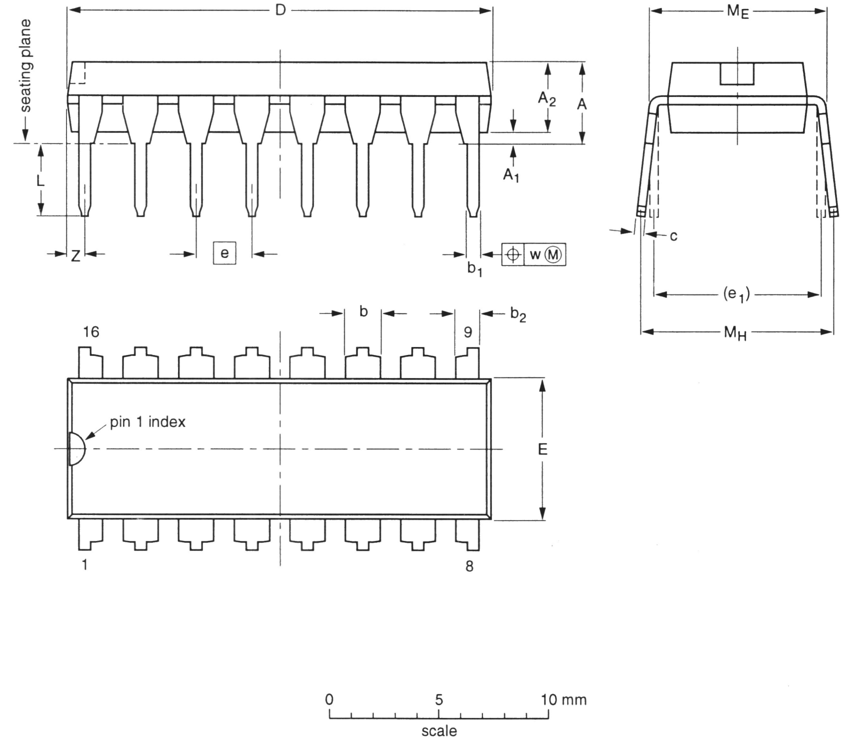
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

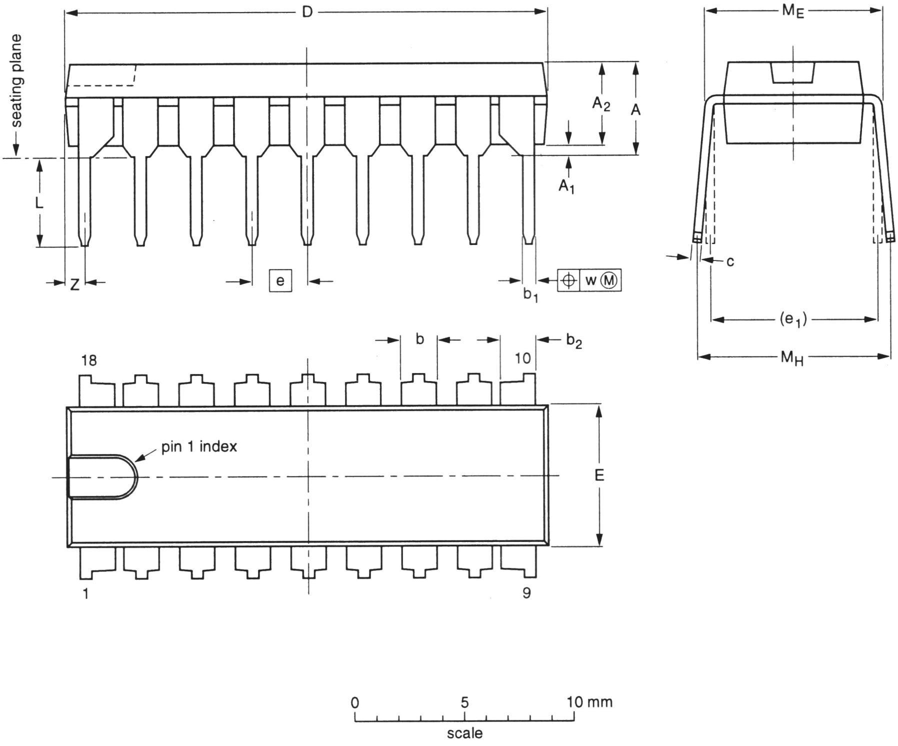
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

DIP18: plastic dual in-line package; 18 leads (300 mil) SOT102-1


D
seating plane
A_2
A
A_1
L
Z
e
b_1
w M
b
b_2
18
10
pin 1 index
E
1
9
M_E
c
(e_1)
M_H
0
5
10 mm
scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

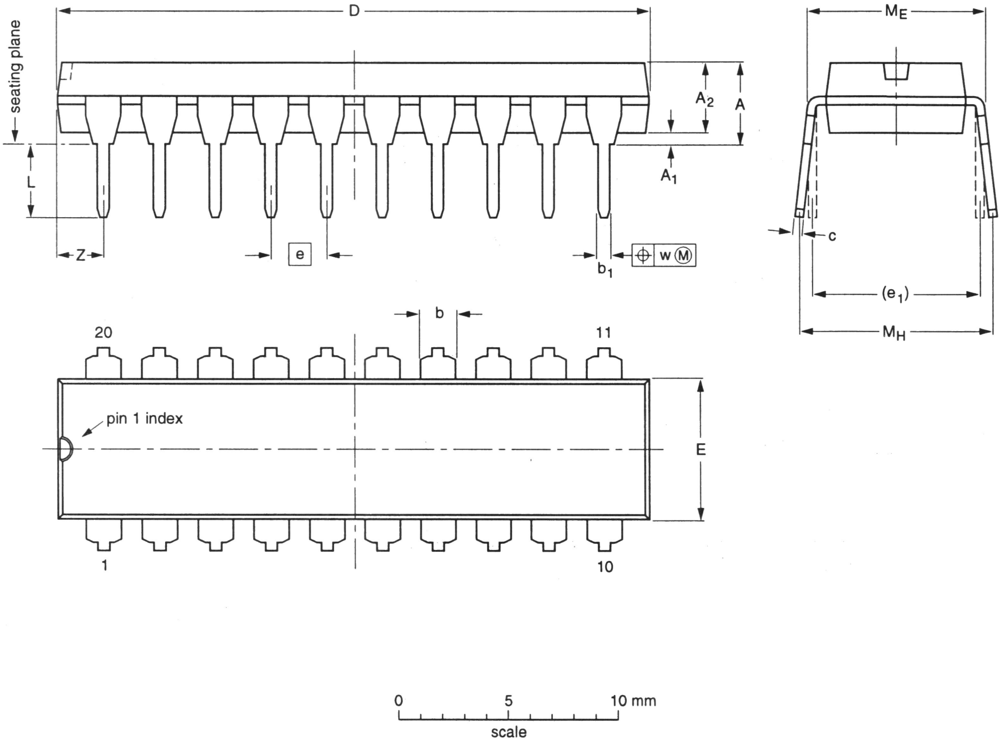
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**


D
seating plane
A2
A
A1
L
Z
e
b1
w M
ME
c
(e1)
MH
b
20
11
pin 1 index
E
1
10
0
5
10 mm
scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

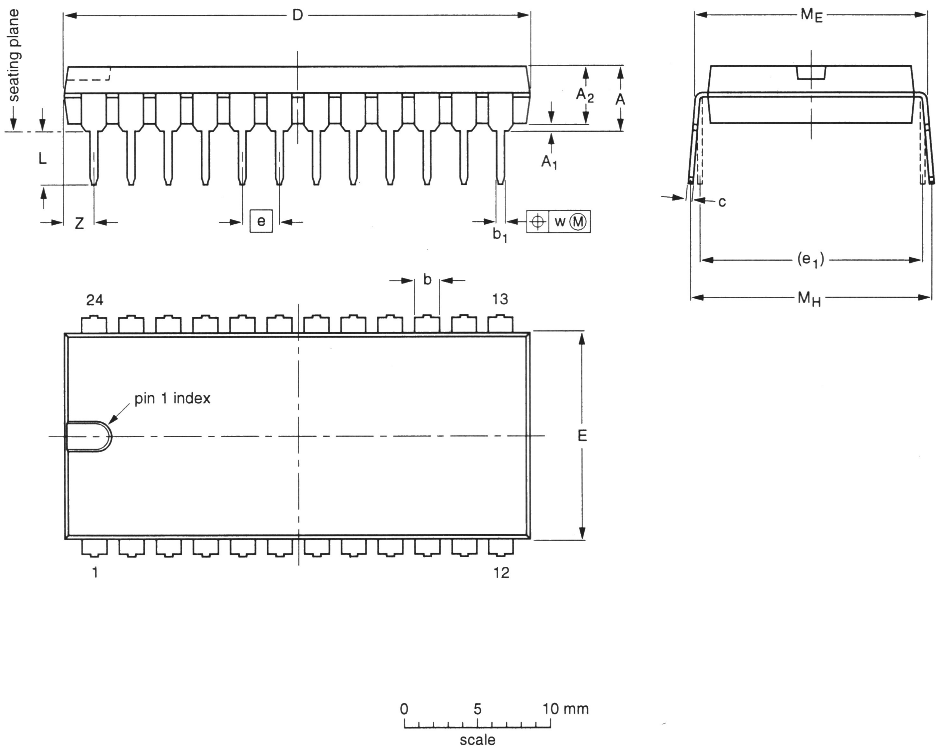
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

DIP24: plastic dual in-line package; 24 leads (600 mil) SOT101-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

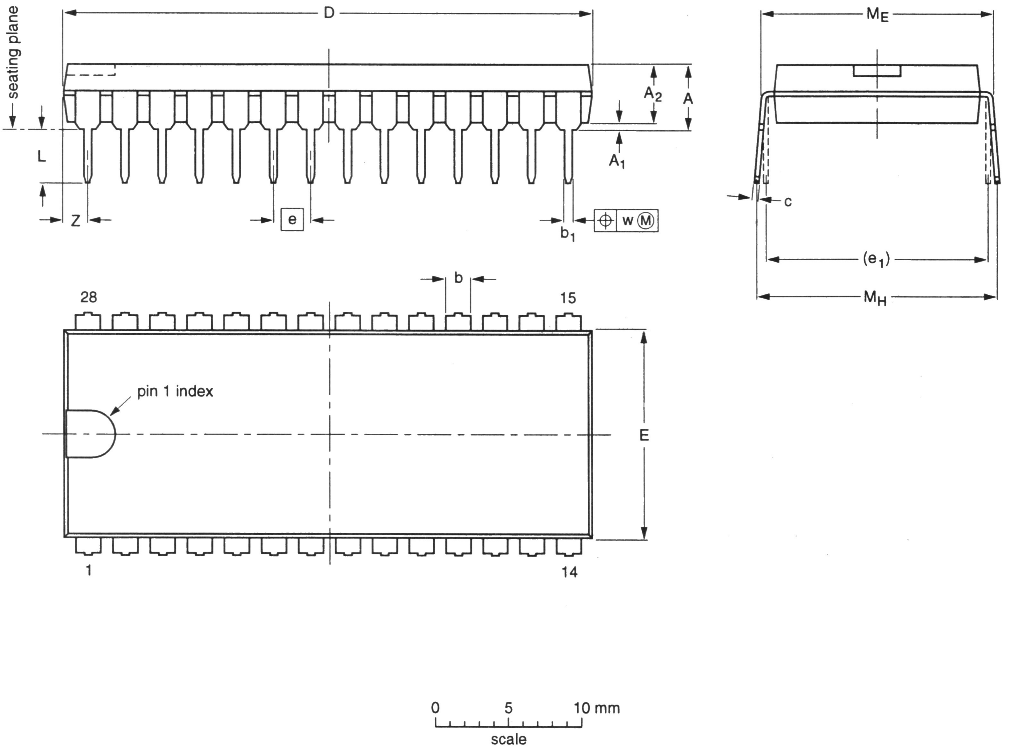
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

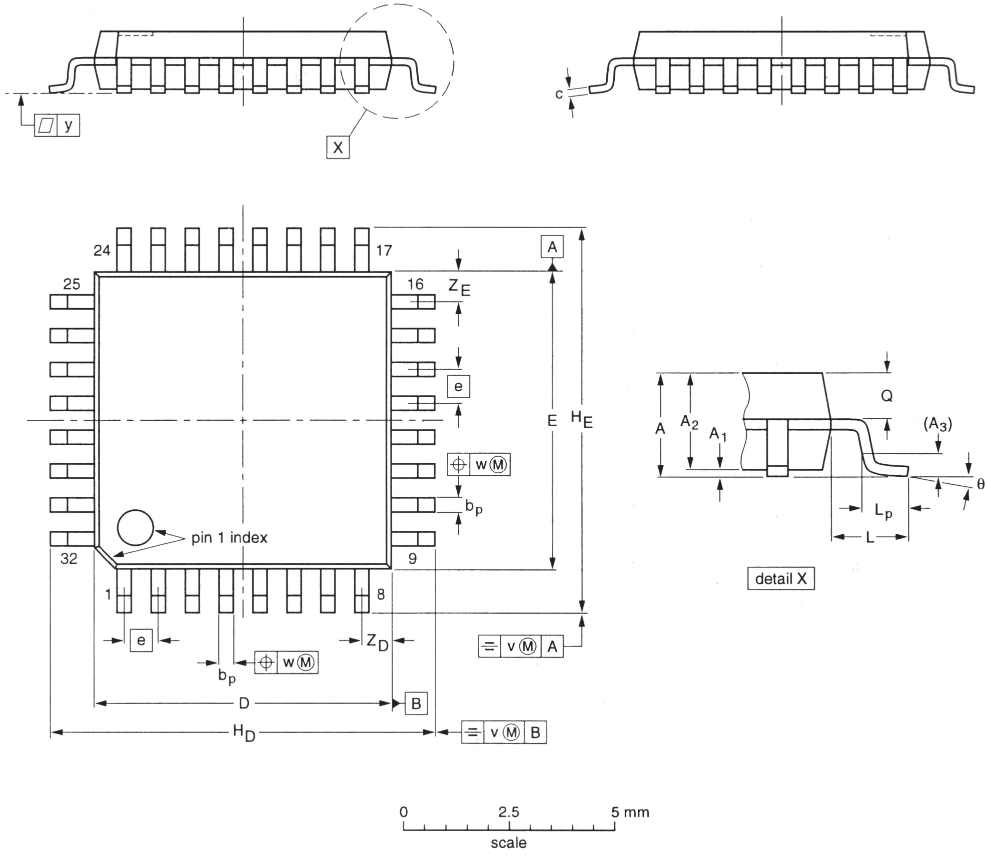
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

LQFP

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm SOT358-1


y
X
c
24
17
25
16
Z_E
A
e
E
H_E
w M
b_p
pin 1 index
32
9
1
8
e
Z_D
v M A
b_p
w M
D
B
H_D
v M B
Q
A
A_2
A_1
(A_3)
θ
L_p
L
detail X
0
2.5
5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

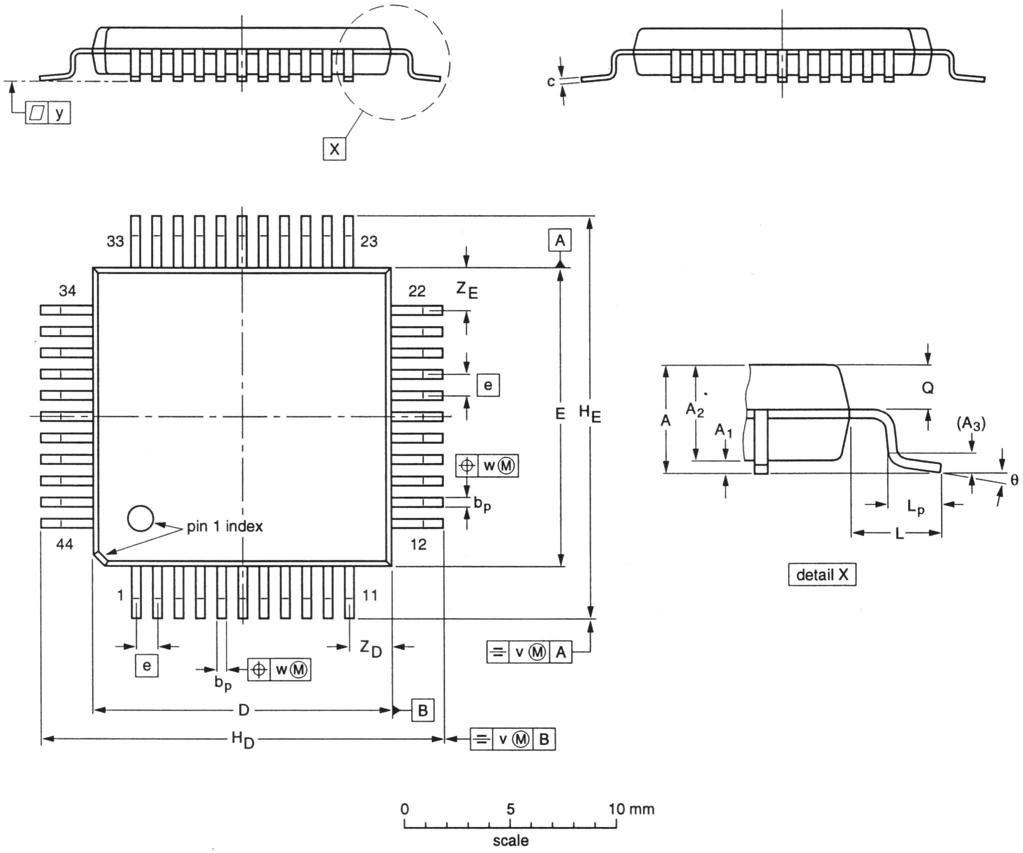
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~93-06-29~~ 95-12-19

QFP

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm SOT205-1


y
X
c
33
23
34
22
Z_E
A
e
E
H_E
w M
b_p
pin 1 index
44
12
1
11
e
Z_D
b_p
w M
v M A
D
B
H_D
v M B
Q
A
A_2
A_1
(A_3)
θ
L_p
L
detail X
0
5
10 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	1.2 0.9	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7° 0°

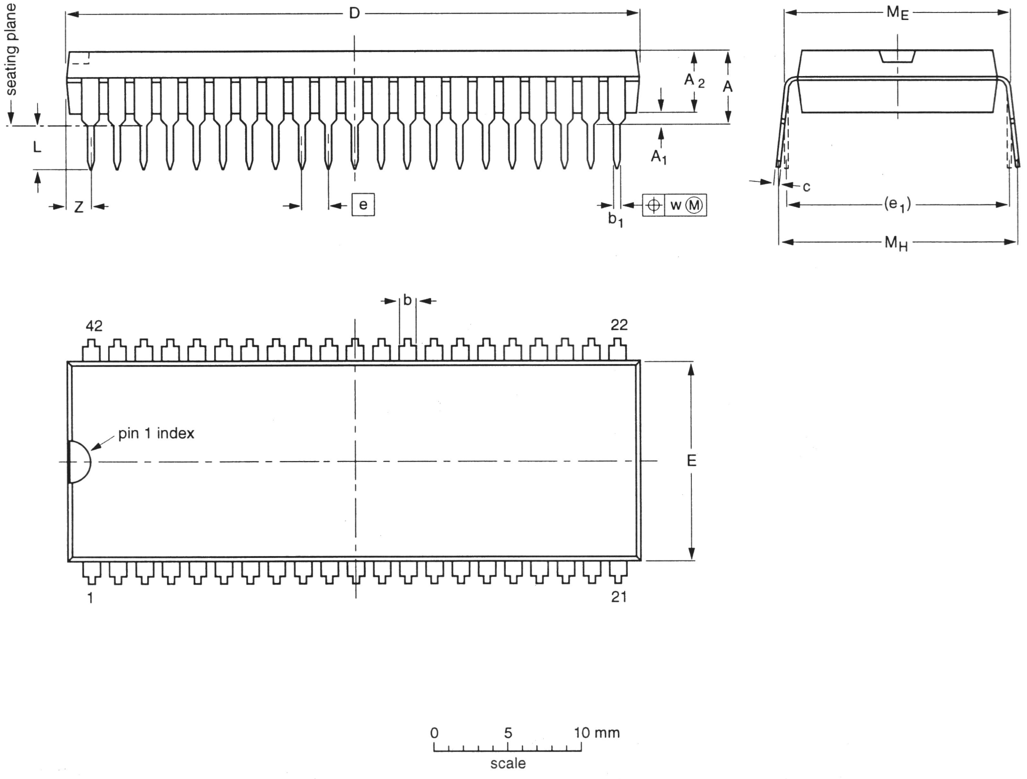
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~92-11-17~~ 95-02-04

SDIP

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) SOT270-1


seating plane
D
A_2
A
A_1
L
Z
e
b_1
w M
M_E
c
(e_1)
M_H
b
42
22
pin 1 index
E
1
21
0
5
10 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

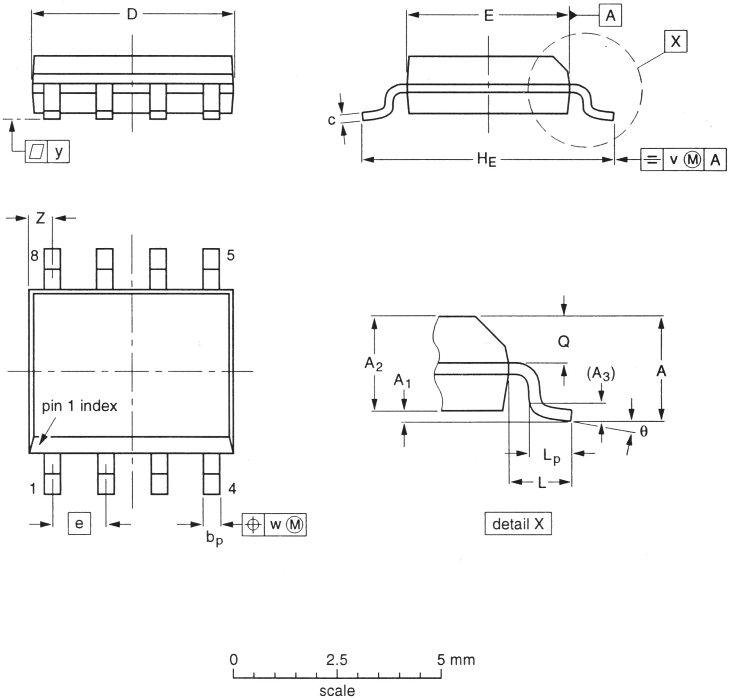
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

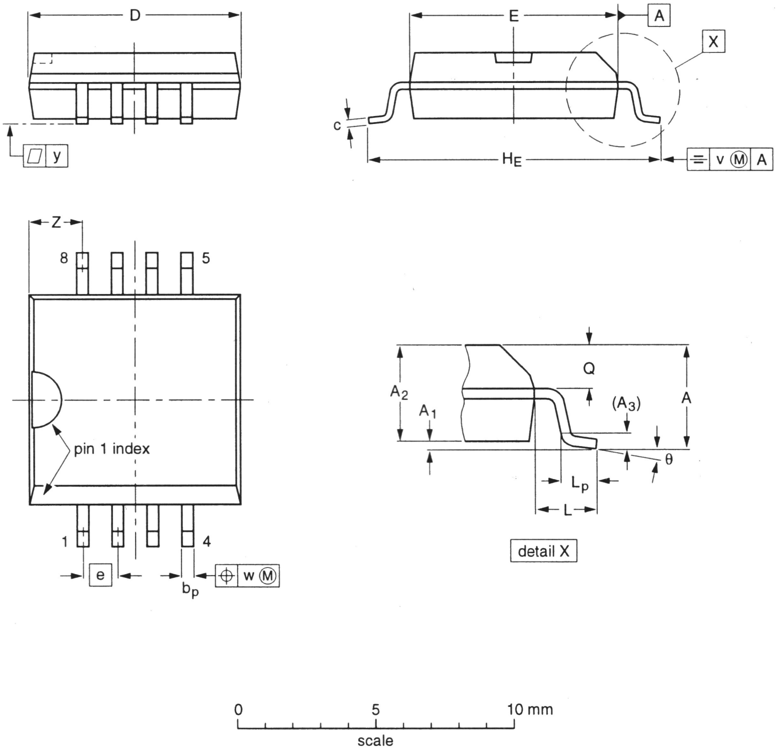
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

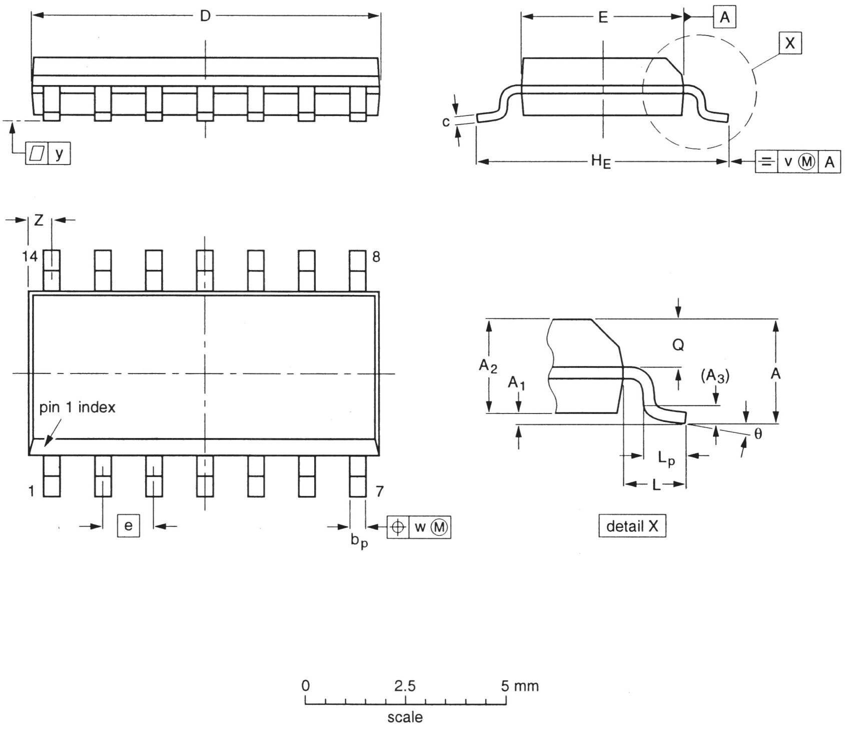
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.42 0.39	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~91-08-13~~ 95-02-25

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

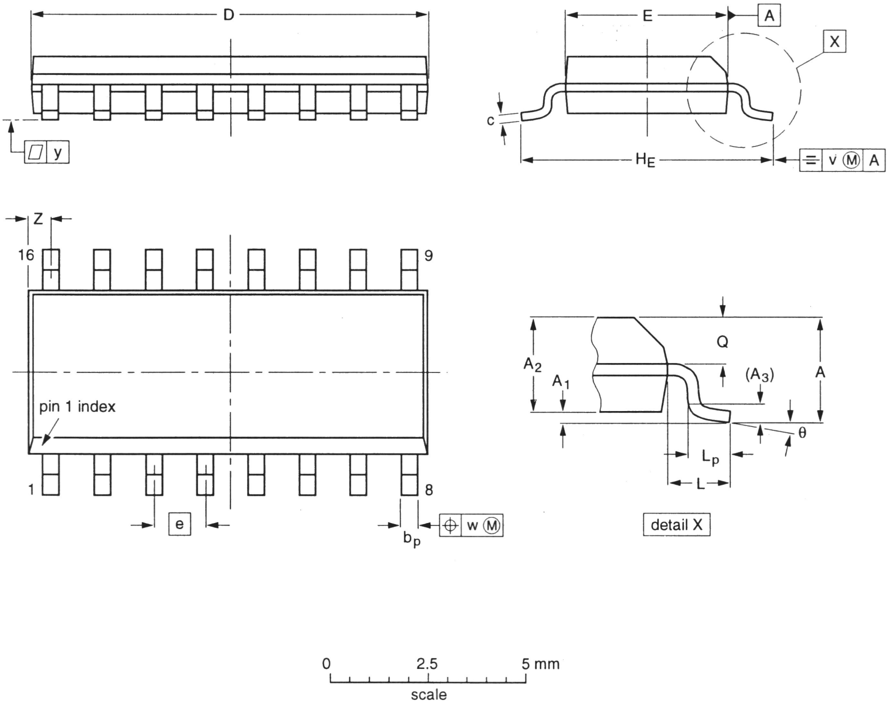
UNIT	A max.	A_1	A_2	A_3	b_p	c	D$^{(1)}$	E$^{(1)}$	e	H_E	L	L_p	Q	v	w	y	Z$^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~91-08-13~~ 95-01-23

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

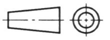


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

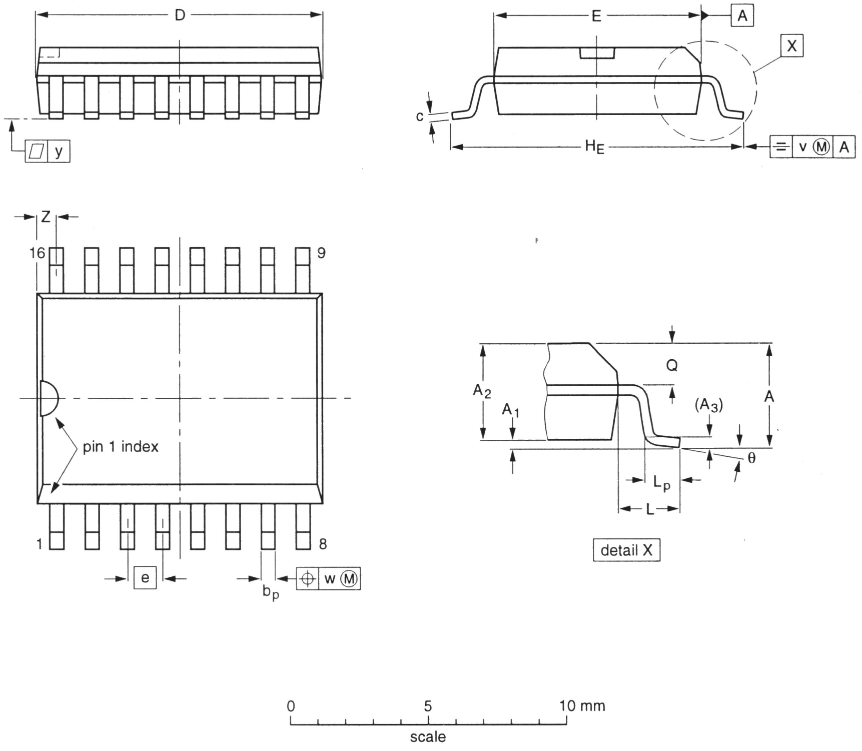
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SO16: plastic small outline package; 16 leads; body width 7.5 mm SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

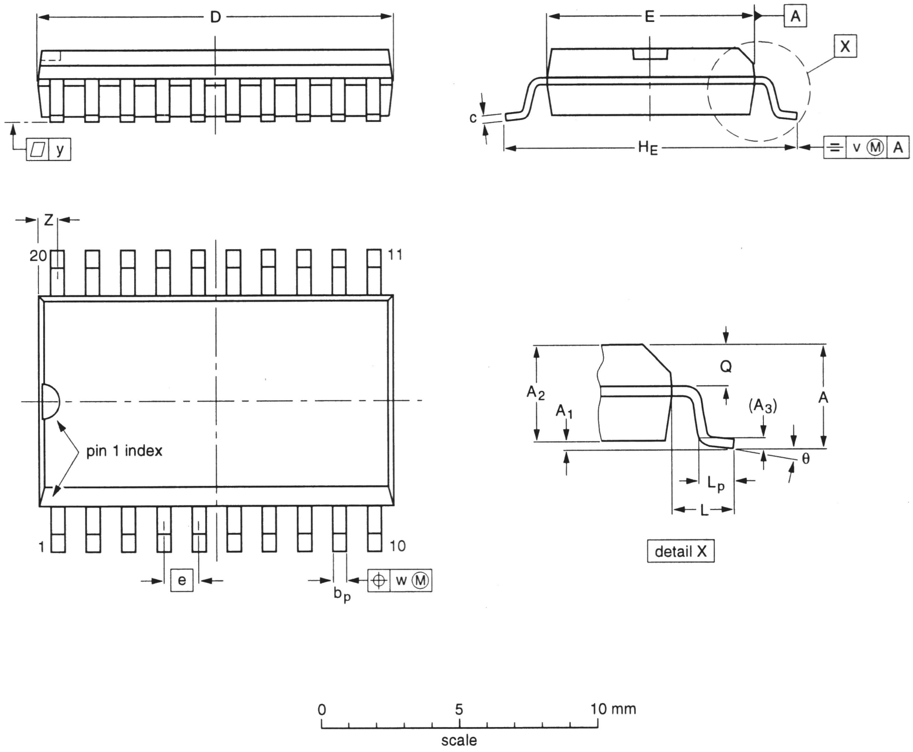
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

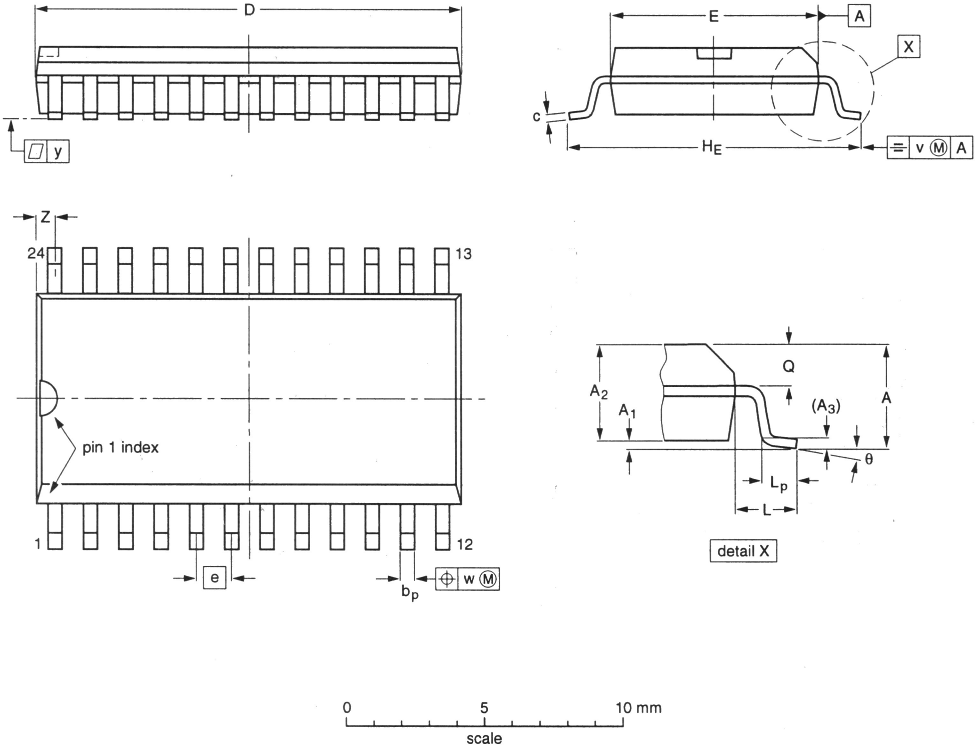
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

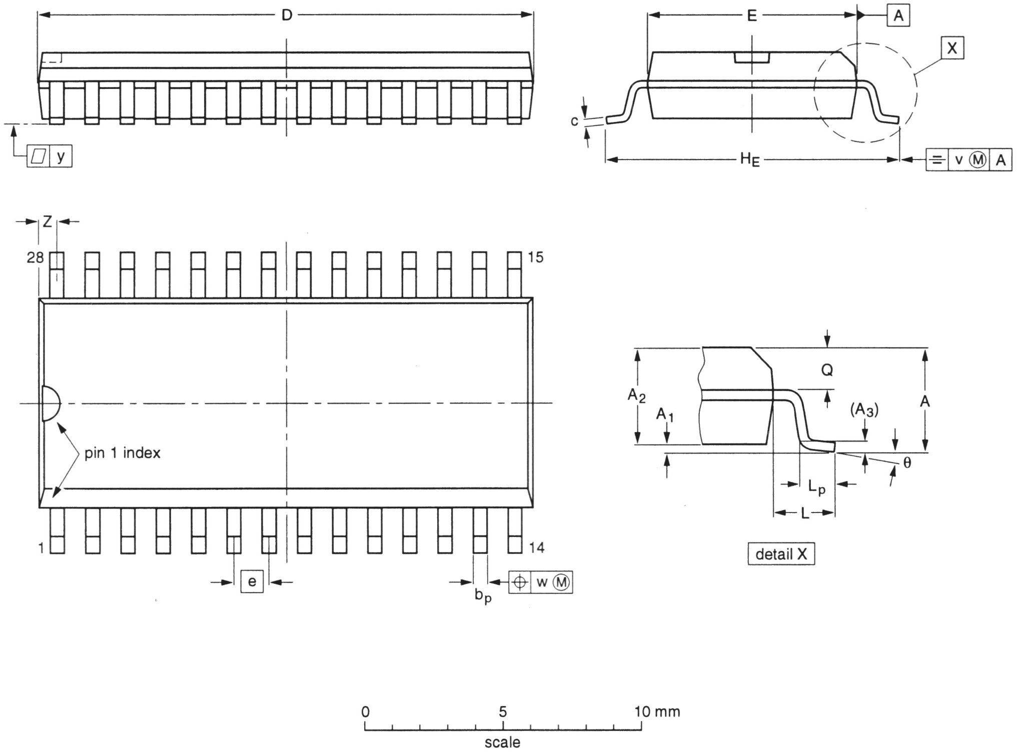
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SO28: plastic small outline package; 28 leads; body width 7.5 mm SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

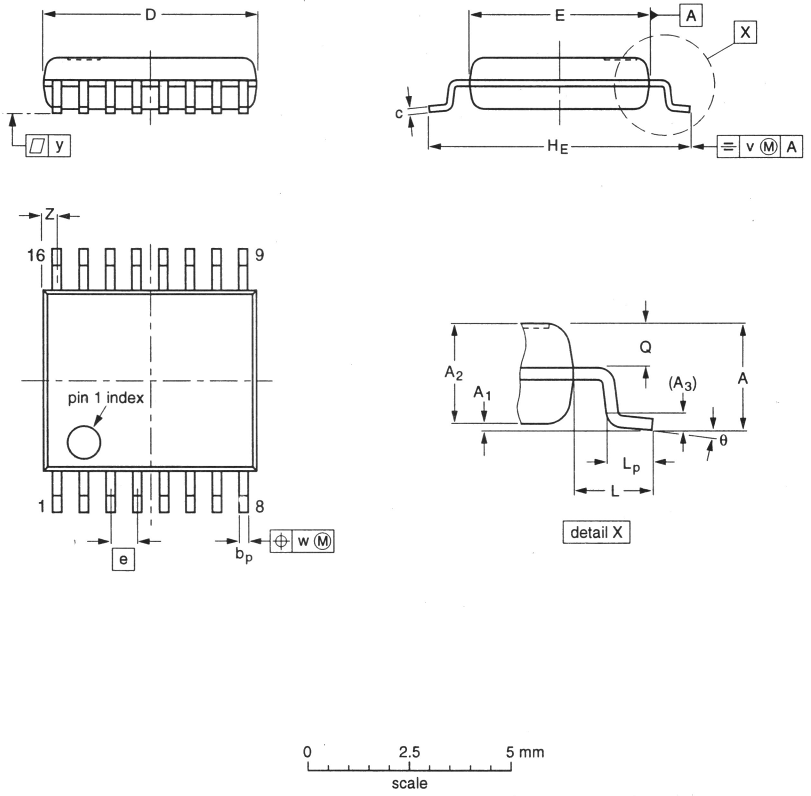
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SSOP

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm SOT369-1


D
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X
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y
Z
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9
pin 1 index
1
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A_2
A_1
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(A_3)
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L_p
L
detail X
0
2.5
5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						~~94-04-20~~ 95-02-04

Table 3 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DATA HANDBOOK SYSTEM

Data handbook system

DATA HANDBOOK SYSTEM

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SC08b	RF Power Transistors for UHF
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Data handbook system

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